Frequency-Modulated Continuous-Wave Radar

Group 16
Mikayla Peña (EE)
Casey Sanchez (EE)
Sebastian Peralta (EE)
Fahim Ahmed (EE)

Sponsor: Dr. Xun Gong, UCF Professor

April 25, 2023

Table of Contents

1.0 Executive Summary

Radar systems have become a prevalent technology in modern times. Due to their versatility, they can be found in a variety of applications, from tracking global weather patterns to mapping terrain. Parameters such as frequency, antenna size, antenna number, power level and mobility all play a part in determining a particular radar's capabilities and what kind of information can be extracted from its received signal. Although large, high-power radar systems have their place, particularly in the defense and aerospace industries, small-scale radar are oftentimes better suited for everyday consumer use. These systems can be used for applications where high power and large range are not necessary, but relatively small dimensions, ease of use, low cost, and direct access to the necessary information is a priority.

One piece of information that radar systems are often used to find is the velocity of objects in the radar's field of view; this system is often referred to as a Doppler radar given that it uses the Doppler effect to calculate the velocities. This velocity information can be used simply to analyze an environment, or it could be used to control an additional subsystem. Another piece of information radar systems can provide is the range of objects in the radar's field of view. Our team planned to build a portable, frequency-modulated continuous-wave (FMCW) radar module that could provide both range and velocity measurements from a dynamic environment.

The project was divided into the following subsystems: high-frequency RF, low-frequency RF, power supply, and software. A signal of a certain frequency will be transmitted from the radar module, and that signal will bounce off objects in the environment and return to the radar receive antenna. The signal is then filtered and amplified in hardware. This filtered, amplified signal is sent to the host and run through code to generate either the velocity or range plot.

2.0 Project Description

2.1 Motivation

Radar system design is highly diverse from a technical perspective, spanning topics from wireless communication to programming digital user interfaces. A project such as our radar system therefore involved knowledge of several electrical engineering subdisciplines. Design of the FMCW radar itself required knowledge of microwave signal propagation and radio frequency signal processing. The low-frequency RF subsystem design required knowledge of basic electronic circuits such as modulators, amplifiers, and filters. And the software aspect of the project required knowledge of digital signal processing and frequency analysis. This means that each of our team members had the opportunity to demonstrate technical ability in the area related to their academic subfield. Additionally, due to signals traveling through the subsystems sequentially, team members needed to have a basic understanding of subsystems interacting with their individual subsystem. This afforded an excellent opportunity for the team to expand our knowledge beyond the subfield-specific courses we have chosen on

our academic track. The diversity in our system's technical requirements and the subsystem interconnectivity presented a challenge that our team was ready and willing to take on.

Another motivation our team had for completing this project was the wide range of possibilities for application of our system. We only demonstrated two applications of our system for academic purposes, but in reality, our system could be used for many other things. The main advantage of our system is that the radar module is portable, meaning it is ideal for aiming at different targets while maintaining its wide field of view. Tracking the speed of vehicles, measuring terrain height, and monitoring activity in parking garages are just a few examples of how our system could be used.

Lastly, one of our main focuses was creating a consumer product. Given our constraints, our end product for academic purposes has left much room for future improvement from a marketing standpoint. Consumer needs would ultimately drive further development of the system design, both on the hardware and software side. The software capability could be expanded to extract additional parameters from the radar data or present the data in real-time rather than after data collection. The hardware could be modified to allow for the radar frequency or power to be set by the user, according to what is required of the specific application. The size and aesthetics of the system could also be improved. Completing our project was just the first step to creating a highly successful, marketable product.

2.2 Goals

There were three goal categories for our project. The first category involved post-measurement processing. This means that the radar is activated, the received data is recorded, and then the corresponding velocity or range plot is generated for the entire time period of the recording. The second goal category involved real-time processing, meaning that signals are being processed and measurements are displayed as the radar is running. The last goal category involved taking the velocity and range information provided by the radar and using it to run a control system.

There were two goals in category one. Our team wanted to use the radar to measure the range of people walking in an Engineering II hallway on UCF's campus. To demonstrate the velocity capabilities of the radar, our team wanted to measure the speed of cars driving on Pegasus Drive, which is near the engineering buildings on campus. The goals in category two were the same as those in category one except the measurements would be displayed in real-time. Lastly, category three contained the single goal of using either real-time range or real-time velocity readings to drive a control system.

In addition to the team's technical goals, there were also project management goals the team strived to achieve. The first was closely related to the technical goals, and this was keeping an accurate record of the project design iterations. Every concrete design change the team made from start to finish was documented such that the team could

have a better understanding of each subsystem's behavior at any point in the project. This included modifications to existing designs from external sources and any changes made from our original designs for each subsystem. In particular, our team kept track of design issues and updates for each PCB iteration during the project.

A second project management goal was to document the results of our final demonstration. Regardless of which technical goals were ultimately achieved or which design iteration of the project subsystems we used, the results of the system demonstration needed to be well-documented. To best evaluate the performance of the device, reference velocities and ranges were used during testing. For instance, the distance to the end of a hallway was first measured using a different measurement device before measuring the distance with the radar. It was important to keep track of the reference measurements to ensure the radar was operating properly. Documentation of the final demonstration was important because it showed the capability achieved by the system at its last design iteration.

Lastly, our team strived to meet on a regular basis and keep to our project schedule. During Senior Design I, our team met regularly at least twice a week. During Senior Design II, despite conflicting schedules, our team made sure to meet at least once weekly, with additional meetings scheduled between individuals as needed. Our team met with this frequency and recorded what progress each team member made toward their individually assigned goals since the previous meeting. This made it clear whether the team was making sufficient progress towards meeting our deadlines.

2.3 Objectives

In order to achieve our goals, steps had to be taken to design and complete each of the subsystems in the project. Each of the subsystems varied in the amount of effort needed to design and construct it, and the effort generally increased as we aimed to achieve each of the successive goals outlined in the previous section. We will begin with a discussion of the radar module, which had to be completed for the post-processing goals to be achieved.

Our radar module was centered around the MIT Lincoln Laboratory laptop-based radar, the design for which is available in the corresponding MIT OpenCourseWare material. The details of that project will be discussed in further detail in Section 3.1 "Similar Products." There are two subsystems that our team split the components of the radar into: a high-frequency subsystem and a low-frequency subsystem. There was a mixer involved that has a high-frequency input and a low-frequency output, but for the purposes of discussion, the mixer is placed in the high-frequency subsystem.

Dr. Xun Gong, professor at the University of Central Florida and the primary advisor for our project, provided our group with a partially built version of the MIT radar for us to start with. The part of the radar he provided includes all the high-frequency components; they are fully assembled and presumably operational. What was left to be completed was the low-frequency circuits, which are the low-pass filter, gain stage, and modulator.

MIT OpenCourseWare provides schematics for these circuits, but the course is dated and details regarding the design of the circuits is limited. In order to complete the radar, our team needed to update the designs for each circuit and test them to verify proper operation. Once the circuits had been tested, the team designed printed circuit boards for use in the final module prototype. Work regarding completion of the radar module constituted our team's first objective.

The next two objectives were specifically for achieving the real-time processing goals of the project, which were ultimately not achieved. The objectives will be discussed here, though, for documentation of the team's efforts. Our team's second objective was to design an operational USB interface, which would facilitate transfer of information from the radar to a host device. A variety of interfaces could have been used to communicate between the radar module and the host computer, including wireless communication or the audio interface already used in MIT's project design. Our team originally decided that a USB interface would be a fair compromise between feasibility and ease of use, though an audio cable would suffice should a USB interface not be achieved. The input of the USB interface circuit would have been the analog output of the radar module. The output of the interface would have been a digitized version of the radar output, sent through USB2. The interface would have transmitted the digitized signal quickly and with minimal error introduced.

The third objective was to design a functional and easy-to-use API. Again, this was ultimately not achieved, but will be discussed here briefly. The most beneficial characteristic of an API is that it can be aligned with radar signal processing standards. This was not a necessity, but using a standard would have ensured that the functions and architectures used in our code were easily understood by certain end users who wish to slightly modify the functionality of the system. For the purposes of our team's project, the code developed would have been able to extract the necessary information from the radar module signal but also be somewhat adaptable. Certain parts of the final code may have gone unused in our demonstrations, but would've at least been available for later use.

The fourth objective was to design the PCBs for the project. Two things were taken into consideration to design the PCBs. The first was testing. The more components that are placed on a single PCB, the harder it is to troubleshoot issues. The circuitry for the project was therefore broken up into multiple PCBs to facilitate the testing process. The second consideration was the size and shape of the PCBs. Although the overall size of the radar module was largely dictated by the size of the antennas, which were already provided by Dr. Gong, it was still important to ensure the shape of the PCBs made it easy to install on the final system. Additionally, the components to be soldered onto the PCB should be large enough for easy assembly, but not so large as to make the entire PCB footprint unnecessarily large.

The fifth and sixth objectives were to acquire the necessary materials for the project and assemble the prototype. This applied only to the USB interface and radar module. Once the subsystems had been assembled, another phase of testing was required. This was

to verify all the parts were working as they should have prior to the final assembly. Once the radar, USB interface and software had all been independently tested, the final objective was to integrate the system and attempt to reach the project goals through demonstrations.

As expected, the final integration stages did reveal shortcomings and issues with regard to subsystem designs. Our team's approach was to meet the final objective as quickly as possible to leave time for circling back and making modifications to the system, which we were able to do.

2.4 Requirement Specifications

2.4.1 Desired System Qualities

2.4.1.1 Accuracy Requirements

There were certain qualities in a product that guided our requirement specifications. Accuracy was one important quality; our goal of measuring car velocities will be used as an example. If a car comes at 30 meters per second and the radar system reports 10 meters per second as its measurement, the radar is essentially useless. If the system reports 30 meters per second but only after a long delay, the radar is not much use either unless the results are adjusted for the time delay (this is not very useful for real time analysis). If the radar reports 28 meters per second with a very short delay, there is still error present, but the system is suitable for general analysis of the environment. In summary, our system needed to prioritize accurate results, but not so much as to cause excessive strain on the technical design.

The first accuracy requirement specification that was imposed on our system said that the output measurement had to be between plus and minus 10 percent of the actual parameter value; this was later modified to be +/- 3 meters, in light of the fact that close-range measurements of less than 10 meters needn't be as accurate as +/- 10 percent. Verification of this requirement involved taking an accurate external reading of the parameter in question and comparing it to the measured parameter generated by our system. This was fairly straightforward in the case of the ranging goal, for instance, where the distance can be easily measured between the radar module and a stationary object. For velocity error calculation, a calibrated commercial off-the-shelf device with a known error could have been used to measure the velocity of the target object. Alternatively, our team chose to have a "control" team member drive a vehicle and keep track of the velocity using the internal speedometer while other team members used the radar to measure the velocity.

The second accuracy requirement specification to be imposed on our system said that for real-time processing, the output measurement must be generated and displayed by the software no longer than three seconds after the measured parameter occurs in the environment. This means that if a velocity of 5 meters/second appears in the environment, and then immediately disappears, it should be no longer than three

seconds before the system displays 5 meters/second. In actuality, this requirement was somewhat lax, as real-time system outputs often appear nearly instantaneously. For the sake of establishing an absolute maximum lag time for our software and taking into account data transmission complexity in our anticipated subsystem architectures, three seconds was used.

The final accuracy requirement specification had to do with the transmitted frequency. In general, as frequency is increased, accuracy of the radar increases as well. Frequency constraints will be discussed more later on, but for now, know that our team imposed a requirement that stated the system must transmit at no less than 2 GHz for sufficient radar accuracy.

2.4.1.2 Operating Distance Requirement

Maximum operating distance was another system parameter that was established. This is the longest length at which the radar output will remain within the maximum error requirement outlined above. The desired maximum operating distance was largely dependent on the specific application of the radar. Since our radar module was meant to be multi-purpose for the general consumer, it was assumed that the targets were within 50 meters of the user. This meant that at the very least, our radar should be able to sense targets up to 50 meters away. Being able to accurately sense anything further was not necessary but would have been an improvement.

2.4.1.3 System Runtime Requirement

A characteristic similar to maximum operating range was minimum system runtime. The necessary runtime for the system was largely dependent on the application. In general, the system should remain on long enough to allow for sufficient data collection in an environment. If the system loses power soon after powering on, not only would the user have to consistently replace the batteries, but the user would not be able to collect very much successive information before having to put the module down. A minimum total runtime of 30 minutes was the requirement for our project. While this does mean the radar module would not be ideal for long-term, continuous environment surveillance, it would work nicely for measuring environment parameters in short sessions.

Verification that the runtime requirement was somewhat theoretical, since in actuality the runtime is not entirely dependent on the system characteristics. It also depends on the type of batteries that are used. Several batteries with the same voltage may have different capacities, which will then translate into different system runtimes. For the sake of catering to the general consumer, our team chose to use batteries that can be easily acquired in a local hardware shop or general store. The capacities and characteristics of those batteries were used as the standard to gauge the runtime performance of our radar module.

2.4.1.4 Transmitted Power Requirement

How much power the system consumes is closely related to runtime. The more power the system consumes, the shorter the run time will be, regardless of what type of (presumably finite) power supply is used. Additionally, high-powered electrical systems have the tendency to generate excessive heat, which will be discussed further in the Health and Safety section of the paper. The primary element of our system that affects power use is the transmitted power of the radar; the other elements of the system have reasonably low current draw that will not raise a power-consumption concern. Prior knowledge and research showed us that our desired radar accuracy could be achieved by transmitting on the order of 10 milliwatts of power. This was set as the lower threshold for transmitted power. Although lower transmitted power is better for runtime, as will be illustrated in the House of Quality figure, on its own a high transmitted power is actually better, in general, for a radar system. For this reason, a lower threshold for transmitted power was established, and the proper balance had to be found between using a higher power and compromising other elements of the system.

2.4.1.5 Module Size Requirements

Portability was an ideal characteristic for our system. The basis is simple: the end-user should be able to pick up the radar module and point it in different directions. This makes it easier to take multiple measurements in an environment without the hassle of moving a large piece of equipment. Two parameters that affect portability are weight and dimensions. The requirements for these two parameters were set to less than 3 kilograms and less than 0.5 cubic meters, respectively.

2.4.1.6 System Cost Requirement

The final characteristic to be considered was cost. Radar systems are relatively expensive when compared to other systems in electrical engineering due to the high cost of RF signal processing components. Our budget for the project, which was almost entirely dependent on the cost of the hardware, will take into account both hardware costs and each team member's maximum contribution to the project. The requirement for cost therefore stated that in total, the system must cost no more than $800.

2.4.2 Requirements Summary

Table 1 below summarizes the quantitative requirements discussed in the previous section. Note that measurement error is the only requirement with both an upper and a lower bound, denoted this way for clarity. Another way of stating it is that the absolute value of the measurement error must be no greater than ten percent of the actual parameter value.

Table I
FMCW Radar Requirements

FMCW Radar Requirements		
Requirement	Minimum	Maximum
Measurement Error	-10%	+10%
Max Operating Distance	50 meters	---
Runtime	30 minutes	---
Cost	---	$800
Size	---	0.5 cubic meters
Frequency	2 GHz	---
Output (TX) Power	10 milliWatta	---
Software Lag Time	---	3 seconds
Weight	---	3 kilograms

2.4.3 House of Quality

Designing a marketable consumer product involves finding a good balance between conflicting consumer desired qualities. Every desired quantity cannot be maximized, because increasing one will inevitably decrease another. For instance, if the cost of the system is very low, it will inevitably cause the system accuracy to become low as well. High accuracy means purchasing high-quality parts, and high-quality parts are more expensive than low-quality parts. It becomes a balancing act between desired qualities.

The house of quality for our system, shown in Figure 1, shows the relationship between all the desired system qualities and the technical characteristics of the system. On the left side of the figure, each quality is listed with a plus or a minus sign, depending on whether the quality should be as high as possible or as low as possible, respectively. The top of the rectangular portion of the figure shows the technical characteristics of the radar system, and whether they should ideally be as high as possible (indicated with a plus sign) or as low as possible (indicated with a minus sign).

The intersection between a quality and a technical characteristic shows how moving the technical characteristic in the ideal direction would impact the quality parameter. The “roof” of the house of quality shows the interrelationship between the technical characteristics.

Note that some intersection points in the figure are blank. This indicates that there is no relationship between the intersecting characteristics. Technical characteristics with many plus signs in their corresponding intersection points can be easily moved in the desired direction without much impact on other parameters. For our specific project, measurement error and software lag time are two technical characteristics whose intersection points with other parameters are mostly blank squares and plus signs. This means the software lag time and measurement error can both be decreased as desired, and other system parameters will either be benefitted or remain unaffected.

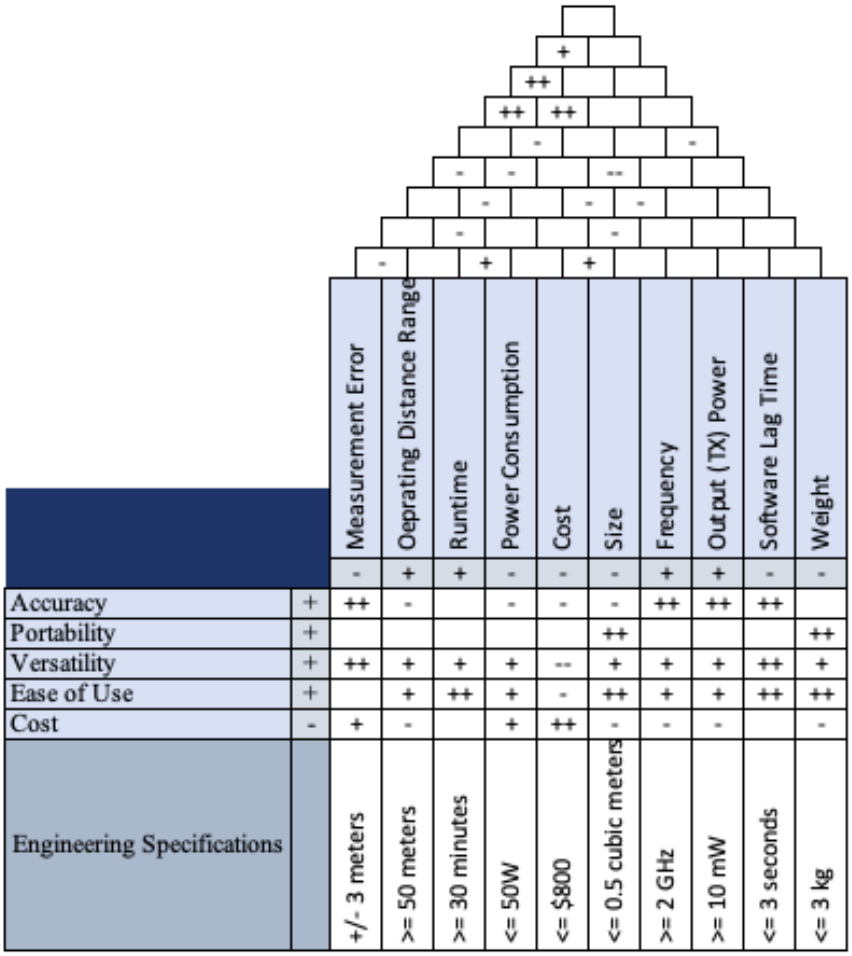


Figure 1: FMCW Radar Module House of Quality

3.0 Project Research

3.1 Radar Background Theory

3.1.1 Radar Transmission Theory

The doppler in our system consists of an oscillator that after some attenuation amplification, gets split in two, where transmitted, the other half is fed into a frequency mixer which performs a multiplication function. The transmitter emits a microwave spherical wavefront, as shown in Figure 3. We could imagine this spherical wavefront propagating from the emitter and reaching a target downrange. Some of the wavefront intersects with the cross-section of the target and is scattered back to the emitter.

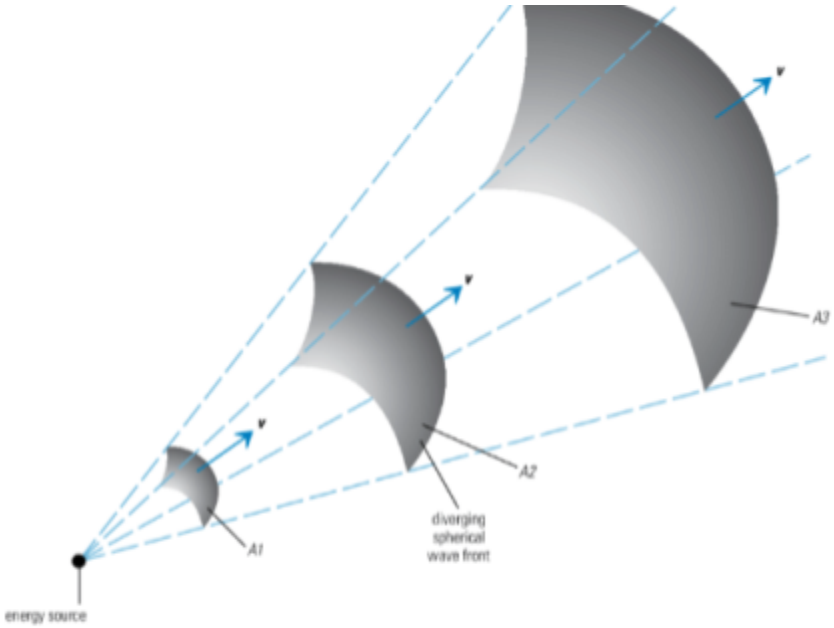


Fig. 3. Spherical wavefront.

In order to reduce the coupling between the transmitter and receiver and avoid deadening the received signal we have separated the two. In conventional radar systems one usually would have only one.

The received scattering is then amplified and fed into the multiplier. The difference comes out of the mixer and is amplified with three op-amps. The three op amps consist of an amplifier and a fourth-order low-pass filter.

The range to the object is calculated by determining the round-trip distance that light would have traveled in that amount of time. Note that signal power drops by the distance to the object raised to the fourth power. This tells us that the farther an object is, the more difficult it is to distinguish the received power pulse from the noise.

Below is the equation for range in a two-way (roundtrip) radar.

$$Range \simeq \frac{P_t G_t G_R \lambda^2}{(4\pi)^3 S_{min}} \quad (1)$$

$$P_t = transmitted\ power$$
$$G_t = transmitted\ antenna\ gain$$
$$G_R = receiver\ antenna\ gain$$
$$\lambda = wavelength\ of\ signal$$

$$S_{min} = \ minimum\ detectable\ signal$$

The gain of antenna is given by

$$G = \frac{4\pi A_e}{\lambda^2} \quad (2)$$

$$A_e = \ equivalent\ area \text{ of aperture}$$

Substituting into Equation (1) results in

$$\text{Range} \simeq \ \left(\frac{P_t \sigma \pi r^2}{2\lambda^2 S_{min}}\right)^{1/4} \quad (3)$$

We can observe based on the above equation that in order to double the range of a range system we would need to increase its power by a factor of 16. We could also increase the frequency by a factor of 4, or double the radius of the aperture. Understanding the technical background of our product lets us have a deeper insight into the design choices and how to improve the product in future iterations.

To minimize range ambiguity we want to ensure the distance to the target is greater than or equal to the speed of light divided by two times the pulse repetition frequency.

$$Distance \ \geq \ \left(\frac{c}{2*(Pulse\ Repetition\ Frequency)}\right) \quad (4)$$

3.1.2 Microwave Theory

There are fundamental differences between traditional circuit and network theory and microwave engineering theory. In the traditional circuit model a circuit is described by how much energy is guided through interconnected components. The sizes of the components do not matter in their function, and the voltage is the same along a transmission line. In network theory the ratio between voltage and current is always a constant. We are able to use Kirchhoff's laws to solve for unknown values in a straight-forward way. The ratio of voltage to current is called impedance. We can model resistors, inductors, and capacitors using impedance. In order to model sinusoidal time variance complex impedance can be used. When signals are traveling through a line, only one mode can propagate.

We can model an infinitely small cross sectional area of a transmission line with the generalized lumped-element model of a transmission line, as shown in Figure 4. This model allows us to calculate characteristic impedance, phase velocity, and both the real and imaginary parts of the propagation constant.

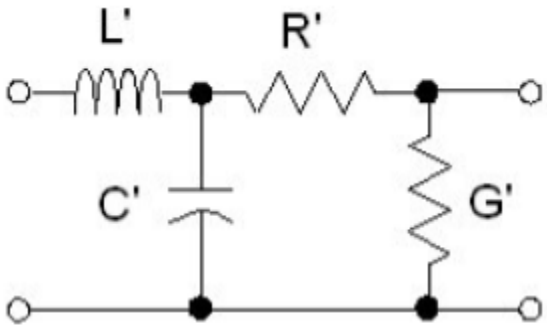


Fig. 4. Generalized lumped-element model.

The relationships between the wavelength, phase velocity, and phase constant are useful to understand. The relationship between wavelength and the phase velocity is given by

$$\beta = \frac{2\pi}{\lambda} \text{ (radians/length)} \tag{5}$$

where $\beta = \omega\sqrt{L'C'} = 2\pi f\sqrt{L'C'}$

The series impedance and shunt admittance are given as

$$Z' = R' + j\omega L' \tag{6}$$

$$Y' = G' + jwC' \tag{7}$$

The propagation constant is given as

$$\gamma = \sqrt{Z'Y'} \tag{8}$$

The characteristic impedance of a transmission line can be found understood using the following equations.

$$Z_0 = \sqrt{\frac{R' + j\omega L'}{G' + jwC'}} \text{ (low-loss)} \tag{9}$$

For lossless transmission lines the following wave equations can be used to derive the phase velocity.

$$-\frac{\partial v(z.t)}{\partial z} = L\frac{\partial i(z.t)}{\partial t} \rightarrow \frac{\partial v^2(z.t)}{\partial z^2} - \frac{1}{v_p^2}\frac{\partial v^2(z.t)}{\partial t^2} = 0 \tag{10}$$

$$-\frac{\partial i(z.t)}{\partial z} = C\frac{\partial v(z.t)}{\partial t} \rightarrow \frac{\partial i^2(z.t)}{\partial z^2} - \frac{1}{v_p^2}\frac{\partial i^2(z.t)}{\partial t^2} = 0 \quad (11)$$

This leads to

$$v_p = \frac{1}{\sqrt{L'C'}} \quad (12)$$

The general solution for a lossless transmission line is given as

$$v(z,t) = v^+(t - \frac{z}{v_p}) + v^-(t + \frac{z}{v_p}) \quad (13)$$

$$i(z,t) = i^+(t - \frac{z}{v_p}) + i^-(t + \frac{z}{v_p}) = \frac{v^+(t-\frac{z}{v_p}) - v^-(t-\frac{z}{v_p})}{Z_0} \quad (14)$$

$$Z_0 = \sqrt{\frac{L}{C}} \text{ (characteristic impedance)} \quad (15)$$

For time harmonic transmission lines (illustrated in Figure 5)

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z) \rightarrow \frac{dV^2(z)}{dz^2} - (R + j\omega L)(G + j\omega C)V(z) = 0 \quad (16)$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z) \rightarrow \frac{dI^2(z)}{dz^2} - (R + j\omega L)(G + j\omega C)I(z) = 0 \quad (17)$$

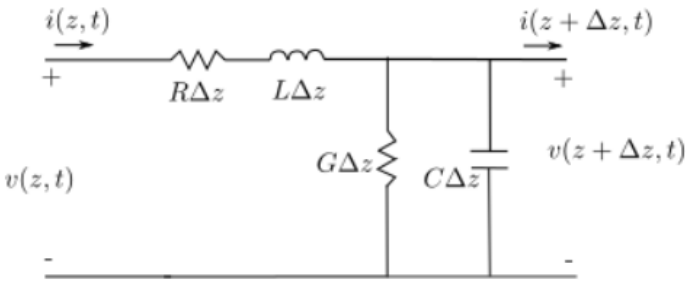


Figure 5: Time Harmonic Transmission Line.

$$Z_0 = \sqrt{\frac{L'}{C'}} \quad (18)$$

The standing wave ratio measures the impedance matching of the loads to the characteristic impedance of the transmission line. Standing waves will be created when the impedance is mismatched. The standing wave ratio is given by

$$SWR = \frac{V_{max}}{V_{min}} = \frac{1+|\Gamma|}{1-|\Gamma|} \quad (19)$$

Voltage on a transmission line is described by

$$V(z) = V_0^+(e^{-j\beta z} + \frac{V_0^-}{V_0^+}) = V_0^+(e^{-j\beta z} + \Gamma_L e^{+j\beta z}) \quad (20)$$

$$I(z) = \frac{V_0^+}{Z_0}(e^{-j\beta z} - \frac{V_0^-}{V_0^+}e^{+j\beta z}) = V_0^+(e^{-j\beta z} + \Gamma_L e^{+j\beta z}) \quad (21)$$

For reflection, a transmission line terminated in a short or open reflects all power back to the source. When considering input impedance (illustrated in Figure 6),

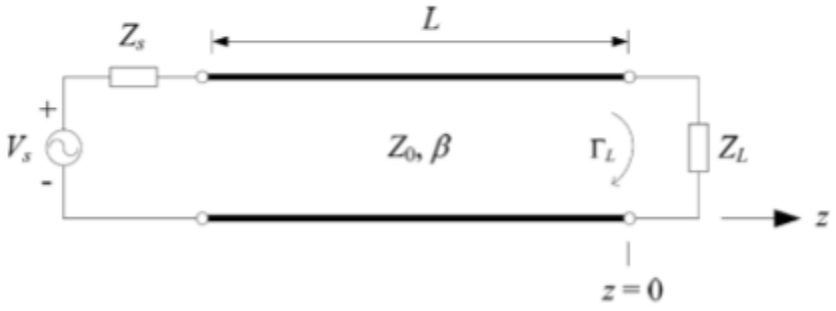


Fig. 6. Input impedance.

$$Z_{in} = \frac{V(z)}{I(z)} = Z_0\frac{1+\Gamma_L e^{+j2\beta z}}{1-\Gamma_L e^{+j2\beta z}} \quad (22)$$

$$Z_{in} = \frac{V(z)}{I(z)} = Z_0\frac{1+\Gamma_L(l)}{1-\Gamma_L(l)} \quad (23)$$

This gives,

$$\Gamma_L(l) = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \quad (24)$$

Note that L' can be thought about as the tendency of a transmission line to oppose a change in current. Conversely, C' can be thought about as the tendency for a transmission line to oppose a change in voltage. The phase velocity can also be found if we know L' and C'.

$$v_p = \frac{1}{\sqrt{L'C'}} \quad (25)$$

3.1.3 Antennas and Electromagnetics

An antenna can convert a signal voltage on a transmission line into a transmitted electromagnetic wave. A time varying signal applied to the transmit antenna induces an electrical current on the antenna which in turn produces electromagnetic radiation. Antennas are dielectric or metal structures that are specifically designed or chosen to provide an efficient launch of electromagnetic waves into space. Physically, we can conceptualize an antenna as providing a sea of free electrons which can be influenced by external forces and that offer zero resistance to movement.

We can derive from Maxwell's equations that electromagnetic radiation occurs when electric charge accelerates. We cannot directly see electromagnetic waves. In order to prove they exist, we can formulate Maxwell's equations as a wave equation in the form

$$\nabla^2\Psi - \frac{1}{v^2}\frac{\partial^2\Psi}{\partial t^2} = g \tag{26}$$

where Ψ is the field quantity. Next, we take the curl of Faraday's law to obtain the new vector field as

$$\nabla x \nabla x E = -\nabla x \frac{\partial B}{\partial t} = \frac{\partial}{\partial t}(\nabla x B) \tag{27}$$

$$\nabla x \nabla x E = -\nabla x \frac{\partial B}{\partial t} = -\epsilon\mu\frac{\partial^2 E}{\partial t^2} - \mu\frac{\partial J}{\partial t} \tag{28}$$

The right hand side of the above equation yields some important observations. In free space $J = 0$ and $\epsilon = \epsilon_0$. Therefore

$$v = c = \frac{1}{\sqrt{\epsilon_o\mu_0}} \tag{29}$$

As the electromagnetic wave traveling at the speed of light reflects off of an object, the reflected energy illuminates the receiving antenna which in turn induces a signal that travels through a coaxial cable. For an isotropic antenna, the electromagnetic wave propagates spherically from the excitation point. A directional antenna (which is the type our system uses) produces a gain radiation pattern as shown in Figure 7.

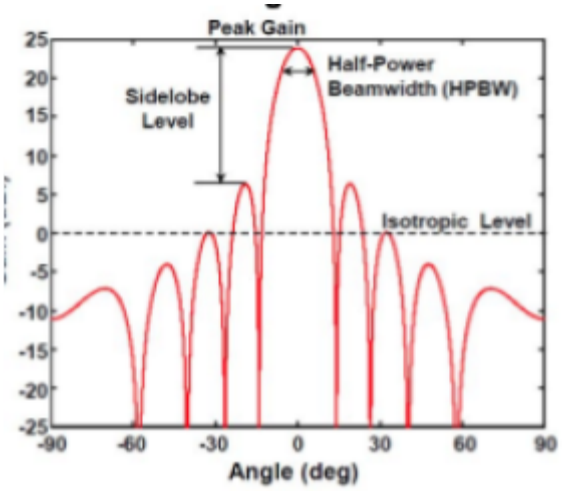


Fig. 7. Gain pattern for circular aperture.

Note that a directional antenna has a main beam that is pointed in a direction and sidelobes that radiate away from the beam. The electromagnetic waves are not sent in a perfectly circular beam. As the antenna diameter increases, the bandwidth gets narrower and the main beam's gain increases. The gain G of an aperture is given by the expression.

$$G = \frac{4\pi A_e}{\lambda^2} \tag{30}$$

The effective isotropic radiated power is a function of the transmitted power and the gain of the transmitting antenna.

When considering calculating the gain from measured power coupling between two identical antennas we can utilize the following relation.

$$G_{dBi} = \frac{1}{2}\left[10log\left(\frac{P_r(\theta,\varphi)}{P_t}\right) + 20log\left(\frac{4\pi r}{\lambda}\right)\right. \tag{31}$$

The voltage reflection coefficient tells us how much of the signal is reflected by the antenna. Note that for a well-designed antenna the magnitude of the voltage reflection coefficient should have a low value. The power transmission coefficient tells us how much power is transmitted relative to the incident power.

If a wire is placed next to a metal wall, the antenna radiation will have a phase shift of 180 degrees. If we want our radiated energy to efficiently be directed in a direction, we would place our antenna a quarter of a wavelength away from the metal wall, causing the phase shift to now be 360 degrees (see Figure 8). In a circular waveguide TE_{11} mode will be used.

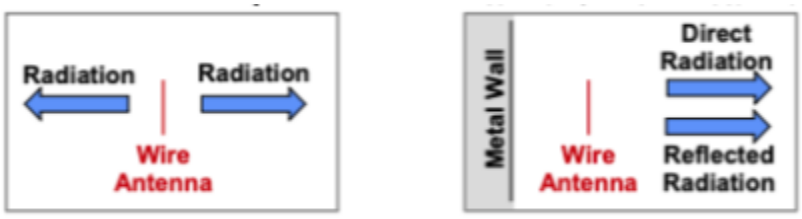


Fig. 8. Wire antenna near a PEC barrier.

In summary we have described some of the fundamental characteristics of antennas. We have also described the design of a circular waveguide antenna that can be used as a transducer, as shown in Figure 9.

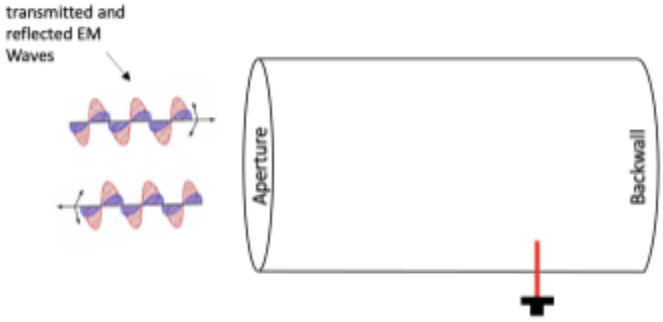


Fig. 9. Diagram of a “cantenna” antenna.

Here are the dimensions of the coffee cans that we have used:

- Metal Can Length = 5.25”
- Metal Can Diameter = 3.9”
- Monopole Wire Length = 1.2”
- Spacing from monopole wire to back wall = 1.8”

An analog to digital converter will need to be implemented to digitize the phase differences for further signal processing.

The modulator will be able to select what mode the radar is in. The square wave mode will select velocity mode for the radar. The square wave is sent into the VCO. This creates a tone signal, this is then sent to the transmitter and bounced off an object moving at a certain velocity. This reflected signal will come back into the receiver antenna with a frequency shift. This signal is then mixed with the original transmitted signal. The lowpass filter selects the difference frequency. This is then going to be sent to the laptop or microcontroller where it will undergo a fast fourier transform. Our note that our FMCW radar is an active system, being powered by 9V batteries.

3.2 Similar Products

During our market search we found the following relevant products available.

3.2.1 MIT Small Radar System

Our initial product design used the MIT Small Radar System as a reference point for the initial design of our product. The setup uses a radar module to interface with a laptop via a two-channel audio cable, which has a 3.5mm audio jack on the laptop side. Key characteristics of the radar module itself are its FMCW architecture, coffee-can receive and transmit antennas, and S-band range of operation. Elements of the MIT design that will remain largely similar in our design include the active gain stage, active low pass filter, and applications (doppler and ranging).

3.2.2 Police Radar Systems

Police radar systems are devices used to track the velocity of vehicles. Though such devices are available on the market, they are typically quite costly, ranging from $500 to $2000. Our system will be able to track velocity at a much lower cost. This will allow our product to reach an untapped market for consumers who wish to have the functionality of a velocity radar system without the steep cost. One difference between our system and police radar systems is that police radars typically operate in several frequency ranges including the X band(≈10.5GHz), K band(≈24GHz), and Ka band(≈33-36GHz) [18]. The primary reason for using these bands would be due to the fact that for higher frequencies, smaller antennas can be used, therefore maximizing space efficiency. To facilitate testing of our project, we will operate in a lower band where design components are a bit easier to obtain. Additionally, specific bands require licensing to use, and this must be taken into consideration for the purposes of our project demonstration.

3.2.3 Automatic Doors

Automatic doors operate by using a sensing system to send signals to a control system that will open the door for oneself. These sensing systems come in many different forms, but at a fundamental level sensing systems will be detecting disturbances within an electromagnetic field.

Our system will encode the received information in a digital format. This allows the potential for digital signal processing and integration with other systems. In theory one will be able to use our system to interface to a control system such as an automatic door. Automatic door installation on the market will run one on the order of thousands. Our system would allow savvy consumers the ability to use the data from our radar for various sensing and controls applications.

3.3 Relevant Technologies

3.3.1 Remote Sensing

When discussing technologies such as remote sensing, electromagnetic energy travels in the form of waves through free-space. The wavelengths can vary from the order of millimeters to kilometers, as illustrated in Figure 10. We are all familiar with visible light, which sits somewhere towards the middle of the electromagnetic spectrum. Visible light only covers a very small portion of the electromagnetic spectrum. We need instrumentation to observe any other forms of electromagnetic energy.

Remote sensing is the process of measuring the reflected and emitted electromagnetic energy at a distance; without contact. These measurements can be used to detect and monitor the physical characteristics of an object of interest. The required spectral, radiometric, and spectral resolutions will vary based on the desired application.

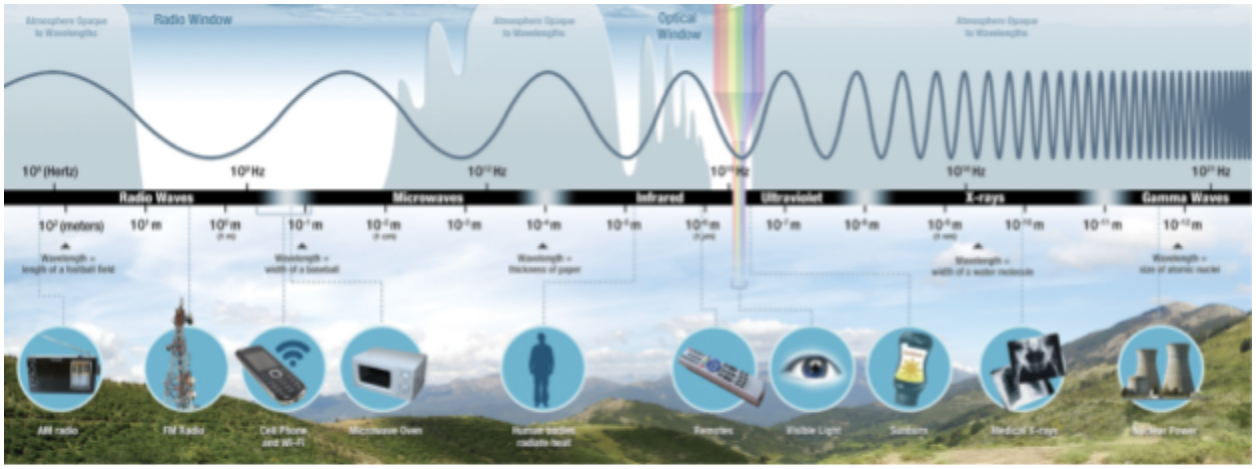


Fig. 10. Diagram of electromagnetic spectrum. Credit: NASA Science.

3.3.2 Pulse-Doppler Signal Processing

Our system will be able to determine the range of an object using Pulse-Doppler Signal Processing. This process utilizes the Doppler effect which describes the change in frequency of a wave in relation to an observer who is moving relative to the wave source. We frequently hear this phenomenon in our daily lives when we hear a car horn or police siren change pitch as it drives away or towards us.

It is important to recognize that we are not directly measuring the frequency shift, but are measuring the phase shift between pulses.

As the object that is reflecting the electromagnetic waves moves in position, the returned signal carries a phase difference relative to the previous pulse. This principle allows us to translate the information to electrical signals and ultimately compute range.

3.3.3 Transceiver Architectures

A basic radio system at a fundamental level, has a transmitter to propagate the electromagnetic wave carrying the signal and also a receiver to obtain these waves being propagated within the air. The transmitter will generally have a modulator that will combine a low frequency signal with the high frequency signal, using a mixer. The receiver will serve the opposite function of demodulating the signal and obtaining the signal at hand and then provide the system information sent over from a transmitter. There are 2 popular types of radio systems, which are the following: the Time-Domain Duplexing (TDD) and the Frequency-Domain Duplexing (FDD).

3.3.3.1 Time-Domain Duplexing Model

The TDD (shown in Figure 11) is a progressing area in the current area of 5G communication since it provides better quality signals for this range. The system on chip, is based on complementary mosfet technology (CMOS) which includes the modem and transceiver of the overall system. The RF frontend where we primarily work with high frequency signals is at a very base level composed of the power amplifier (PA), switch (III-V semiconductors, MEMS, etc.), and filter. This system is convenient to implement since we are able to use a switch to swap from transmit or receive mode.

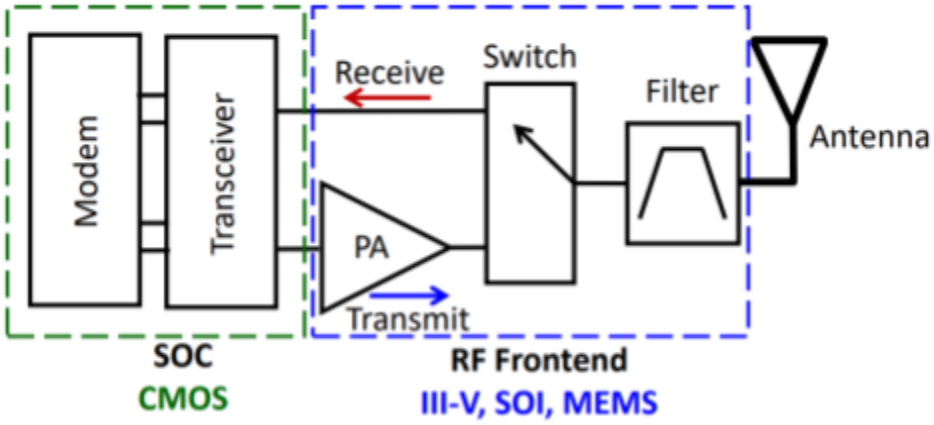


Fig. 11. The time-domain duplexing model.

3.3.3.2 Frequency-Domain Duplexing Model

The Frequency-Domain Duplexing (FDD) shown in Figure 12 has both transmission and receiving operating at the same time. It similarly has the CMOS technology for the SOC and the III-V compounds & MEMS for the RF frontend. 4G-LTE bands generally depend on this system to operate.

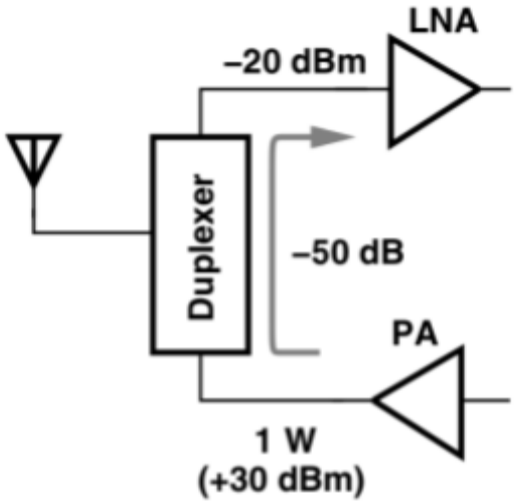
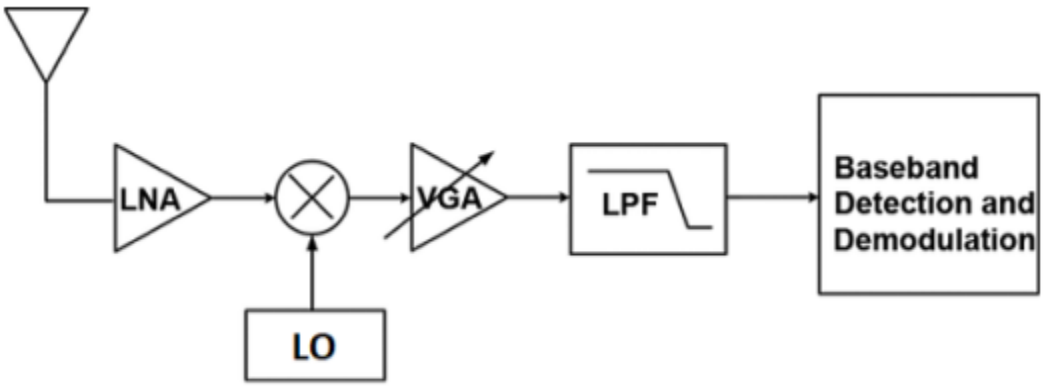


Fig. 12. The frequency-domain duplexing model.

Above we discussed a very high level understanding of the 2 techniques of the transceiver architectures. If we go further in detail, the system becomes increasingly complicated. The receiver system and transmit system have their own block diagrams, and the receiver is generally much more complicated than the transmit. This would because the receiver must deal with interferers, noise, non-linearity, dynamic range, etc. Generally, there are 3 different receiver architectures that we would consider. These are the Direct Conversion (RF to Low Frequency), Heterodyne (RF to IF [Intermediate Frequency] to Low Frequency), and the Super Heterodyne (RF to IF2 to IF1 to Low Frequency).

3.3.3.3 Direct Conversion Receiver

A direct conversion receiver, shown in Figure 13, demodulates the radio frequency signal using synchronous detection with a local oscillator that has a frequency close to the carrier frequency of the signal. This simple system is good, for overall simplicity of circuit design. Though the issue using this technique would be dynamic range. This technique was initially useless in its initial conception due to errors you may receive in the signal. Modern technology has allowed this to be considered again because of corrections that can be made with the aid of software.



3.3.3.4 Heterodyne Receiver

A heterodyne receiver, shown in Figure 14, makes the use of an intermediary frequency signal and then into the low frequency territory. We are able to make use of this by using one mixer to bring a modulated RF signal to the modulated IF signal, which when demodulated brings us to baseband signal. The main reason we would want to use the intermediate frequency is to improve the frequency selectivity. Since radio frequency is really used in some form of communication circuits, we generally would like to easily pick out the desired signals and this would require filtering. The better the frequency selectivity, the better it is to pick out our desired signal. Finally, there is the super heterodyne receiver which makes use of 2 different intermediate frequency conversions. This would therefore cause us to use 2 mixers in the system actually. The primary reason we would want to use a system like this is to better tune the frequency selectivity than with just 1 IF conversion. We would first go from RF to the first IF which is “high” then to the second IF which is “low” and then finally to the low frequency signal.

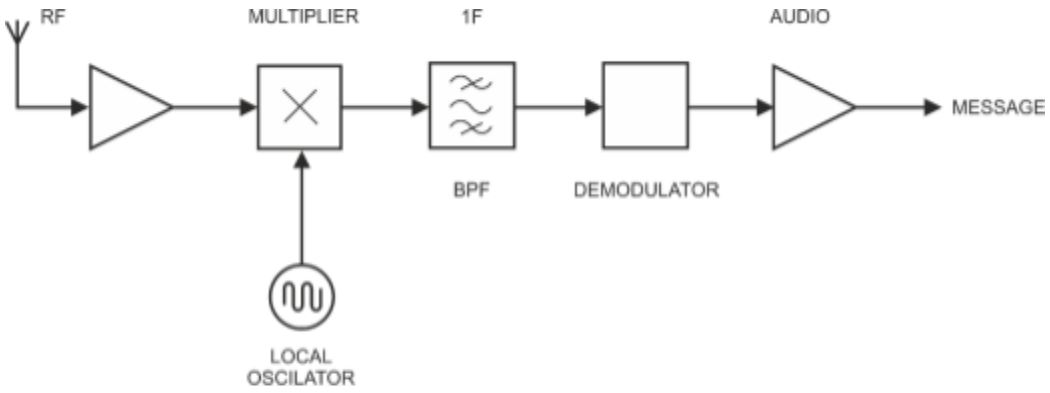


Fig. 14. A heterodyne receiver

3.4 Strategic Components and Part Selections

In order to strategically select our components and part selections, it is important to have some understanding of transmission line theory, as at high frequencies circuits behave much differently than at low-frequencies as seen in linear circuits theory.

Also, in order to properly understand the operation of the radar, it is important to make sure we are informed of the relevant theory that would help us visualize how the various components are working together in order to make the system function.

3.4.1 RF Signal Processing Components

Our RF signal processing components were chosen to meet the following parameters.

- ➢ Frequency = 2.4Hz
- ➢ Bandwidth = 80MHz

- ➢ Antenna Isolation = 50dB
- ➢ DC Power < 1W
- ➢ RF Power < 1W (EIRP)

Some realization constraints were inherent in our design. We wanted the system to be able to use off the shelf parts, use connectorized components, and run on 9V batteries. On the transmitted side we needed a modulated source, amplification, distribution, and an antenna for radiation. On the receiver end we needed an antenna to receive aperture, amplification, and a demodulator.

The transmitting RF component chain is made up of a cascaded two-port network model that consists of a VCO, attenuator, amplifier, splitter, and finally transmitting antenna. The receive chain consists of the receiving antenna, amplifier, and finally the mixer.

The receiving and transmitting antennas are dubbed as “cantennas” due to the fact that cans were used as the circularly polarized waveguide antennas. These antennas are surprisingly highly efficient and suit our purposes very well. In order to understand the RF and antenna subsystem, it is worthwhile to describe some of the fundamental characteristics of antennas. We want to develop a stronger understanding of gain radiation patterns, power density, beamwidth, reflection coefficient, transmission coefficient, antennas arrays, measurements. We will use this understanding to follow the design, fabrication, and testing of an antenna that can be used as a transducer.

3.4.2 RF Design Description

The RF section of our hardware design will consist of a voltage controlled oscillator that is fed into an attenuator the signal is then amplified and sent through a beam splitter. Half of the signal will be transmitted, and the other half will be sent to the mixer. Once the signal is received the received signal will be amplified and then multiplied with the reference signal that was sent into the mixer. The signal is then sent through a gain stage and then low-passed to prevent aliasing. This signal will be sent for further signal processing. This architecture is illustrated in Figure 15.

The system will be powered with a 9V battery pack, producing +9V and +18V. This powers the RF components and provides a reference voltage for the analog circuits The +5V will power analog circuits including the modulator, gain stage, and fourth order low pass filter.

Our next steps will include building the system on a breadboard and starting the testing phase.

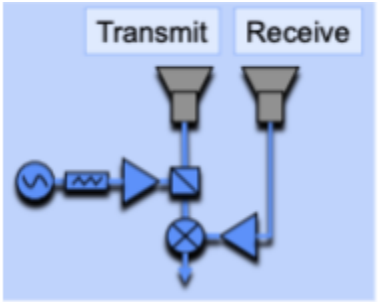


Fig. 15. RF hardware setup.

We will be using the ZX95-2536C+ Voltage Controlled Oscillator, the ZX60-272LN-S+ Low Noise Amplifier, the ZX10-2-42+ 0.1dB insertion loss splitter, and the ZX05-43MH-S+ Mixer.

3.4.3 Modulator

The modulator is what will be driving our transmitted signal. We will use an integrated chip that would be able to produce various waveforms such as ramp, sine, and square. For the purposes of range and velocity sensing we will be using a ramp waveform. Our modulator would modulate oscillator 1 yielding a voltage that is proportional to the transmit frequency. The modulator also provides a syncing function.

The Vtune voltage in the modulator will be proportional to the transmit frequency. The linear ramping of the voltage of the modulator will cause the oscillator to produce a linear FM chirp that is used for transmitting and receiving. The ramp time will be approximately 20ms with a triangular wave period of 40ms. The magnitude of the ramp will modulate the desired transmitted bandwidth.

For the high frequency modulation, we have used a ramp generator to modulate the low frequency information. The XR-2206 is a monolithic function generator which we will use to create our modulating signal in the low frequency range. This component is capable of creating high quality sine, square, triangle, ramp, and pulse signals that have high stability and accuracy. This specific application we would like the XR-2206 to produce a ramp signal, which is popular to use in communication systems. Ramp generators are very popular to use since they provide a quick response and provide the capability to change the start-up & return flow time. The “Sync Pulse Inhibit” is a feature of the circuit since we would like to have a functionality that allows the converter to be turned off and on without having the cycle power. This would help up therefore, save power, reducing inrush current, help prevent input impedance problems and delay the converter turning on before the voltage stabilizes.The frequency space portion of the ramp generator is meant to help us adjust the frequency range we would like to use on the circuit based upon what range we would like to create the ramp at and will be manually done here with a potentiometer. The chirp rate adjust part is what the name implies, adjusts the rate of the chirp seen on the low frequency end. A chirp is generally defined as a signal where the frequency either increases or decreases over time. This specific part of a circuit is common to sonar, radar and laser systems since they are generally sending signals out to be transmitted and received. We also see the use of decoupling by the XR-2206 which is a common component to put near any integrated

circuit since it protects the IC from any instantaneous changes in voltage and filters out unwanted noise that interferes with the IC outside of the system.

3.4.4 Mixer

Mixers are a popular IC to use in RF communication systems. Applications of interest include military radar, cellular base stations, etc. A RF mixer can be a 3-port passive or active device that is integrated in the modulator or demodulator. The ideal goal of the mixer is to change the frequency of the electromagnetic signal, preserving the signal as much as possible (phase and amplitude). As we have discussed earlier, a mixer is a fundamental part for the heterodyne receiver models that converts RF signals to IF.

There are 2 primary conversions that the mixer is used for, downconversion and upconversion (see Figure 16). Downconversion is best described as the frequency conversion process where a radio frequency signal is mixed with the frequency coming from a local oscillator to receive the intermediate frequency to better obtain the signal integrity of the system. This process is typically done when we are interested in demodulating the desired signal at hand. Up-conversion is the reciprocal process where you combine the IF signal with the signal from the local oscillator in the frequency domain and convert it to an RF signal.

Passive mixers generally are more popular to use since they are simple in design, have a relatively large bandwidth and have good intermodulation distortion performance. Active mixers are really only used in RFIC design. Generally, active mixers provide conversion gain, good isolation between ports and do not need as much power to drive the local oscillator. They are easily able to be integrated with signal processing circuits & are not as sensitive to load matching.

Mixer parameters to be considered are conversion loss/gain, 3rd order intercept, spurious behavior, isolation, noise figure, and dynamic range. We consider conversion loss/gain to measure the active gain or loss in a mixer. This is defined as the relationship of the IF output power to the RF input power. Conversion loss is a very important parameter for passive mixers. 3rd order intercept is the RF input power where the unwanted intermodulation signals equal to the desired IF output power. Spurious behavior is seen as external signals that create interference in the IF range. Isolation looks into the amount of power leaked from one port to another. Noise figure is a characteristic where we see how much noise (or undesired random signal) is seen from the input to the output of the mixer. Dynamic range is the power range which the mixer operates ideally.

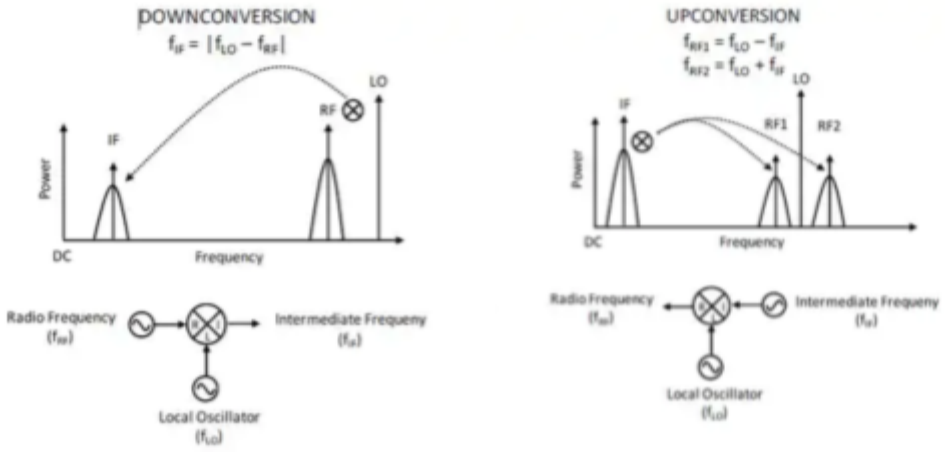


Figure 16: (Left) Down Conversion Using a Mixer;
(Right) Up Conversion Using a Mixer

In order to choose a mixer for our project, there are a few specifications that must be established. The first is the operating frequency of the mixer. Since there are three ports on a mixer, there are three frequency specifications that should be established (typically in terms of ranges). Our mixer needs to be able to handle an RF port frequency of our radar's receive signal, which may be anywhere between 2 GHz and 2.5 GHz. It is entirely dependent on the transmit frequency the team decides on. A wider range is ideal, but the primary goal is a lower operating threshold of at least 2 GHz.

Next, the IF port frequency must be established. We wish to convert the RF signal down to the order of 10 kHz. This means our mixer must be capable of outputting this frequency on the IF port. Consequently, the mixer's LO port must be able to take an input frequency nearly identical to that of the RF port for the differential to be on the order of only 10 kHz. Another important parameter is the required power of the LO port. Mixers often have specified minimum power levels at the LO port for the mixer to operate. If this power level is excessively high, it may strain the power source of the system. A lower LO power level is generally more convenient for small-scale applications such as our project. Additional considerations when choosing a mixer is the versatility of the module, which typically refers to whether the module can work both as an upconverter and a downconverter, and the conversion loss, which should remain as low as possible.

We have decided to use the mixer suggested by the MIT OpenCourseWare course, which is the ZX05-43MH-S+ frequency mixer by MiniCircuits. Its LO and RF port frequency range is 824 MHz to 4200 MHz, which covers the 2000 MHz to 2500 MHz range needed. Its IF port ranges between DC (zero frequency) and 1500 MHz, which is more than enough for our purposes. The LO signal power is +13 dBm, which is a bit high, but ultimately this will work out nicely considering the power levels already being generated by our circuit (as will be seen in the hardware design portion of the paper).

The ZX05-43MH-S+ also has a 6.1 dB typical conversion loss, which is acceptable, and very good port isolation. All around it is a great choice for our frequency mixer.

3.4.5 Power Amplifier

An RF power amplifier is best defined as an electronic amplifier that is designed to take a low power RF signal and boost it up to a high power RF signal. Power amplifiers are known to drive the antenna of a transmitter generally. Important parameters for the design of a power amplifier are typically: gain, power output, bandwidth, power efficient, linearity, input/output impedance matching and heat.

Power amplifiers are the most power consumption heavy components in a RF transceiver and provide the most difficult design challenges within the system. Basic power amplifiers include Class A, Class B, Class C, as shown in Figure 17.

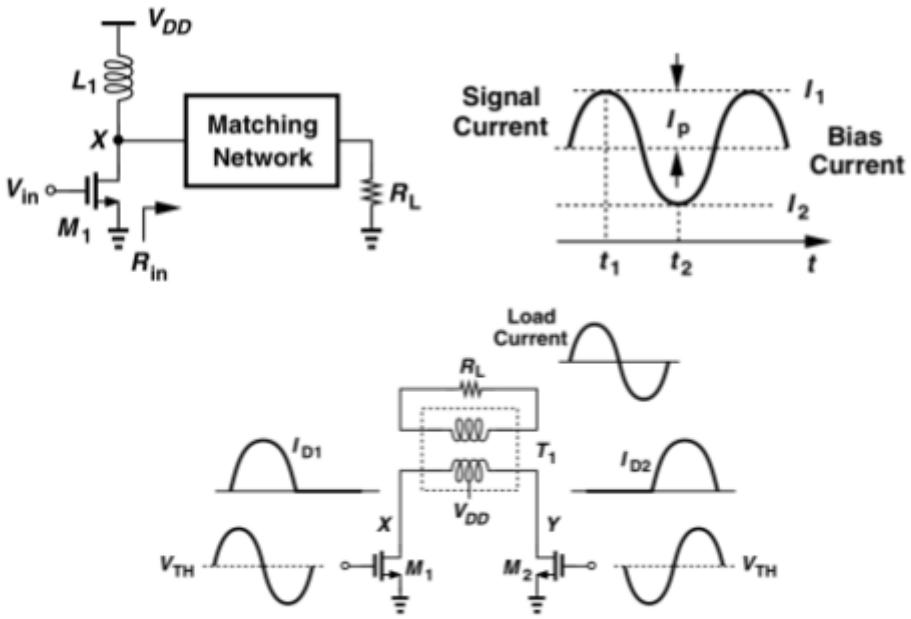


Fig. 17. Top left: Class A power amplifier. Top right: Class B power amplifier. Bottom: Class C power amplifier

Power amplifiers are often placed just before a radar's transmit antenna to give the signal a final boost, and that is the use of the power amplifier in our design. Like many RF signal processing components, the most important parameter of a power amplifier is its frequency range. In our project, we need to amplify the outgoing signal at its radio frequency, which at a minimum will be 2 GHz as previously mentioned. Anywhere in the 2 GHz to 2.5 GHz range would be ideal. The second most important parameter is the

amplification factor of the power amplifier, which is expressed in decibels. The MIT reference documents have suggested that the required amplification is at least 10 dB. Not only must the amplifier have the desired gain, but it must also have the ability to actually output the desired power level. A power amplifier with 10 dB of gain may not necessarily be able to output the expected 20 dBm of power from a 10 dBm input. It is important to determine the necessary output power before selecting a component.

We will use the MIT suggested MiniCircuits low noise amplifier ZX60-272LN-S+. This device has an operating frequency of between 2300 MHz and 2700 MHz, and an average gain of 14 dB, which is plenty for our purposes. One important characteristic is that this is a low noise amplifier, which helps to set a low noise factor for the entire system. This is better than a typical power amplifier, which is designed primarily for its gain characteristics and tends to have poorer noise characteristics. Though this component is called a low noise amplifier, it is functioning as a power amplifier in terms of where it is placed in the radar system.

3.4.6 Oscillator

Oscillators are a fundamental part of the RF transceiver architecture. They are extensively used in both the transmit and receive paths of the system. An oscillator used in a RF transceiver must satisfy 2 primary sets of requirements: system specifications and interface specifications. System specifications relate to the frequency of operation and the signal integrity of the output. Interface specifications relate to the drive of the oscillator or the output swing. Figure 18 shows three different oscillator topologies.

RF oscillators should ideally be designed such that the frequency range can be tuned across a set range. The two sets of criteria to fit the frequency range would be, the system specification of the oscillator needed to go into the mixer and second would be an additional margin to cover process and temperature variations and errors due to modeling inaccuracies. Output voltage swing is a strong consideration as well for oscillators since they must be able to produce sufficient swings on the output to guarantee the switching of transistors for the consecutive stage. A buffer could be used to amplify/drive to drive the stages. Driving is also an important feature for oscillators as well since we would need them to be able to drive a large load capacitance. Capacitive loading is more serious in transmitters, since the input capacitance of a power amplifier can propagate to a local oscillator of upconversion mixers.

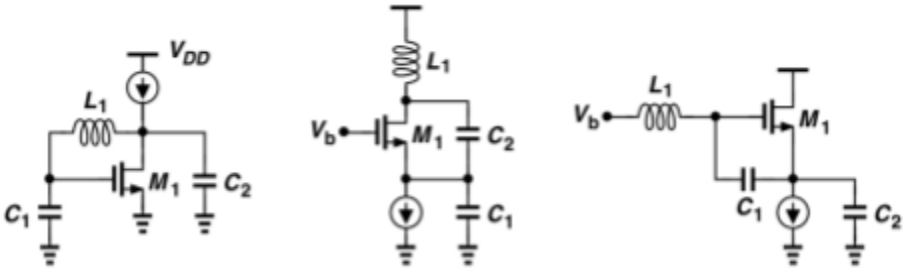


Fig. 18. Topology of 3 Different 3-Point Oscillators

Regarding the basic principles of an oscillator, an oscillator generates a periodic output. This creates a necessity for the circuit to have a system in place that allows its own noise to grow and then become a periodic signal. From the controls system point of view, an oscillator can be viewed as a system that is a “poorly designed” negative feedback amplifier. Baurkhausen’s criteria states that the following condition must be satisfied to ensure stability of the oscillator:

$$|H(s = j\omega_1)| = 1$$
$$\angle H(s = j\omega_1) = 180^\circ$$

The oscillator in our circuit may be the most important component in the radar module. Since it generates the transmitted signal, it is crucial that the correct component be selected. The frequency range must, of course, contain the desired transmit frequencies. The oscillator should also be able to output voltages across the desired range. The harmonics created by the oscillator should be kept to a minimum, as well as the DC operating power. Our team has decided to use the MIT recommended part, MiniCircuit’s ZX95-2536C+. This component has a frequency range of 2315 MHz to 2536 MHz, which meets the primary requirement of being higher than 2 GHz. However, the operating bandwidth of this device is the narrowest of all the RF signal processing components at only 221 MHz. This imposes a restriction on what frequency bands can be chosen for the radar’s operation. Though this component will suffice for project development, this would be an excellent area for the project to be improved in. Increased frequency range is generally a positive when it comes to radar modules.

3.4.7 Low Noise Amplifiers

A low noise amplifier (LNA), is an RF amplifier that is designed to amplify a low power signal without degrading the signal-to-noise ratio. In an ideal since it is what it should do, but it will add noise to the signal due to the noise figure of the integrated circuit itself. An LNA generally adds about 2dB or 3dB to the signal in noise. Gain is another critical parameter for the low noise amplifier since it must be large enough to minimize the noise of the following stages. This becomes a specific issue in downconversion mixers. The choice of this gain largely depends on a compromise between noise figure and then the receiver linearity. Common topologies for an LNA include those shown in Table 2.

The most commonly used topology is the common-source stage with cascode, inductive load and inductive degeneration. Table 2 and Figure 19 show some common topologies for a low noise amplifier.

Table II
LNA Topologies

Common–Source Stage with	Common–Gate Stage with	Broadband Topologies
▪ Inductive Load ▪ Resistive Feedback ▪ Cascode, Inductive Load, Inductive Degeneration	▪ Inductive Load ▪ Feedback ▪ Feedforward ▪ Cascode and Inductive Load	▪ Noise–Cancelling LNAs ▪ Reactance–Cancelling LNAs

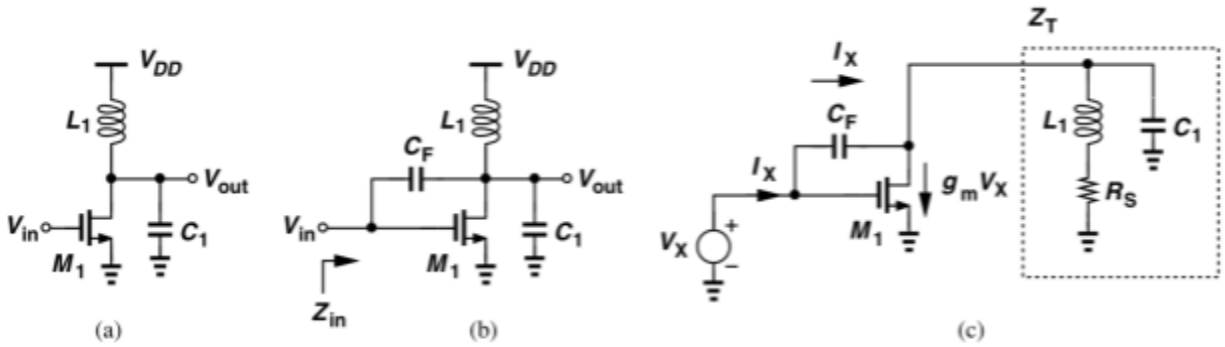


Fig. 19. LNA Topologies

There is a second amplification that often occurs in a radar system, and that is after the signal has been received. After traveling a distance, hitting targets and losing power upon reflection, the signal that was originally transmitted will have lost nearly all of its power by the time it arrives back at the receive antenna. Often there is just enough power to detect the most important characteristics of the signal. In order for the signal to actually be processed and analyzed, it needs to be amplified back up to a more detectable level. This is the purpose of placing a low noise amplifier directly after, or nearly directly after, the receive antenna of a radar. The purpose of using a low noise amplifier as opposed to a power amplifier is that at this point in the system, the focus is no longer on boosting the signal high enough to get the desired range or accuracy. The focus is creating a large but clean signal for proper analysis. Low noise amplifiers are ideal because they minimize the noise passed onto subsequent system components. For our system, will we use a second ZX60-272LN-S+ amplifier as our low noise amplifier.

3.4.8 Analog-to-Digital Converters

The received analog RF signal must be converted to a digital representation in order to extract meaningful information from the signal. To achieve this an analog-to-digital converter must be utilized, which samples the signal and converts the voltage of the sample to a sequence of bits to be interpreted by the microcontroller and subsequently the host device. Key properties to be considered when choosing an analog-to-digital converter are the following: its full scale value (the maximum signal amplitude that the device can measure), its bit resolution (the number of bits used to represent the value in binary), and its sampling frequency (the rate at which samples are acquired). These properties may be visualized in Figure 20 below, which may have a full scale value of 7, a bit resolution of 3, and a sampling frequency of 1 Hz. In this case, the minimum representable value by the analog-to-digital converter would be $7V \,/\, (2^3 - 1) \;=\; 1V$.

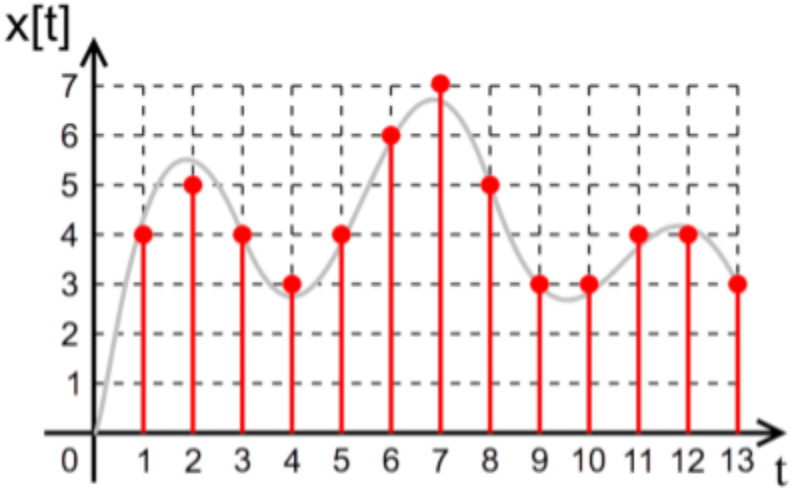


Fig. 20. The discretization of a time domain signal at 1 second intervals.

The analog to digital converter in our system will be used to turn the analog receive radar signal into a signal we can analyze in the host computer. The primary concern when it comes to converting analog signals to digital is having a sufficient sampling rate. If the sampling rate is too low, the signal will not be accurately represented in the digital domain. As a general rule, the sampling frequency should be twice that of the highest frequency component present in the signal. In the case of our system, the frequency of the signal being processed will be no more than 20 kHz. This means the analog to digital converter must have a sampling rate of at least 40 kHz.

The original MIT implementation of our radar module used the sound card within a laptop to digitize the radar signal. To mimic this process outside of a laptop, we will be using a 24-bit audio analog to digital converter, the PCM1802 by Texas Instruments. It uses a delta-sigma conversion method and includes internal filters to prevent aliasing.

Best of all, the sampling frequency can go up to 96 kHz, allowing for input signals of up to 48 kHz.

3.4.9 Microcontroller

The microcontroller is the gateway between the analog radar-side of the project and the digital host-side of the project. It is responsible for accumulating the digital samples generated by the analog to digital converter and passing those packets of information onto the host computer. The microcontroller also allows the radar module to be controlled by the host. For instance, capabilities such as frequency changes, switching the radar module on and off, or selecting alternative modes of operation requires that digital commands be converted in analog equivalents. Microcontrollers are a great option for this type of interface, as they are often equipped with analog and digital input and output pins. They can easily receive digital instructions from the host and translate those instructions into analog electronic signals that affect the radar operation.

There are many considerations when selecting a microcontroller, and like many electronic parts, there are often several possible options that will suffice for a given application. We have decided to use the Arduino Zero for our project. This development board is equipped with Atmel's SAMD21 microcontroller. The Zero was chosen for several reasons, including its number of general input/output pins, 48 MHz clock speed, 32-bit ARM Cortex M0+ Core and small size. All of these had an effect on the final decision, though should it be necessary, the Arduino Mega has been identified as a suitable replacement and can be used in the same way as the Zero for our project.

3.4.10 Operational Amplifiers

Both the gain stage and the low-pass stages consist of operational amplifiers, typically called op-amps. Op-amps have five terminals: the non-inverting terminal, the inverting terminal, the positive power rail, the negative power rail, and the output terminal. The positive and negative power rails make the op-amp an active device. The voltages at the positive and negative rail are the limiting thresholds of the output; some op-amps are not even capable of reaching those limits. Typically the absolute value of the power rails are equal, such as +12V and -12V. However, this is not necessary, and in our applications we will use ground as the negative rail.

Several different classes of circuits can be constructed using op-amps, including filters, summing circuits and amplifiers. These circuits could certainly be constructed from passive devices, but the design process is often lengthy due to the interdependency of the circuit stages. One major advantage of using op-amps is that one stage has no direct effect on the following stage, aside from the signal being passed between them. The behavior of each circuit remains independent, allowing for quick design and integration of large circuits. An additional advantage of op-amps is their low cost compared to other devices that provide the same capabilities.

The two types of op-amp circuits used in our design are a gain circuit (or amplifier) and low pass filter. Although these two circuits are cascaded, their behaviors are

independent of each other. The gain circuit has an output that is greater in amplitude than the input. Some op-amp gain circuit configurations are called inverting amplifiers because the gain is actually negative, meaning the output is larger in magnitude but the negative or flipped version of the input. In our design, we will be using a non-inverting amplifier configuration, so the gain is positive.

Filters designed using op-amps have a different focus; they are used to change the frequency spectrum of the input signal. Different types of basic filters are low-pass, high-pass, bandpass and band-reject. Each of these passes frequencies according to either one or two cutoff frequencies. Low pass filters allow frequencies lower than the cutoff, high pass filters allow frequencies higher than the cutoff, bandpass filters allow frequencies between two cutoffs, and band-reject filters allow frequencies outside two cutoffs. In addition to the type, filters can have different names according to their mathematical characteristics. Types of filters in that sense include such as Butterworth, Bessel, and Chebyshev, where each of these has a characteristic shape of the filter's frequency response.

Cascading filters is an excellent way to improve the accuracy of the filtering. Cascading two low-pass filters with the same performance will decrease the presence of frequencies beyond the cutoff more so than if a single filter had been used. In our design, two second-order low-pass filters will be cascaded to create an effective fourth-order filter.

The operational amplifier used in our design will be the LM324N, a quad operational amplifier, meaning there are four separate op-amps powered by identical power rails. Using this device will reduce the space needed on the PBCs. The power rail for the device can span from +3V to +36V, which is more than sufficient for our application.

3.5 Complete System Block Diagram

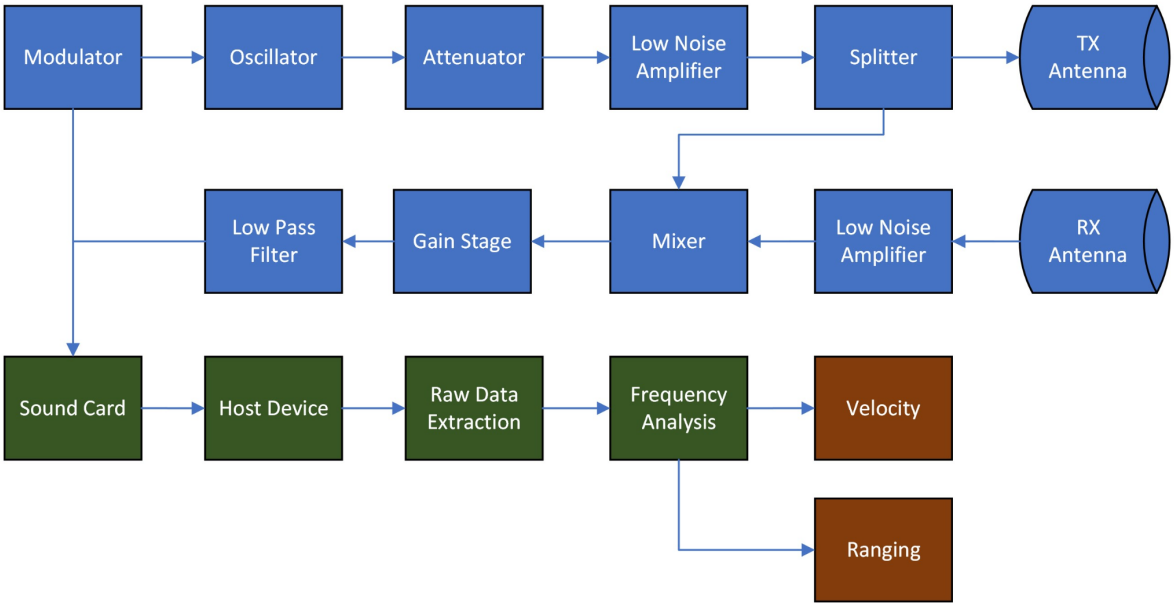
Figure 21 shows a block diagram of our entire system. The design shown can achieve every goal outlined previously, though certain elements may not be needed for any given goal.

The design has been divided into three different subsystems: the RF system, the RF data processing, and the implementation. The RF subsystem is entirely analog. It begins with input DC voltages, which are converted to electronic signals with a defined shape, amplitude, and frequency. This signal is converted to an RF signal that passes through a series of devices via SMA-to-SMA connectors. The signal is sent out into the environment through the transmit antenna and reenters the system through the receive antenna. It proceeds through two additional RF signal processing components before entering two electronic circuits, the gain stage and low pass filter.

The oscillator, attenuator, amplifiers, mixer, and splitter are all single, pre-assembled block components with internal circuitry. The modulator, gain stage and low pass filter are all circuits that will be designed by our team and assembled on PCBs.

The next subsystem is the RF data processing. There are two steps to the RF data processing. The first step is to convert the output signal of the RF system from analog to digital so it can be sent to the host device. The use of a USB2 connection, implemented through the microcontroller (MCU), is a part of the signal transmission to the host device. The second step in the RF data processing is implemented in software. The raw data is extracted from the digital, time-domain representation of the signal by using Fourier frequency analysis techniques. The resulting analysis can then be used for the implementation.

The concept of the implementation subsystem is the display or use of the information gathered in the RF data processing subsystem. For the first two project goals of acquiring velocity and ranging readings, the only necessary aspect of the implementation is to display the readings on the host device monitor. For the third project goal of using the information gathered to drive a control system, hardware may be used in the implementation subsystem such as motors, LEDs, or other devices.



In summary, our RF system design chain will consist of a two-port cascaded network model containing modulator, oscillator, attenuator, amplifier, and splitter. This signal is then sent through the transmitting antenna. The received signal is then sent through a low noise amplifier and finally through a mixer, where it is compared with the transmitted signal. Our part selection for this RF component chain will be centered around our requirements for the above sub-systems.

Once the signal is sent through the mixer, it is sent through the gain stage and the low pass filter. This filtered, amplified signal is then sent out to the ADC. The ADC sends the digitized signal through the MCU to the host device via USB. The host device processes

and analyzes the signal. The information obtained can then be either displayed or utilized in an external system.

One area in which our project may be improved in the future is the host device. As of now, the host device is a laptop like that used in the MIT radar system. Ideally the host device would be included in the radar module itself; this could easily be accomplished through the use of a microprocessor.

4.0 Project Constraints

4.1 Standards

Aligning with standards ensured our project would be easily compatible with existing products and components on the market, as well as remain safe and reliable during operation. Though not entirely complete due to the vast number of standards in existence, the following list covers the standards that were most relevant to our project design.

4.1.1 Hardware Standards

4.1.1.1 IEC 60086-1 Primary Batteries - General

Our radar module had to be portable, so our team decided to power it using 9V batteries. The IEC Primary Batteries standard outlines several important characteristics that should be consistent among general primary (single-use) batteries. Some of these characteristics are physical, such as the dimensions of the battery, while other characteristics are electrical, such as the maximum voltage each battery cell should supply. The most important aspect of this standard is that it allows for batteries from different manufacturers to be used interchangeably, eliminating the need to consider differences in function or form [1].

There are a few implications this standard had with respect to our system design. The first is that the physical size of the batteries was predetermined. Because 9V batteries have standard dimensions, the battery holder we selected had to be the correct size and shape. The way we chose to physically assemble our final integrated system, particularly the power supply, had to take the standard size of 9V batteries into account. Another implication is that the input voltage levels we had to work with were finite. Each new 9V battery had a nominal voltage of +9V, so the only available input voltages were k*+9V, where k is any positive integer. Because of the major implications this had on our power supply circuit design, it was taken into account prior to selecting the type of battery the system runs on. The section on our power supply circuit will further discuss the reasoning behind choosing 9V batteries for our system.

One additional thing to note with regard to our system's batteries is that our system can run on either primary or secondary batteries. If secondary batteries are used, there are additional standards that would apply to their safe use and storage.

4.1.1.2 ANSI C18.1M – Portable Primary Cells and Batteries with Aqueous Electrolyte

This standard is similar to IEC 60086-1. It outlines several standards for portable primary battery cells, including information on safety standards. An interesting subsection of the standard is consideration of potential misuse. Things such as installing batteries backwards, dropping batteries and over-discharging batteries are all addressed [2].

Almost all batteries, even common household batteries such as 9V batteries, come with instructions on how to properly use them. Our team had to abide by these rules because the consequences of misuse have already been tested for and established.

4.1.1.3 IEC 61169-15 – Radio Frequency Connectors (SMA)

There are many types of radio frequency connectors. All of the connectors are used to transmit RF signals, but equipment such as spectrum analyzers and components such as RF frequency mixers come with certain connectors already embedded. If a device has a certain connector already on it, the complementary connector must be used to securely attach a cable or another device. For instance, if a device has a male N-type connector, a cable with a female N-type connector must be used to access the device port.

The IEC 61169-15 standard outlines the physical dimensions and quality parameters for the SMA connection [3]. The high frequency components of our radar module all came with female SMA connections, so in order to connect them, our team needed to ensure we used male SMA to male SMA cables or adapters. Using other types of connectors would not ensure a solid electrical connection.

The SMA standard was also important for the design of our PCB. One PCB in our design uses an SMA connector for one of its input signals since it interfaces with a device that uses an SMA connector for its output. Knowing the size and construction of a standard SMA connector partially dictated the design of the PCB, as the size and electrical characteristics of the SMA connector had to be taken into account.

4.1.2 Software Standards

Programming language and other software standards are a bit different from hardware standards, especially when it comes to the consequences of diverging from them. Imagine trying to insert an SD card into a microSD card port; it simply would not fit, and the lack of adherence to the standard would be quite obvious before the system is constructed and tested. But in software, failing to align with standards may have consequences that are not apparent until after system implementation.

An example of this is programming language compilers. They typically will either give an error or a warning when users diverge from standards, such as not using correct syntax. But computers are not mind-readers. Even if code technically aligns with standards, it is

possible that the functionality of the code is not what the user intended because the user did not align with standards before attempting to use them.

Our project has two subsystems that use software, the USB interface and the API. Standards specific to USB have been listed in the Hardware/Software Hybrid Standards section, but because our USB interface uses a programmable microcontroller, standards related to the language used to program the microcontroller have been included in this section.

4.1.2.1. MATLAB Programming Language

The program our team developed for displaying range and velocity plots was based on the MATLAB code provided by MIT for their laptop-based radar. MATLAB is a high-level programming language that makes it easy to manipulate matrices of data. In our project, it is used to manipulate and process the digitized output signals from the radar module. In order for the code to work properly, our team had to make sure it aligned with the standards of the MATLAB coding language, especially with regards to matrix indexing. Unlike some other programming languages, MATLAB is not zero indexed; rows are index one rather than index zero, and columns are index two rather than index one. This characteristic of the language is one that can easily be overlooked, as mistakes can be made that are technically allowed by the compiler but do not produce the intended results. As with any programming language, understanding the specifics of the language helped facilitate the software development and troubleshooting process.

4.1.2.4 Ripple Radar API Standard

One way to ensure our API is easily adaptable by the end-user is to use a standard API as the baseline code. The Consumer Technology Association (CTA) hosts Ripple, an open radar API standard released in January 2022 [7]. According to the CTA website, Ripple has been especially designed for general purpose consumer radar and is meant to enable hardware and software interoperability for radar applications. Ripple can be thought of as a more specialized version of a software standard; it defines special functions and structures that must be used in a certain way, but which can be combined to create certain functionality in a project. Choosing to align with this standard facilitates software development for our project by making it more straightforward to extract information from our radar module. Ripple also makes it easier to adapt code for other radar modules or for other software designers to understand and later modify our API.

4.1.3 Hardware/Software Hybrid Standards

4.1.3.1 IEC 62680-2-1 – USB Specification

Our team wanted an interface for our project that would be compatible with most laptop computers. There are a limited number of port types used for inputting data to a laptop, the most common being USB, audio, ethernet, and SD/microSD. We chose USB

because it is easiest to implement from a technical perspective and also a common port for laptops.

Standard IEC 62680-20-1 is a very extensive document, covering nearly all aspects of a USB interface both on the hardware side and the software side. According to the standard preview provided by IEC, topics discussed include USB architecture, the data flow model, considerations for isochronous transfers, the mechanics of USB assemblies, electrical characteristics, protocol layering, device framework, USB host requirements, and hub specifications [8].

This list alone indicates that the USB standard imposes many restrictions on our project interface design. Manufacturers have already aligned their laptops with the standard both in hardware and in software, so even a slight change such as a slightly bigger wire housing will render our interface essentially unusable. Though these restrictions leave little room for freedom of design, aligning to the standard actually facilitates the development of our system's USB interface. So long as we align with the standard, any laptop with a USB input port will be compatible with our interface, and the laptop can therefore be used to receive and process signals from our radar module.

4.1.3.2 SCPI-99 – Standard Commands for Programmable Instruments

The Standard Commands for Programmable Instruments (SCPI) standard provides a structured means of controlling electronics test equipment and automatic test equipment [9]. SCPI originally sat atop the IEEE 488.2 General Purpose Interface Bus (GPIB) specification which dictated how bytes of data were communicated between these pieces of test equipment and computers, but did not provide a rigid command syntax for making measurements. In this sense, it was possible for two different devices to employ the IEEE 488.2 specification to communicate with a computer, but they may have had completely different sets of commands to make measurements. This greatly complicated the testing process, where many pieces of test equipment may be connected to a single computer by way of bus topology. Examples of such standardized commands include the following (where capitalized letters are required and lower case letters are optional): "MEASure:VOLTage?" to measure the average voltage at a test point with a multimeter; "SOURce1:FREQuency 100" to set the frequency of channel 1 on a function generator; "MEASurement1:MAIN FREQuency" to select the frequency as the measurement of interest of channel 1 on an oscilloscope; and "MEASurement1:STATistics:VALue:ALL?" to retrieve all of the statistics of the aforementioned measurement, which includes the peak & trough values, the standard deviation value, and the average value.

4.1.3.3 VISA - Virtual Instrument Software Architecture

The aforementioned SCPI standard was originally intended to work with the IEEE 488.2 GPIB interface, however newer bus interface developments have occurred throughout the years. The Virtual Instrument Software Architecture (VISA) [10] specification defines an Application Programming Interface (API) that enables communication with a wide variety of pieces of test equipment using a multitude of different interface standards,

such as GPIB, USB, and TCP/IP. Users can leverage this API to write programs that communicate with test equipment by issuing SCPI commands.

4.2 Constraints

4.2.1 Federal Communication Commission

Any project involving wireless transmission should verify compliance with Federal Communication Commission (FCC) regulations. The FCC regulates what, when, where, at what power, and at what frequency we are allowed to transmit signals in the U.S. The reason for wireless transmission regulation is that devices are tuned to receive at certain frequencies. If signals other than the expected signal are being broadcast at the same frequencies, interference is created, and depending on the application, the consequences can range from being merely inconvenient to having a drastic effect on national security. To ensure our project adhered to federal regulations, we had to understand exactly how the FCC regulates wireless transmission.

The basis for regulation is dividing the frequency spectrum into bands. Bands are then allocated for specific purposes such as radio stations, military communication, or cell services [11]. In order to broadcast frequencies within a certain band, permission must be granted by the FCC. In most cases a license must be obtained, but ISM bands have also been allocated. ISM bands are for Industrial, Scientific and Medical use license-free. Consequently, the bands are often used for hobbyists' projects and for short-range communications such as Bluetooth [12]. Our project uses the 2.4 GHz ISM band to avoid going through the tedious process of obtaining a license from the FCC.

Although a license is not required to transmit in the 2.4GHz band, there are still restrictions that must be adhered to. These requirements include parameters such as maximum transmitted power and number of channels for channel-hopping devices. The restriction we are most concerned with is the transmit power. According to the FCC, the maximum transmit power allowed in the 2.4GHz band is 1W [20]. This had to be taken into consideration when designing our RF subsystem. A higher transmit power is ideal according to our project's house of quality, but the maximum power is capped by the FCC regulation.

4.2.2 Time Constraints

A major constraint in our project was time. The course policies outlined at what time the final project was to be completed, which was this month, April 2023. There were also several reports due periodically up until the project completion date, at which time certain components of our project had to be completed. The planning and design work, and corresponding documentation, were to be completed by December 2022, and the prototype construction and testing have just been completed as of this month. But simply looking at the deadlines set forth by the course policies was insufficient to completely understand the time constraints placed on the team back when the project began.

An important factor to consider in any project is the dependencies between tasks. Completing three independent tasks that each take one month does not imply the same time constraint as completing three tasks of the same length, but with the condition that one task must be done after the other. This shows that additional time constraints are created by the dependencies between tasks in a project. Our project's subsystems could be designed and developed independently up to the point of integration, at which point a setback in one aspect of the system would cause a setback for the entire integration process. Ultimately this could've extended the anticipated completion date of crucial, end-of-project tasks such as the final demonstration. The team had to work to not only get tasks done in a timely fashion but also take into consideration task dependencies. It was the dependencies that drove our prioritization of team tasks.

In addition to time constraints created directly by the course calendar, everyone on the team had other commitments outside of Senior Design. We may have been allowed four weeks to complete a certain task according to the course guidelines, but in reality, our team members had only two to three weeks' worth of time to actually work towards completing that task. Additionally, unexpected setbacks such as supply chain issues could have delayed task completion. This is why our team strived to complete tasks as early as possible.

In order to keep to a plan that was well ahead of schedule, our team had to consider the effects supply chain issues would have on hardware acquisition. Certain suppliers may have had long lead times for crucial elements in our design, or they may not have had our preferred item available at all. Shipping times were potentially lengthy when ordering hardware or PCBs. It was the team's responsibility to check lead times, shipping times and product availability for multiple suppliers to determine which could deliver our items as quickly as possible. This was especially important when design changes were made or replacement parts were needed very close to deadlines.

4.2.3 Economic Constraints

Because our team was donated a partially completed radar, we were relieved of the bulk of our project's cost. The radar signal processing hardware such as the mixer, splitter and oscillator, in addition to the many SMA connections, were the most expensive components of the design. However, in preparation for the worst -case scenario in which we no longer had access to the donated parts, our team had to consider the maximum extent of our economic resources.

We wanted to keep the overall cost of our project below $800. Because we had no sponsor aside from Dr. Gong's part donation, our budget implied a maximum contribution of $200 per team member to complete the project. We needed to keep costs within these bounds, and if necessary, we could modify our design or source parts from suppliers who offer cheaper prices than our preferred suppliers.

The supply chain issues mentioned in the Time Constraints section are, at their root, economic constraints. In our current market, there is still a shortage of certain electronic components. When these items have high demand and low availability, it drives prices much higher than they would be under normal conditions. The team's first choice of parts or suppliers could easily have turned out to be unreasonably expensive, so it was anticipated that alternatives would need to be considered.

4.2.4 Health and Safety Constraints

There are a few things that had to be taken into consideration when performing RF transmission experiments. Electromagnetic radiation can cause biological harm under certain conditions if the proper precautions are not taken. There are three parameters that determine the safety factor of a particular RF experiment. These are the transmitted power, the transmitted frequency, and personnel proximity.

From a technical standpoint, high-power RF systems are used to achieve high resolution or to reach targets at extended distances. However, the introduced risk is that organisms in the presence of the high-power energy could potentially be harmed. The amount of energy absorbed by a person or animal in the presence of RF energy is typically measured in watts per kg (W/kg) or milliwatts per gram (mW/g) [13]. If this measurement is too high, damage to body cells may occur causing serious medical issues.

Another significant parameter in radar systems is the frequency used. Much like power level, frequency is catered to the specific radar application. High frequencies are better suited for speed and high resolution, while low frequencies are best for range. According to the FCC, humans absorb RF energy at a maximum rate when the signal frequency is 70 MHz; this is why RF safety standards typically apply to frequencies between about 30 to 300 MHz. When in these ranges of operation, it is crucial to consider the effects the transmitted signal may have on nearby people or animals.

Note that personnel proximity is an important factor when considering safety implications of both frequency and transmitted power level. Even if an RF system is transmitting at around 70 MHz and at a relatively high power, if there is nobody within the range of the radar system, there poses very little if any risk of causing harmful biological effects.

Our project is designed to operate at 2.4 GHz (in an ISM frequency band) and transmits approximately 10 mW (10 dBm) of power. This means there is very low safety risk, and pretty much any location away from sensitive lab equipment or people with high health risks should be suitable for conducting our tests. However, it was still very important that we verified that our system was operating as intended before performing field tests. If the system was actually transmitting at a different frequency or higher power level than desired, there would be significant safety implications.

Aside from the RF safety factors of our system, there was a safety concern regarding the thermal characteristics of our design. Electronic systems, especially poorly designed power systems, have the potential to heat up very quickly. Normally the worst-case scenario in these situations is component failure and ultimately damage to the device, but for our project, the PCBs and components were originally mounted on a wooden board, and then a plastic chassis. A potential consequence of allowing any of our components to overheat was the module melting or even catching fire! Not only would this be unacceptable from a technical perspective, but it would put the consumer in danger. PCBs often have heat sinks added for components that tend to heat up, and selecting circuit elements wisely can prevent components from heating up in the first place. Our team had to take all of this into consideration when designing and constructing our radar module, but the team determined that our final design had no significant thermal activity.

4.2.5 Manufacturability Constraints

The radar module that our team was donated by our sponsor is a wooden board with all the components of the high-frequency RF subsystem already attached. This included the MiniCircuits RF circuit packages and the antennas. Although the plan was originally to use the preexisting wooden chassis, our team decided to fabricate a smaller, more aesthetically pleasing plastic chassis and cover. The design process from there was to ensure that the remainder of the components for the radar would be able to fit on the chassis.

It was a course requirement that our project involved a PCB, so our team decided to create one PCB for the modulator circuit, one PCB for the low pass filter and gain stage, and one PCB for the power supply. We just needed to make sure the PCBs were of the appropriate dimensions to fit on the module chassis. Rather than mounting the PCBs directly to the chassis, standoffs were used, which added minimal additional weight to the module.

Fitting the PCBs onto the chassis was not just a matter of putting puzzle pieces together. Each of our PCBs has certain inputs and outputs. It would not be wise to place a PCB all the way to the left of the board if its input is coming from the right side of the board. Additionally, the power supply circuit powers every other circuit on the board, so it needed to be placed strategically. This was taken into consideration when determining the mounting holes' positioning in the chassis.

5.0 Hardware Design

5.1 Power Supply Circuit

The power supply was designed anticipating that all circuits needed to reach the real-time processing goals would be included in the final prototype. Although some of these circuits were ultimately not used, such as the ADC circuit, the voltage level and current requirements for such circuits were still taken into consideration.

There are three supply voltages required for our system to operate: +3.3V, +5V and +12V, all DC generated from alkaline batteries. The +12V supplies the modulator, which pulls 12mA. The +5V supplies the op-amp positive rails in the gain stage and low pass filter circuits, the oscillator, the low noise amplifiers and the analog-to-digital converter, which collectively pull about 200 mA. +3.3V supplies the microcontroller in our system, and its current draw is highly dependent on the application and which pins are being used. Although our current design has the MCU running on power from the host CPU, the power supply will be designed for the worst case scenario in which the microcontroller pulls 200mA from the batteries. +3.3V is also used for the analog-to-digital digital supply voltage and the offset voltage in our op-amp circuits, though these contribute negligible current draw. These current and voltage requirements will drive the design of our power supply circuit.

5.1.1 Battery Selection and Configuration

Because we knew the necessary supply voltages for our system, we were able to select which type of batteries we wanted to design for. There were three important considerations when selecting the batteries. The first was that the battery type should be easily accessible to the consumer. The second was that the number of batteries in total should be kept to a minimum. The third was that battery depletion must be kept in mind. Our team decided to use buck converters for efficiency purposes, so choosing batteries that added up to exactly the needed voltage levels would be insufficient. The battery voltages would soon deplete to just below their nominal levels, and then the buck converters would not be able to supply the voltages needed to power the components in our system. In consideration of all these points, our team chose to design around the use of common 9V alkaline batteries.

9V batteries are affordable and accessible to the general consumer, which is one of our desired system characteristics. In order to generate the three voltages required from 9V batteries, our design uses 4 batteries. First, two batteries were placed in parallel to increase the total capacity. Each battery has approximately 600mAh of capacity alone, and when batteries are placed in parallel their total capacity is equal to the sum of their individual capacities. Our design then generates a higher voltage by placing another pair of +9V batteries in series with the first pair. This doubles the available voltage to +18V. This means our design contains four +9V batteries in total. There is one +9V node, one +18V node, and approximately 1200mAh capacity for each node. The battery configuration is shown in Figure 22.

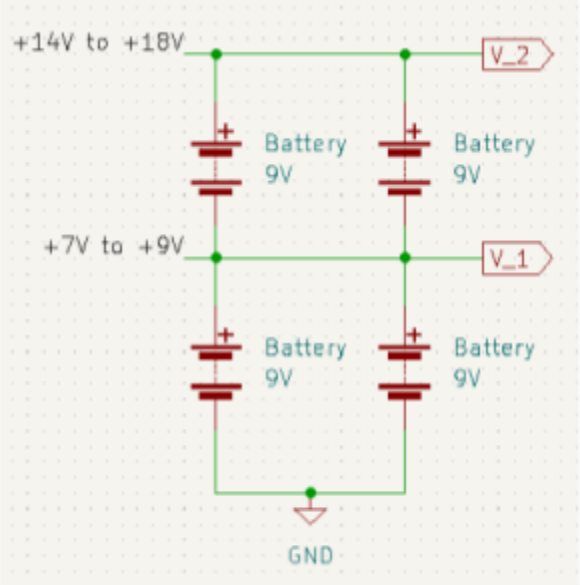


Fig. 22. Power supply battery configuration.

Now that our batteries and their configuration have been established, the circuit design can be discussed. Our goal was to achieve an output of +3.3V, +5V and +12V regardless of fluctuations in the batteries' voltages, at least up to the point where the batteries would simply be considered dead. The tool our team used to design our power supply is Texas Instruments' WEBENCH tool. It takes in the desired output voltage, desired output current and the range of input currents, and outputs a variety of possible power supply circuits that could be used to achieve the desired goals. The chosen design is a balance of cost, PCB footprint and efficiency.

5.1.2 +3.3 V Power Supply

For our +3.3V circuit, the input voltage may range between +9V (when the battery is full) and +7V (when the battery is nearly dead). And as mentioned before, the output current at +3.3V needs to be 200mA in the worst possible case. Figure 23 below shows the chosen design for the generation of +3.3V from an input voltage of V_1. The key component in the design is the TPS54233 by Texas Instruments, a +3.5V to +28V input, 2A step-down DC to DC converter. It takes in the input voltage of between +9V and +7V produced by the first pair of batteries and reduces it down to +3.3V for our system components.

The two resistors tied to the PH and VENSE pins of the converter determine the output voltage of the circuit. Equation X gives the relationship between the circuit's input and output voltages. V_{ref} is +0.8V, R_1 is the resistor tied to PH, and R_2 is the resistor tied to ground.

$$V_o = V_{ref}\left(\frac{R_1}{R_2} + 1\right)$$

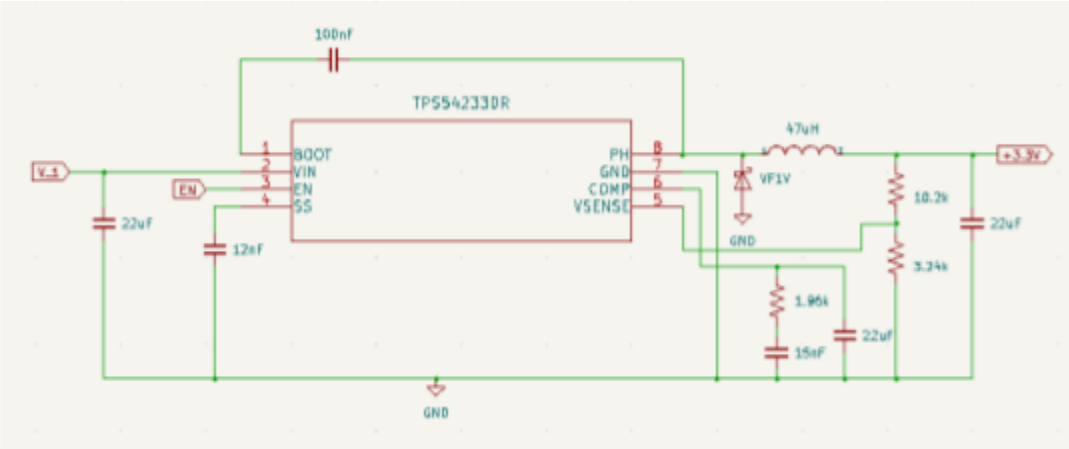


Fig. 23. +3.3V power supply circuit.

The circuit uses an input decoupling capacitor to smooth out any ripples that may be present in V_1. The capacitor connected to the SS pin is used for setting the start-up time for the circuit; using the equations available in the converter datasheet, a 12nF capacitor results in a start-up time of 5 milliseconds, which is within the recommended range of 1 millisecond to 10 milliseconds. The components at the COMP pin function as external compensation for the converter. TI's WEBENCH tool automatically generates the appropriate values for these components, though they can be manually calculated using the corresponding datasheet equations. An additional inductor and capacitor were used for output filtering, and the remaining components were required per the design of the converter.

5.1.2 +5 V Power Supply

A similar approach was used to design the +5V supply voltage circuit as was used for the +3.3V circuit (see Figure 24). Note that the input voltage is still coming from the first pair of +9V batteries, so the input is still potentially varying between +9V and +7V. The only difference is that, at a maximum, the amount of current being drawn at this voltage level is only 150mA rather than a potential 200mA for the +3.3V supply. Regardless, because the desired output voltage and current are still within the range of the TPS54233DR, it was used again for the +5V power supply.

The only differences between the components in the +5V supply and +3.3V supply circuits were the value of the resistor tied from VSENSE to ground (which sets the output voltage), the value of the output capacitor, and the components at the COMP pin.

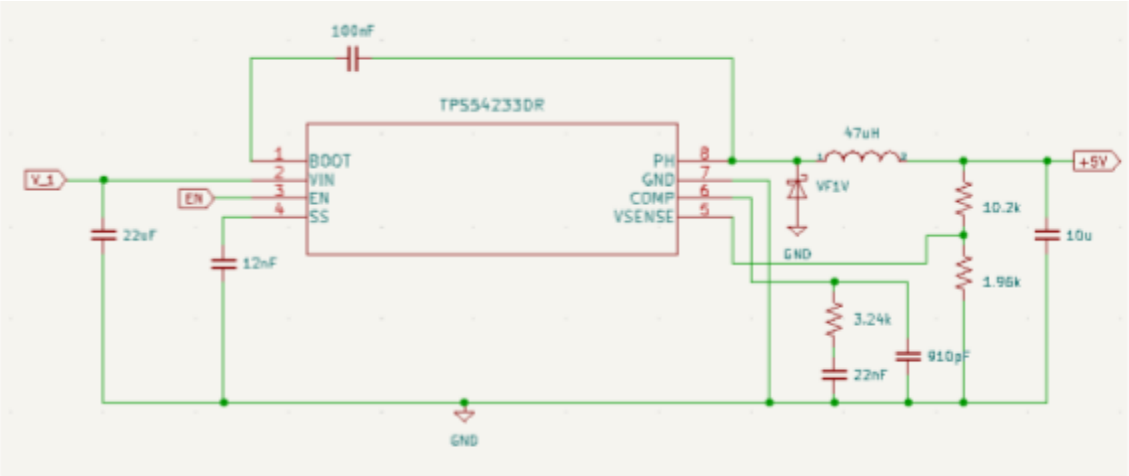


Fig. 24. +5V power supply circuit.

5.1.3 +12 V Power Supply

Lastly, there is the circuit for the +12V supply. This circuit will use the voltage generated from using both pairs of batteries and requires only 12mA to be output. Because two pairs of parallel batteries were being used instead of one, the voltage can vary more as each pair of batteries begins to deplete. If each pair reduces to only +7V, then the total voltage supplied will only be +14V. Though this particular scenario is unlikely considering the small current being drawn at the +18V node, it must be taken into account when designing the circuit. Figure 33 shows the results of the WEBENCH design search. The key component is the LMZM23600 step-down power module. It has a higher output voltage capacity of +35V but a lower maximum output current at 0.5A. This is perfectly suited for the +12V supply since the primary concern is the output voltage, not the output current. Note that in Figure 25, the input voltage is coming from the V_2 battery node.

The TPS54233DR DC to DC converter is used once again as in the +3.3V and +5V power supply circuits, and the same components were modified as discussed in the +5V power supply design. The voltage divider at VSENSE and PH pins were adjusted to generate a +12V output, and other components were adjusted as necessary to account for the change in output voltage and current.

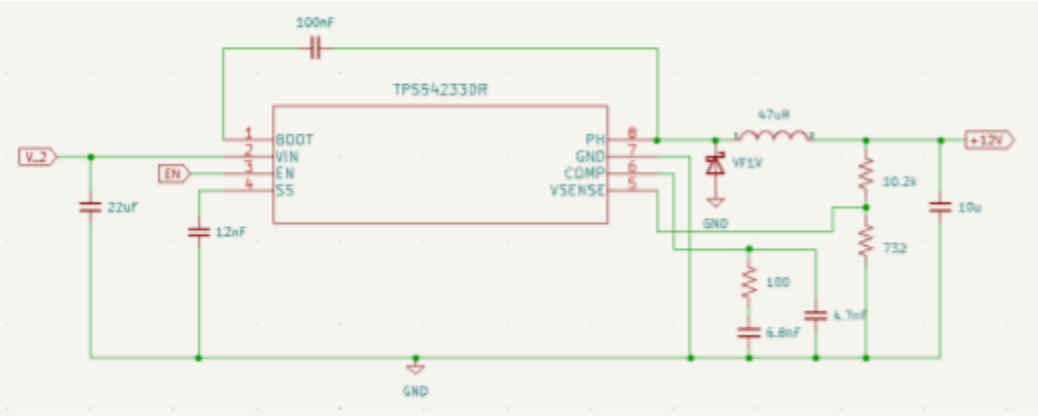


Fig. 25. +12V power supply circuit.

5.1.4 Complete Power Supply Circuit

The complete power supply schematic is shown in Figure 26.

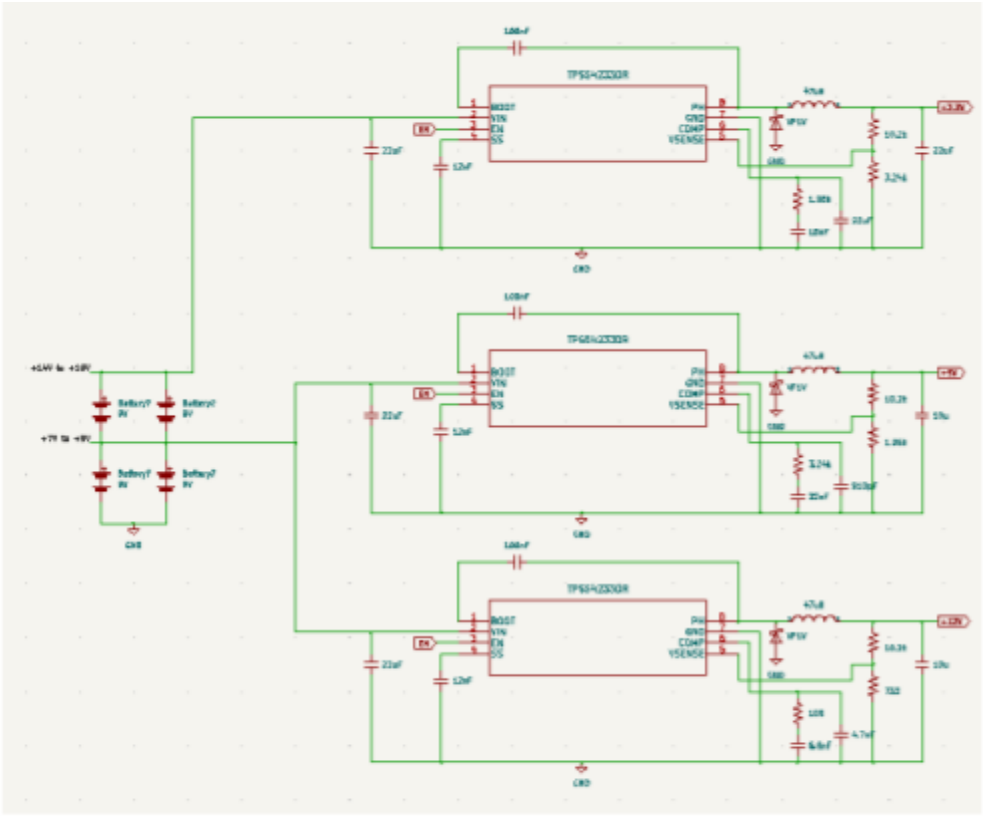


Fig. 26. Complete power supply circuit.

5.1.5 Power Enable Functionality

One additional capability of our system is a power-down function. This was intended to be controlled by the host device and implemented through the MCU, though this functionality was ultimately not implemented in the final prototype. It will be discussed here, though, as it is something that can easily be added to improve the system later on. Note that there are pins denoted as “EN" on each of the three voltage regulation devices used in the power supply circuits. The EN pins are active high, which means that the voltage regulation device only generates an output when there is a high voltage on the EN pin. For the TPS54233DR, voltages over +1.25V are considered sufficiently high. Alternatively, the pin may be left floating to keep the device enabled. If the EN pin’s voltage is less than +1.25V, the device generates no output. This feature will be used to power the radar module on and off via host control.

The MCU used to process the ADC data in our original system would have been used to drive the EN pins in the power supply. When the host device would give the command for a system power-up, the MCU would have changed the output of a designated digital pin to high. For powering down, the MCU digital output would have remained low.

5.2 Modulator Circuit and Oscillator

There are two basic applications of our radar module: doppler (for measuring velocity) and ranging. For doppler, the transmitted signal only needs to be of a single frequency. For ranging, the frequency is linearly swept in a triangle-wave pattern. In our project, going from a single transmit frequency to a swept frequency is simply a matter of disconnecting the +12V supply from the modulator circuit. This changes the output of the modulator from a ramp with a DC offset to just a DC value at the center of that ramp.

The oscillator has a linear input-output relationship between the voltage at its Vtune pin and its output pin. If the effects of other parameters such as temperature are ignored, there is only one possible oscillator output frequency for any given Vtune voltage. This means that for a doppler application where only one output frequency is needed, Vtune will remain constant. The correct voltage would be determined from Figure 27, which shows the relationship between Vtune and the oscillator output voltage at 25 degrees Celsius.

A higher frequency is ideal for maximum resolution in doppler applications. The highest frequency in the ISM band our project operates in is 2.495 GHz, so for a simplified configuration that achieves the highest possible velocity resolution, Vtune could be tied directly to +3.2V. However, due to the nature of the modulator circuit, the constant voltage used will be +2.6V.

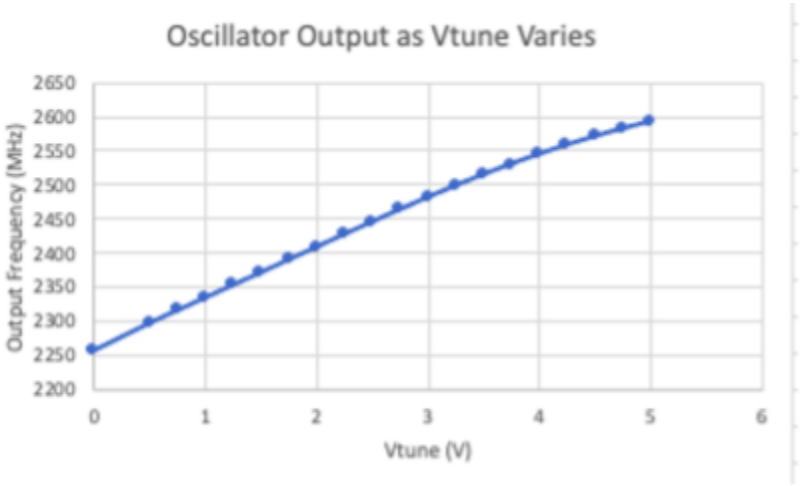


Fig. 27. Oscillator output characteristics.

For the ramp, the signal will begin at a certain frequency, increase linearly until it reaches a stop frequency, then linearly decrease at the same rate until it returns to the start frequency again. This increase and subsequent decrease in frequency constitutes a single period of the signal, which is called a chirp in the context of our RF transmitter.

Before the modulator circuit could be designed, we needed to specify the desired transmit frequencies and the desired length of a chirp in seconds. The frequencies were dealt with first. Our system operates in the entire 2.402 GHz to 2.495 GHz ISM band, resulting in a 93 MHz bandwidth. Figure 27 shows that the corresponding voltage sweep should be from +2V to +3.2V. This provides two specifications that must be dealt with separately in the modulator circuit design: the triangle wave peak-to-peak voltage is 1.2V and the offset voltage is +2.6V. The resistance at the modulator pin 3 is used to control the triangle wave amplitude. A series capacitor and voltage divider at the modulator pin 2 output sets the DC offset. The series capacitor filters out any DC offset already present in the signal, and the voltage divider creates the new DC offset.

$$2.6 = 5\frac{R_1}{R_1 + R_2} \rightarrow R_2 = 0.923R_1$$

The next step was to set the period of the triangle wave. The total period, consisting of the signal linearly increasing and subsequently decreasing back to its start value, is called a chirp. The chirp rate was set to 40 milliseconds. The signal period of the modulator's output signal is set by two components, the timing resistor connected to either Pin 7 or Pin 8 (our design uses Pin 7) and the external timing capacitor across pins 5 and 6. See Equation X.

$$f_0 = \frac{1}{RC} Hz$$

Though there are an infinite number of combinations that would result in our desired signal period, there are also recommended values for the resistor and the capacitor. The modulator datasheet states that the resistance should be within the range of 4kΩ

and 200kΩ, while the capacitor value should remain within 1000pF and 100μF. Our design uses a 100kΩ resistor in series with potentiometer for the resistance, and the capacitor is 0.47μF. This allows the signal period to be varied if desired, but for a 40-millisecond period, the potentiometer resistance would be set to 84kΩ, for a total resistance of 85kΩ.

Lastly, it should be noted that the modulator has an additional output, a square wave which has a rising edge aligning with the beginning of the ramp and a falling edge aligning with the halfway point of the ramp. This signal is used for de-chirping recorded ranging profiles, since the rising edge of the square wave would denote the start of a new chirp. For our velocity applications, this isn't necessary because the transmit frequency is constant; there are no start and stop frequencies that define a chirp.

Figure 28 shows our modulator circuit. The inputs are +12V to power the circuit and +5V to create the output DC offset voltage through the voltage divider. The outputs are the ramp signal, which is sent to the oscillator for both doppler and ranging applications, and the square wave signal, which is used for ranging applications. Note that the square wave signal can still be recorded for ranging, it will just go unused.

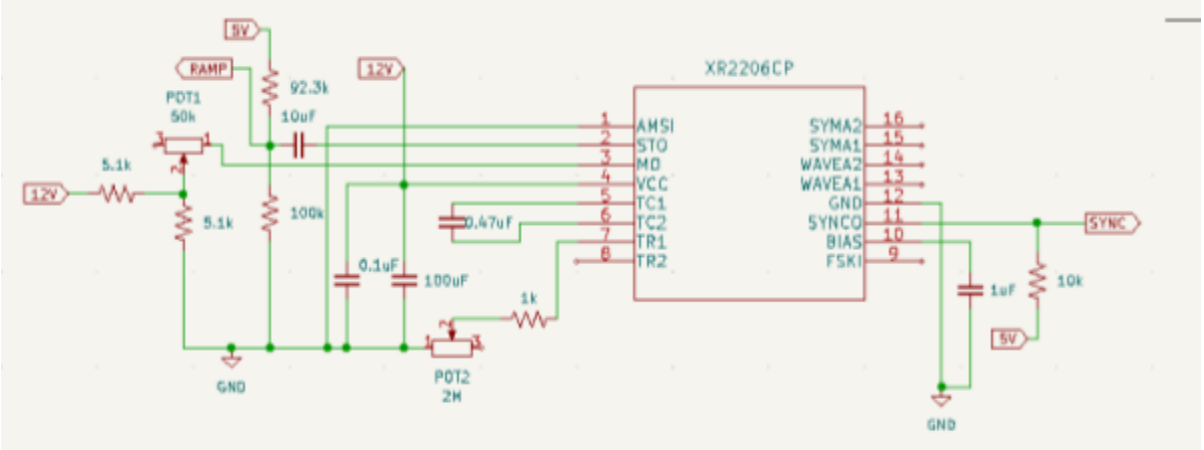


Fig. 28. Modulator circuit.

5.3 RF Subsystem Design

The RF subsystem is a series of components that changes either the frequency or power of the input signal. The input signal to the series comes from the modulator circuit and oscillator discussed in the previous section. The oscillator is the first component in which the signal power analysis switches from traditional DC power analysis using resistance, current and voltage relationships to using RF power analysis. In RF power analysis, signal power is measured in decibels per watt (dB), or in the case of a low powered system like our radar module, decibels per milliwatt (dBm). This change in signal type is accompanied by a change in connector; rather than using jumper wires, the RF subsystem will use SMA to SMA connectors between its components.

Figure 29 shows how the components of our RADAR module were interconnected. For sensing the environment, a signal is generated at Modulator 1 and moves through the system, out the transmitting antenna, back in from the environment into the receive antenna, and then continues until it exits through the video amplifier. This final signal, in addition to another output signal that is generated by the modulator, holds the information that is subsequently digitized and analyzed.

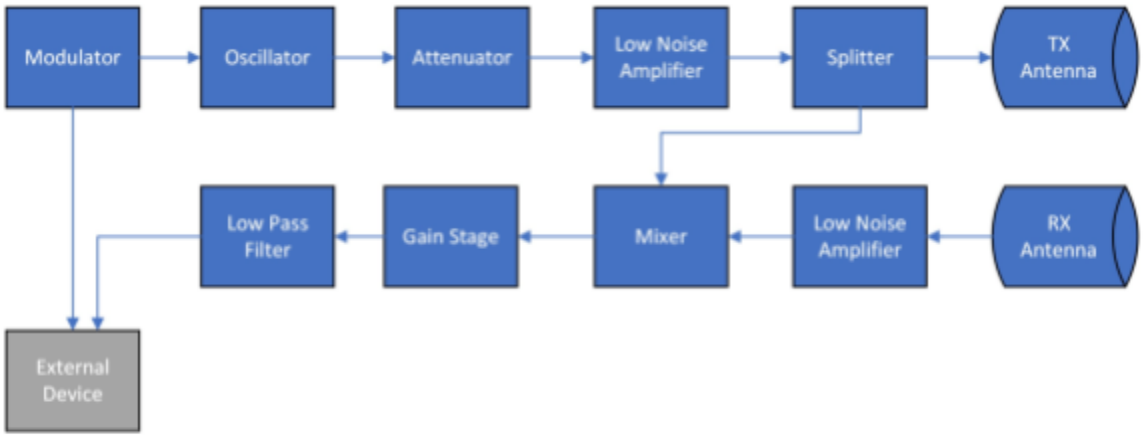


Fig. 29. RF subsystem block diagram.

The RF system may be viewed as a series of power increases and decreases as the signal moves through each component. The oscillator's output power is +6dBm; this is the starting signal power. The next component in the system is the attenuator. Attenuators have multiple functionalities. The first is to decrease the power of an incoming signal. The second is to improve the impedance matching of the system. Here, the attenuator is used directly before a power amplifier, so its primary functionality is impedance matching rather than decreasing the signal power. For the MiniCircuits VAT-3+ attenuator used in our system, the attenuation is dependent on the frequency of the signal. Our signal is below 3 GHz, so the attenuation is only 0.2dB. When working in decibels, scaling is done by addition rather than multiplication, so the signal power is now +6dBm minus 0.2dBm, which is +5.8dBm.

Next comes the power amplifier. It boosts the signal power by 11.5dB at a minimum, bringing the signal power up to at least 17.3dBm. After the amplifier comes the splitter. The splitter has two effects on the incoming signal. The first is that it sends identical copies of the signal to two separate output ports. But as the result of splitting the signal, the power of each signal is only half that of the original signal. This corresponds to a decrease of 3dB. So after the splitter, two identical signals of 14.3dBm are created, one of which is routed to the mixer and the other which is routed to the transmitting antenna.

The transmit antenna has an associated gain of 8.1 dBi, so the final power of the signal at transmission is 22.4dBm, which is about 150 mW. The transmitted signal loses power as it propagates through the air, hits targets in the environment, and comes back through the receive antenna. The power of the received signal cannot be directly calculated. It is dependent on many factors, the most relevant to our application being

the distance and velocity of targets in the environment. The material composition, size and shape of the target also have a significant effect on received power. However, the received signal power can be approximated as being between -150dBm and -50dBm. -100dBm will be used in the discussion moving forward.

The receive antenna has the same gain as the transmit antenna, so the signal is increased by 8.1dB upon reentry into the system. Its power is now -91.9dBm. Immediately after the signal comes through the receive antenna, it goes through a low noise amplifier that increases the power by 11.5dB at a minimum (this amplifier is the same as that used before the splitter). This results in a signal power of -80.4dBm. The final component of the component in the system that uses RF power analysis is the mixer. Aside from any activity in the environment, the mixer is the only element of the RF subsystem that alters the frequency of the signal. The original signal is fed into the mixer's LO port. The received signal from the environment is fed into the mixer's RF port. The frequency of the signal at the IF port is equal to that of the original signal minus that of the received signal, effectively producing a signal whose frequency directly reflects how the signal's frequency changed while it was propagating through the environment. In addition to a change in frequency, the input signal to the mixer's RF port sees a maximum drop in power of 6.3dB at the output port. The signal power is then -86.7dBm by the time it reaches the gain stage. Figure 30 below shows a diagram of the power flow through the RF subsystem, from the oscillator to the mixer.

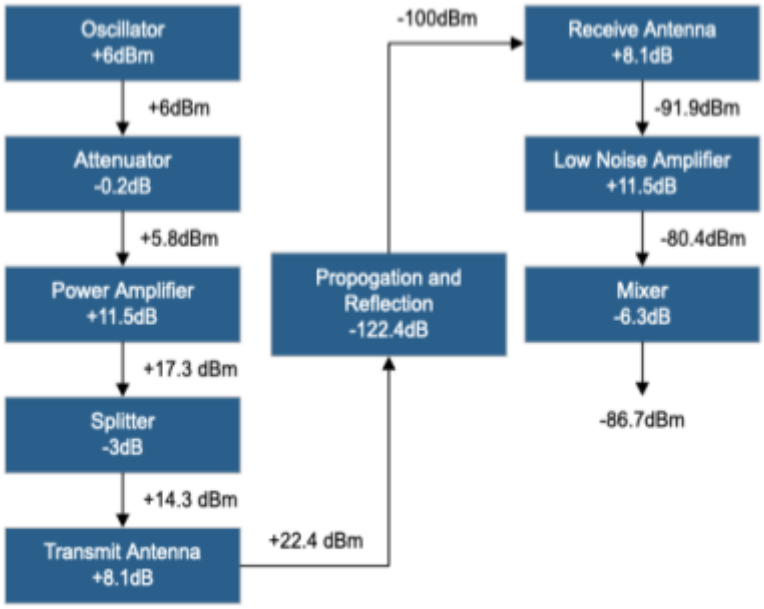


Fig. 30. Example power flow diagram for the RF subsystem.

For close-range applications, the loss due to propagation and reflection is likely to be much lower, so the final signal power will be much higher.

5.4 Gain Stage

The gain stage is the first circuit coming after the RF signal processing components. The SMA connector from the mixer leads to an SMA connector on the gain stage PCB, and that SMA connector feeds two traces (ground and signal voltage) into the gain stage circuitry. The power analysis will now be converted back to a DC analysis. The incoming power is on the order of -10dBm. Three concepts were used to determine the input voltage to the gain stage: the relationship between power in dBm and power in watts, the equation to calculate voltage from watts and resistance, and the impedance of the RF signal processing components, which is 50Ω. An input RF power of -80 dBm will be used as an example to illustrate the calculations.

-80 dBm is equivalent to 10^{-11} watts. The corresponding voltage into the gain stage is then the square root of 10^{-11} times 50Ω, which is 22μV. This means that the order of the voltage going into the gain stage is on the order of microvolts. This is much too small for accurate signal analysis, so the signal needs to be amplified further. An adjustable active non-inverting amplifier will be used for this purpose.

The active amplifier consists of two resistors, a capacitor, a potentiometer and an operational amplifier. The capacitor and resistor tied to the non-inverting terminal of the op-amp serve to create a DC offset for the incoming signal. As it is, the signal is sometimes positive and sometimes negative; to make the signal positive all the time, it must be offset by some DC value. Our team has decided on an offset of +3.3V, which is what the other end of the resistor is tied to. On the inverting terminal of the op-amp, there is one resistor going to +3.3V and a potentiometer tied to the output terminal. These two resistances determine the gain of the circuit as given in Equation X, where the resistor is R_1 and the potentiometer is R_2. .

$$Gain = \frac{R_2}{R_1} + 1$$

Because one of the resistances is variable, the gain of the circuit is variable. Depending on the particular application of the radar and the measured power ratings of the RF signal processing components, the gain of the circuit will need to be adjusted. The gain can vary from unity to 45.45. This is enough to get the signal voltage up to the order of millivolts instead of microvolts. Figure 31 shows the gain stage schematic.

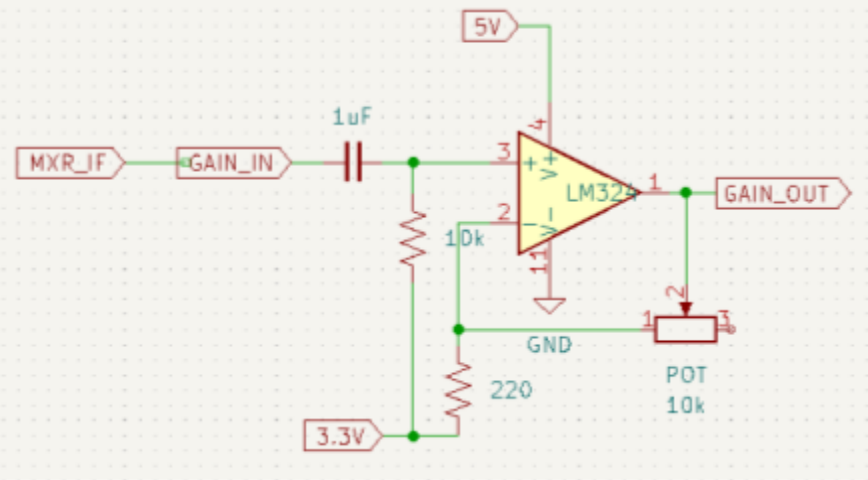


Fig. 31. Gain stage schematic.

Multisim was used to simulate the gain stage circuit design and verify that it is operating as desired. The primary concern was the gain of the circuit. We wanted to make sure the actual gain aligns closely with the theoretical gain for a given value of the potentiometer. For demonstrative purposes, the potentiometer was set to its maximum value and represented as a resistor in the Multisim circuit. Figure 32 shows the circuit being simulated, with input and output probes.

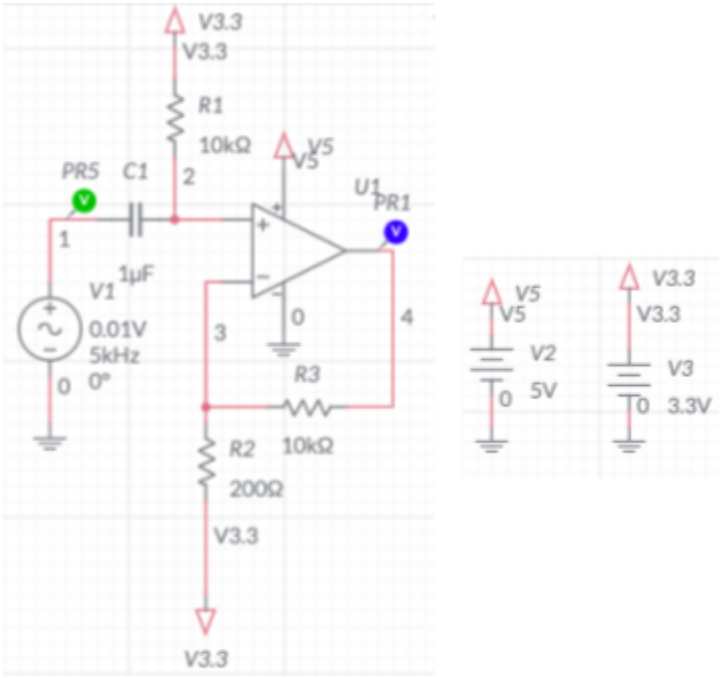


Fig. 32. Multisim gain stage simulated circuit.

Figure 33 shows the input and output signals of the circuit. Note that the input is on the order of millivolts, whereas the realistic input would be on the order of microvolts. A larger input is used to make the output easier to visualize. Note the +3.3V DC offset of the output.

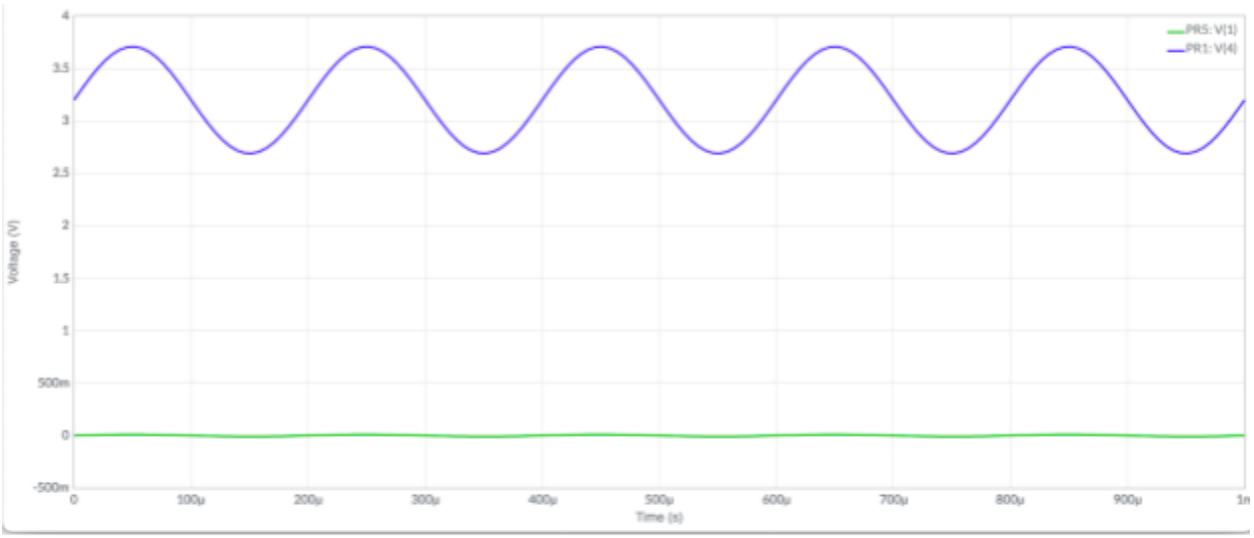


Fig. 33. Multisim gain stage simulated input and output.

A second characteristic that needed to be verified was the frequency response of the circuit. Our gain stage needed to maintain the expected gain for the entire frequency range of the input signal, which for our application is up to 20kHz. Figure 34 shows the gain stage output as the input frequency is varied. The graph shows that the circuit greatly exceeds the frequency response specification. Note that below 20 Hz, the gain of the circuit drops off. This is not a concern, as frequencies this low are not essential to the data analysis.

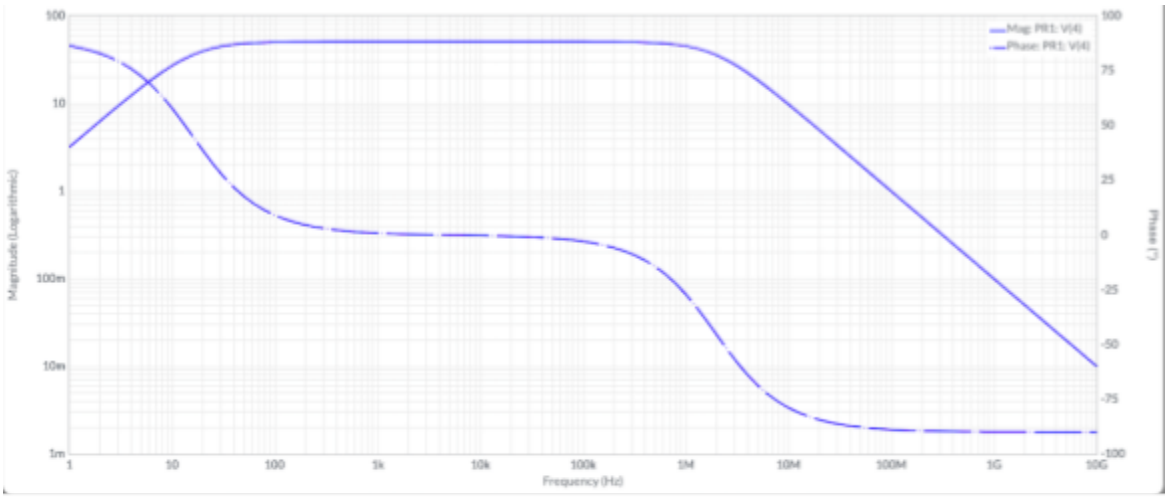


Fig. 34. Multisim gain stage frequency sweep.

5.5 Low Pass Filter

A filter is a circuit that removes unwanted frequencies from a given signal. There are various kinds of filters, denoted by what frequencies they filter and whether they are active or passive. For this project, we have used an active low pass filter. A low pass filter as a circuit that is designed to reject frequencies higher than a certain cutoff frequency. This can both come in the package of a passive or active filter. A passive filter is made up of resistors, inductors and capacitors and primarily rely on the resonance of capacitors and inductors to achieve the required values. It is relatively hard to get a passive filter to operate in general how you would want it to, due to the large capacitance or inductance that would be needed for it to properly operate. Inductance is a particular concern as well since it introduces magnetic interference within the system and can affect performance. Typically it is ideal to stay away from using inductance unless absolutely needed, such as radio frequency or power systems applications. The advantage of a passive device is that we would not have to provide biasing for the device to function. Thus, we would save costs on power consumption if we can prioritize using passive components unless the benefit of an active device outweighs the cost. An active filter is ideally used in most situations since it is much easier to control due to the transistors in an operational amplifier that enable the adjustment of the gain and therefore, change the frequency range being used by the transfer function. For our desired functions the active components will consume a relatively small amount of power. Operational amplifiers do also provide the nice benefit of helping us eliminate the need for inductors on a circuit.

The low pass filter topology being used here is that of a Sallen-Key filter cascaded with other filters. The Sallen-Key is a good topology to use because of its simplicity. Sallen Keys are a voltage-controlled voltage-source (VCVS) filter topology that uses a voltage amplifier with high input impedance and near 0 output impedance. Input Impedance is best defined as the measure of opposition to a given current, into a given load. Having high input impedance means that we receive as much of the voltage signal as we possibly can, ultimately reducing the loss of the signal so we can provide, in this case, maximum gain from the operational amplifier. Similarly, we would want “0” output impedance from the circuit to ensure that we have maximum gain from the operational amplifier. This becomes especially important in a cascaded system, since we would want the amplifiers to have as minimum loss as possible as they transition throughout the chain. Generally, if the input impedance were to be high we could “fix” it by cascading additional parts onto the circuit. Though doing this would not be ideal at all, since it would create higher costs with the increased number of ICs, complicate the circuit further & reduce layout space for either the printed circuit board (in this case) or the integrated circuit that would be fabricated on a silicon wafer. We need to have a 15 kilohertz low pass filter here to filter out everything above that range.

In order to understand the design decisions surrounding our fourth-order sallen-key low-pass filter design we will first explore the behavior of a first-order low-pass filter and then move up to a fourth-order filter. Consider the circuit in figure 35. When the

frequency of the source is varied, only the impedance of the capacitor is affected. At lower frequencies the capacitor acts as an open circuit.

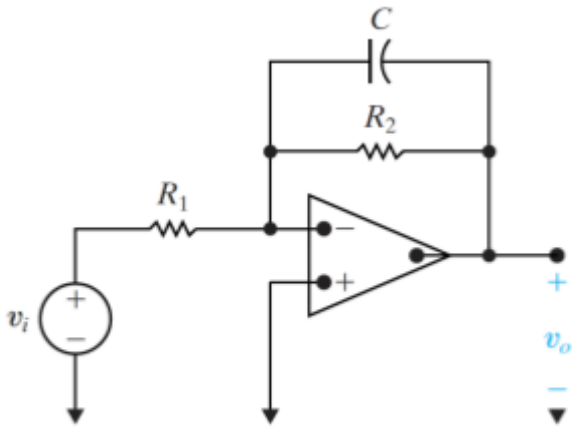


Fig. 35. Example low pass filter circuit.

The impedance of a capacitor is given as

$$X_c = \frac{1}{2\pi f C}$$

As we can see from the above equation, as the frequency decreases the impedance of a capacitor increases. Therefore, a capacitor does not act as an open circuit, but rather has a very high impedance. Recall that an open circuit has an impedance of ∞. The frequency of a DC current is effectively zero, which is why a capacitor acts like an open circuit for DC currents.

So, at low frequencies the op-amp circuit acts as an amplifier with a gain of $\frac{-R_2}{R_1}$. At very high frequencies the capacitor acts as a short circuit, which connects the output of the op-amp circuit to ground. This is why the circuit in figure # acts as a low-pass filter with a pass-band gain of $\frac{-R_2}{R_1}$.

We can also confirm this by computing the transfer function $H(s) = \frac{V_0}{V_{in}}$.

$$H(s) = \frac{-Z_f}{Z_i}$$

$$H(s) = \frac{-R_2 \,||\, (\frac{1}{sC})}{R_1}$$

$$H(s) = -K\,\frac{\omega_c}{s+\omega_c}\text{ ; where } K = \frac{R_2}{R_1} \text{ and } \omega_c = \frac{1}{R_2 C}$$

To calculate a specified cutoff frequency we can therefore use the following equation.

$$C = \frac{1}{R_2 \omega_c}$$

The above equations imply that the op-amp filter will allow us to independently specify the cutoff frequency and passband gain based on the component values used.

The cutoff frequency of a filter is defined as the frequency at which the maximum magnitude of the transfer function has been reduced by -3dB.

In order to construct a circuit with a sharper but continuous frequency response at cutoff frequency we can utilize a higher-order op amp filter.

As more filters are cascaded, the transition from the passband to the stopband becomes sharper.

In order to compute the transfer function for a cascade of n-prototype low-pass filters we simply multiply the individual transfer functions.

$$H(s)' = \left(\frac{-1}{s+1}\right)\left(\frac{-1}{s+1}\right)\ldots\left(\frac{-1}{s+1}\right) = \frac{(-1)^n}{(s+1)^n}$$

One must note that as the order of the low-pass filter is increased by adding prototype low-pass filters to the cascade, the cutoff frequency also changes.

If we are able to calculate the cutoff frequency of the higher order filters formed in the cascade of the first-order filters, we can use frequency scaling to calculate component values that move the cutoff frequency to its desired location. Once we start with a cascade of n prototype low-pass filters, we can compute the cutoff frequency for the resulting nth order low-pass filter.

For a Sallen-key filter we can choose our components for a desired cut-off frequency using the following formula

$$f_c = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

Our values were chosen such that $f_c = 15kHz$.

Figure 36 below shows the schematic for the low pass filter. The input comes directly from the gain stage, and the output goes to the analog to digital converter. The low pass filter is the final processing of the analog signal before it is digitized. The two operational amplifiers shown are only two within the quad operational amplifier package we have

used. They have shared power rails, but their inverting, non-inverting, and output terminals are unique.

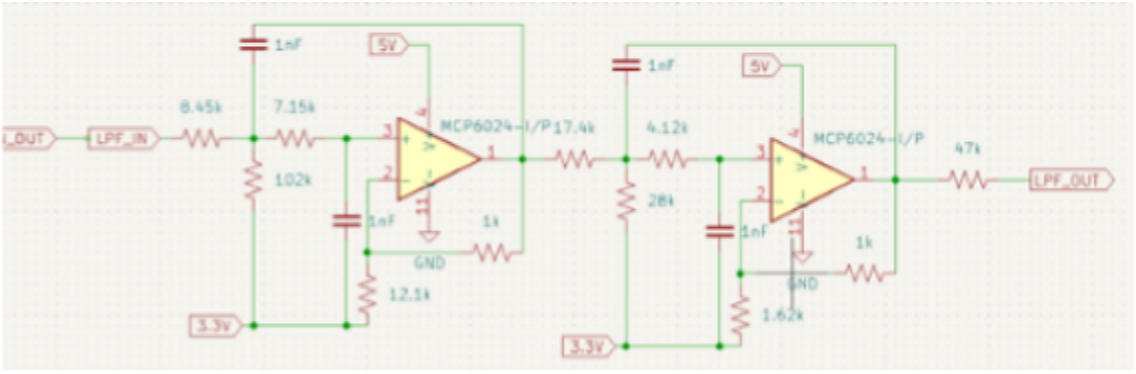


Fig. 36. Low pass filter schematic.

Multisim was used to simulate the low pass filter circuit design and verify that it was operating as desired. The primary concern was the frequency response of the circuit, so first a frequency sweep was performed. Figure 37 shows the circuit being simulated, with a single input probe and two output probes, one after each filter stage. The second output probe shows the frequency response of the entire circuit, not just the second filter stage.

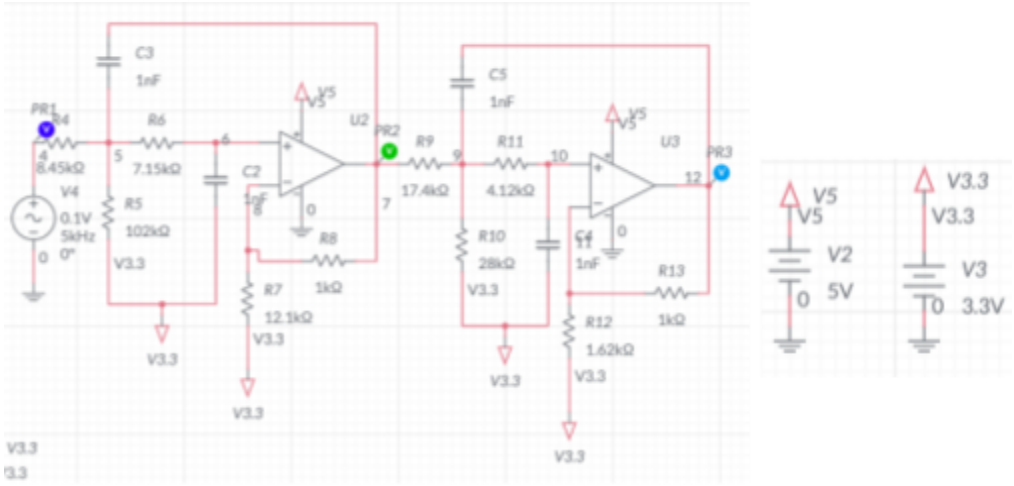


Fig. 37. Multisim low pass filter circuit.

Figure 38 shows the AC sweep for the circuit. Notice how the cutoff frequency of the first stage (in green) and the cutoff frequency of both stages combined (the blue) are identical at 15 kHz. The difference is how steep the drop-off is after the cutoff frequency. After the first stage, the cutoff is not very steep, meaning the output signal still contains quite a bit of the frequencies beyond the cutoff. After the second stage is added, the cutoff becomes much steeper, meaning much more of the frequencies beyond the cutoff are eliminated from the signal.

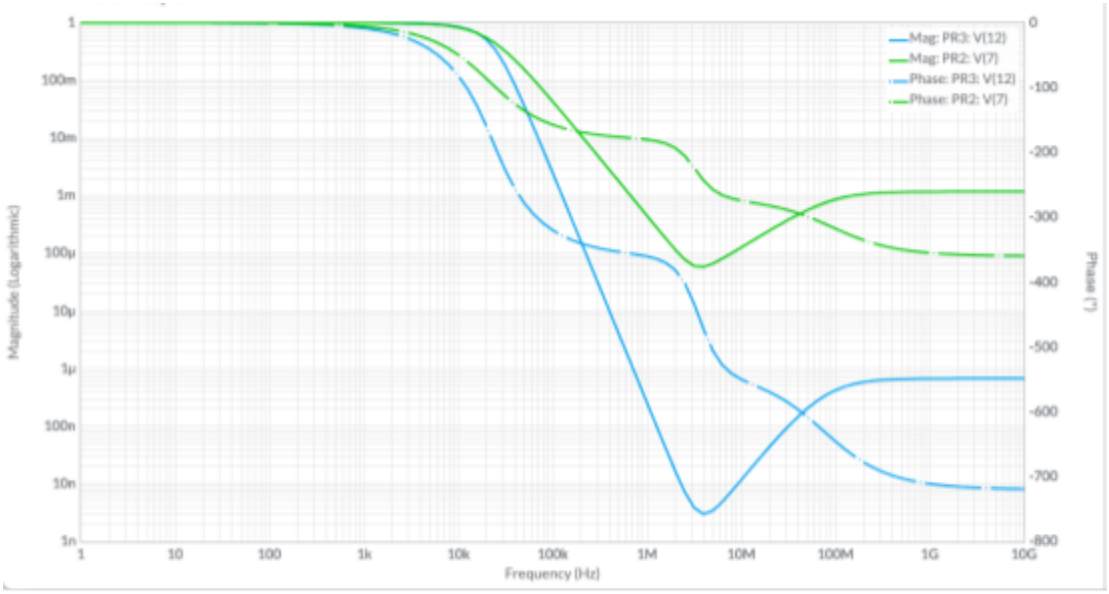


Fig. 38. Low pass filter AC sweep. The green shows the output of the first stage. The blue shows the output of both stages combined.

An example transient response will be shown to demonstrate the removal of unwanted frequencies. In Figure 39, the input signal is at 20kHz, which is beyond the filter's cutoff frequency. Notice how the magnitude of the output signal is already half that of the input signal. The output phase aligns with that shown in the AC sweep for 20kHz.

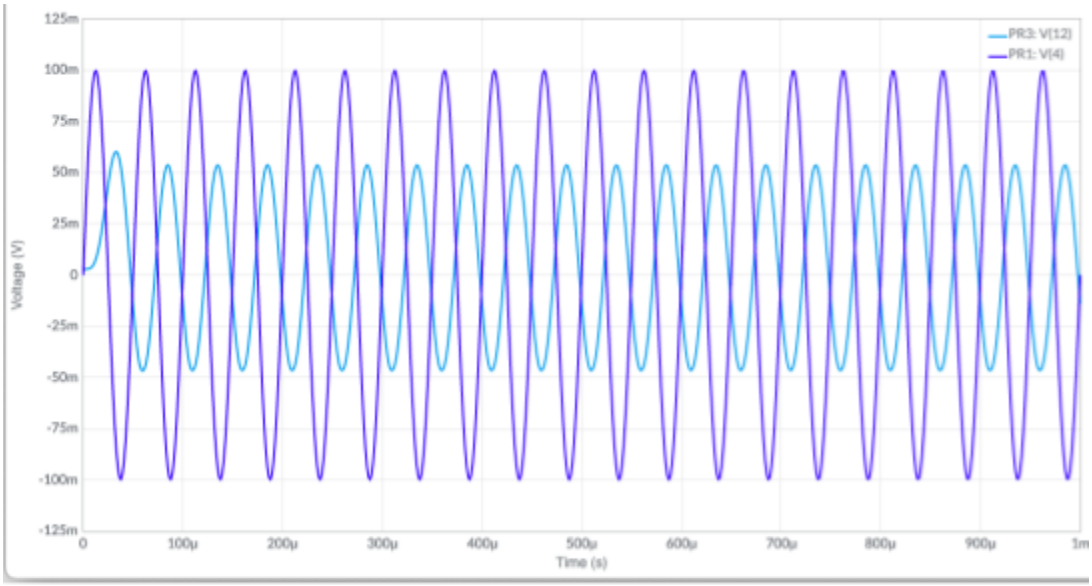


Fig. 39. Low pass filter simulated input (indigo) and output (light blue).

5.6 PCB Vendor and Assembly

For our printed circuit boards, we outsourced PCB manufacturing to JCLPCB due to their ability to provide cheap, efficient and effective manufacturing for our end product. Additionally, our team utilized the Senior Design Lab milling machine to verify the footprint of one of our components, the footprint for which was not available online.

Assembly of all components was done by hand by our team using solder, a soldering iron, flux, a heat gun and a hot plate. The assembly was straightforward for the boards included in the final prototype, as the surface mount components were all of size 0805 or larger, thru-hole ICs were used, and the ICs that were surface mount had a large enough pitch to ensure solid connections could be made by hand.

6.0 Software Design

Given that the low pass filter attenuates intermediate-frequency signals exceeding 15kHz, analog-to-digital conversion (ADC) of the filtered signal would require a sampling frequency of at least twice that of 15kHz. To satisfy this sampling frequency requirement, the filtered IF signal and sync signal were digitized by an external sound card with a sampling frequency of 44.1kHz, a 16-bit output, and a full-scale voltage of $\frac{4}{\sqrt{2}}$Vpp. Given this full-scale voltage the signal resolution is $\frac{4}{\sqrt{2}}/2^{16}/10^{-6} = 43.16\mu V$.
In our FMCW radar architecture velocity and ranging estimates were obtained by analyzing the “chirps” within a given “burst” using the fast Fourier transform. “Chirps” are composed by sweeping the TX frequency with the triangular waveform generated by the modulator, where sets of chirps comprise “bursts”. Given the modulation period of 40ms and the sampling frequency of 44.1kHz, there were 1764 samples-per-chirp. With the ADC’s sample size of 16 bits, each chirp has a size of 3528 bytes. These samples were produced by the left channel of the sound card. The composition of a burst may be visualized in Figure 40 below.

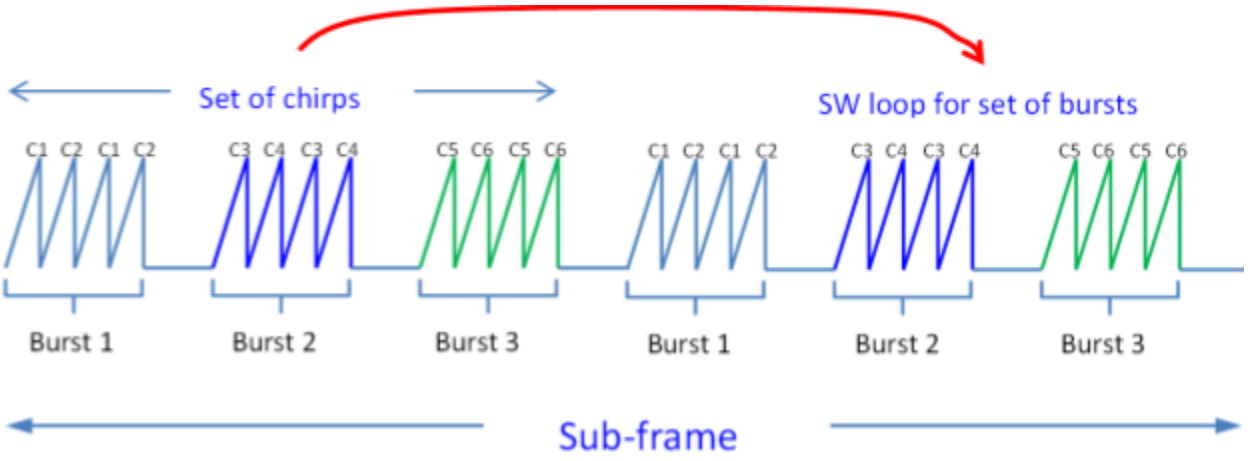


Fig. 40. Waveform of an FMCW radar burst. Credit: Texas Instruments [14].

Burst readings were acquired by activating the FMCW radar module and connecting a 3.5mm TRS jack to a computer for processing. These readings were stored in the WAV audio format to be read using two separate MATLAB programs: one for visualizing range readings; and one for visualizing velocity readings.
The ranging algorithm extracts the filtered IF signal from the left channel and the sync signal from the right channel of the audio recording. The rising edges of the sync signal were used to identify and extract the chirps from the filtered IF signal. These extracted chirps were inserted as rows into a chirp matrix. Neighboring chirps in the chirp matrix were subtracted for clutter attenuation purposes. The clutter-attenuated chirp matrix then has the inverse fast Fourier transform computed along its columns. The data in the chirp matrix is converted to the logarithmic scale by converting from V to dBV. This logarithmic data is plotted in a Range-Time-Intensity colormap as shown in Figure 41.

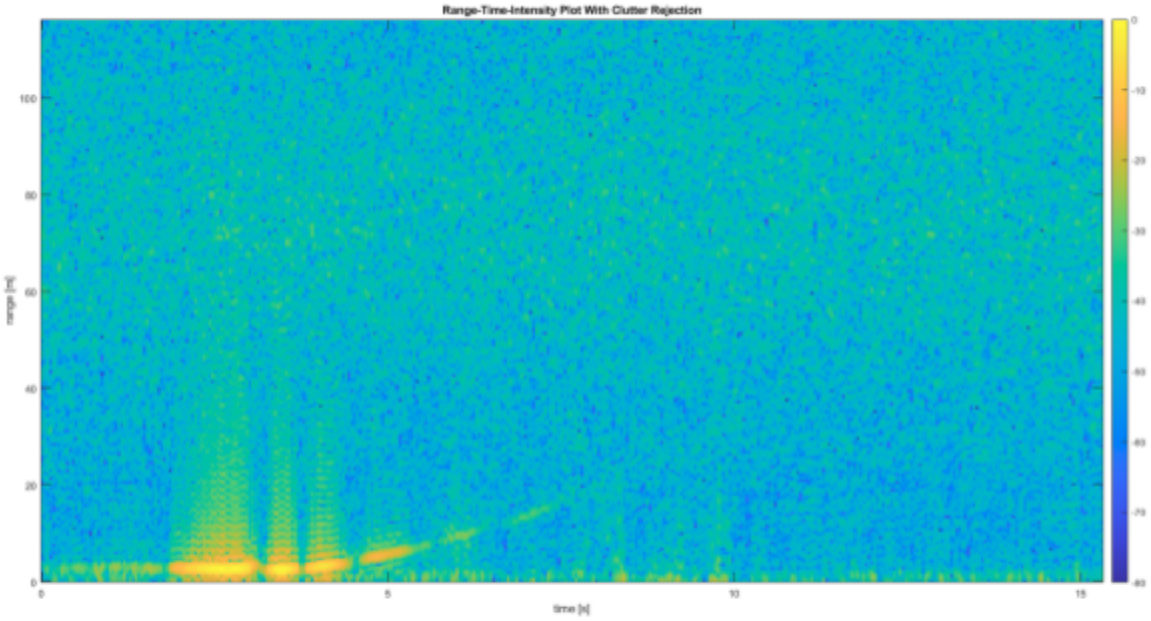


Fig. 41. Range-Time-Intensity colormap.

The velocity algorithm extracts the filtered IF signal from the left channel and the sync signal is excluded, as the data is acquired by tying the VTUNE pin of the voltage-controlled oscillator to a DC voltage. The samples-per-burst value is computed given the known sampling rate, samples-per-chirp, and chirps-per-burst. Bursts were extracted from the filtered IF signal and inserted as rows into the burst matrix. The inverse fast Fourier transform is computed along the columns of the burst matrix. The data in the burst matrix is converted to the logarithmic scale by converting from V to dBV. This logarithmic data is plotted in a Velocity-Time-Intensity colormap as shown in Figure 42.

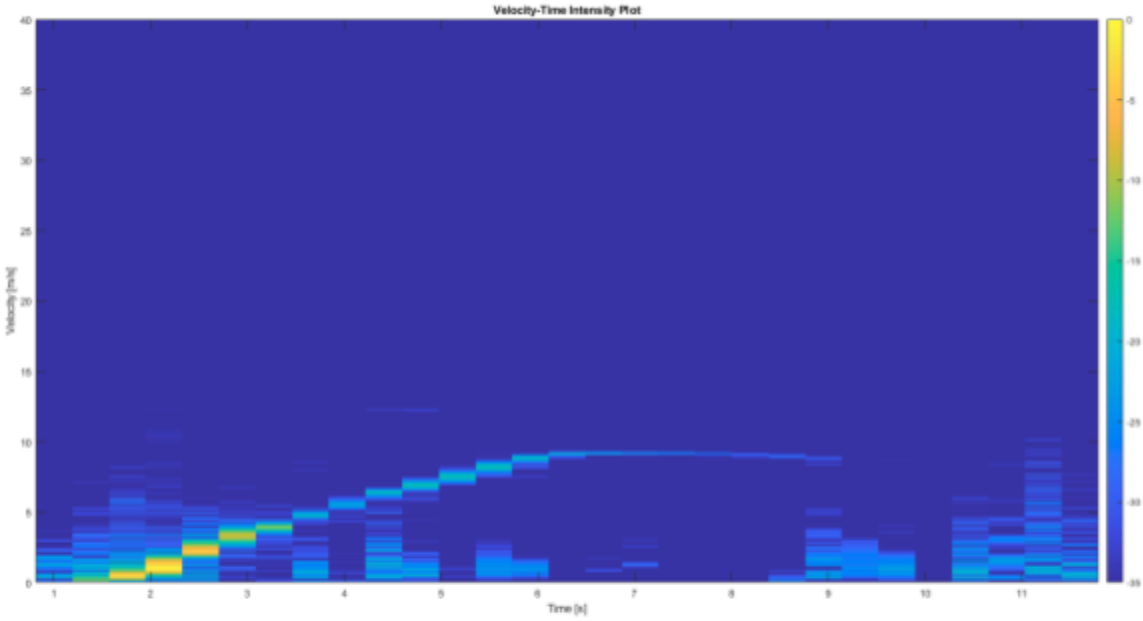


Fig. 42. Velocity-Time-Intensity colormap.

7.0 Project Prototype Construction

7.1 PCB Design Standardization

Our project originally consisted of 4 different PCBs: the power supply, the low pass filter and gain stage, the modulator and the ADC. After several design iterations, the ADC PCB was omitted, leaving 3 PCBs in our system. In order to maintain design consistency across our PCBs, a set of basic standards was outlined, which will be discussed here.

The first standard had to do with component size. Although certain ICs in our system come in only one or two package sizes, most common surface mount components such as resistors, capacitors, and LEDs come in a variety of sizes, and an appropriate size must be selected that takes into consideration the possibility of needing to test, replace or assemble the final circuits. Our team opted to use 0805 components for resistors, capacitors, and inductors. They were large enough to allow for hand-soldering, but not so large that they unnecessarily increased the dimensions of the PCBs. Additionally, because the 0805 components are surface mount (SMD), the PCB could be made smaller and were easier to assemble than if the components had all been thru-hole.

The next standard was that our PCBs had at most two layers. This design choice was primarily driven by the 2-layer limitation of the milling machine available to our team; additional details about the milling process are discussed in the next section. Though

our PCBs were ultimately manufactured and assembled by a professional supplier, it was good to have designs that could be made using the milling machine if necessary. In light of this, all of our PCB designs had two layers at most.

The next standard defined how our PCBs would be interconnected. 2.54 mm pin header sockets were used for all of our input and output signals between PCBs. Male-to-male Dupont wires were then used to connect nodes. In the case of our MiniCircuits RF components, their inputs and outputs were SMA but their power supply terminals were turret terminals, a type of connection that involves wrapping wire around the terminal and soldering the connection. To simplify the assembly process, our team chose to wrap wire around the terminals without soldering the connection. Additionally, since the gauge used to wrap the wires was thinner than the 22 gauge wire used to connect to 2.54 mm pin headers, our team had to solder and heat shrink the two wires of the two different gauges together. This left the thinner gauge wire on the component side and the thicker gauge wire on the power supply side.

Additional standards were defined for the edges of our PCB. The outer shape of our PCBs were all rectangles, with the exception of the power supply which was a composite shape made of two rectangles joined together. Mounting holes were added at the corners of the PCBs that measured 3mm in diameter. The distance between any edge of the PCBs, whether that was the outer edge or the edge of a mounting hole, had to be at least 5mm. This was confirmed using the PCB design software.

Finally, our PCB designs had to adhere to a set of requirements for trace length, component spacing and via size. The traces for our PCBs were all 0.025mm in width. The milling machine previously mentioned has spacing limitation which restricts how close components may come to traces. To allow enough space for traces to run between components, pads were all at least 1.25mm apart. Lastly, all via points were 0.8mm in diameter with a 0.4mm hole diameter. All of these measurements were confirmed while designing the PCBs in KiCAD, which allows the user to set or measure these parameters.

7.2 PCB Prototyping

In order to build a functioning prototype, we will need to mill PCBs in-house for quick testing and prototyping. We will use the Quick Circuit J5 shown in Figure 43 for this purpose.

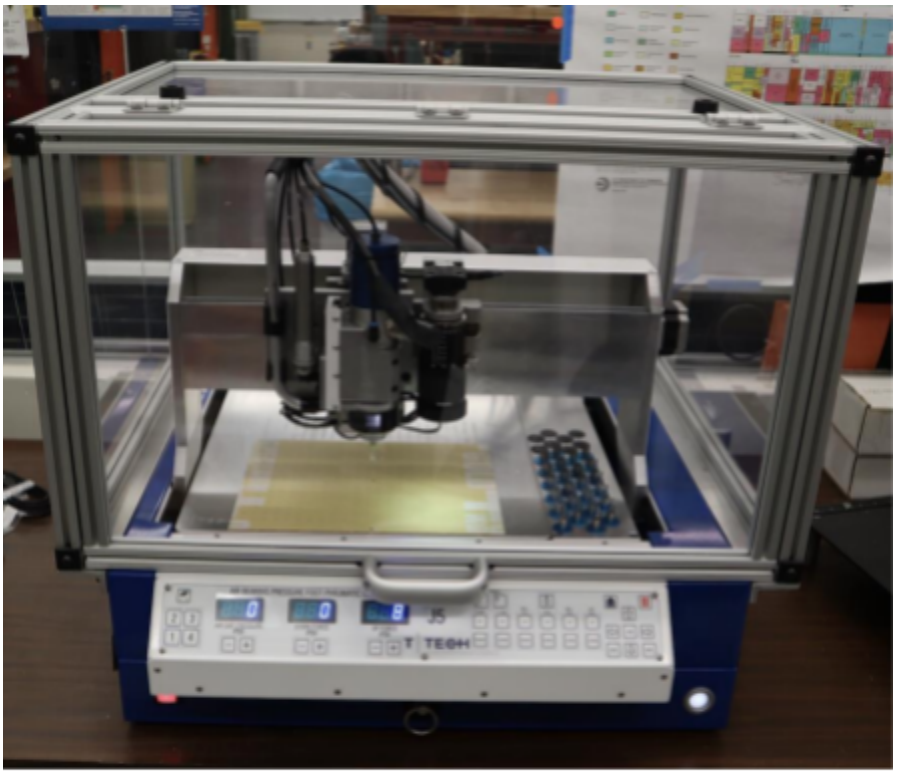


Fig. 43. Quick circuit J5 PCB prototyping machine

The Quick Circuit QCJ5 is a three axis micro-milling and drilling machine. The main purpose of this machine is to quickly create cost effective prototype printed circuit boards. This allows us to greatly reduce design-to-test cycle times. Micro-milling is distinct from conventional milling due to increased precision and damping which leads to the capability to more accurate milling paths and drill holes. This also means that the components inherently have a tighter relationship with each other. For example, a small quality issue with the spindle may have a significant negative effect on the quality of the milled part. The revolutions-per-minute is much higher in micro-milling than in conventional milling. The size of the cutting tool can be extremely small (diameter of 25 micrometers is possible). This means that the length-to-diameter ratio is often high. This increases the likelihood of tool breakage. In addition, the stiffness, attenuation, and accuracy of the micro-milling machine have a significant influence on the quality of the parts. It is also very important to constantly monitor the micro-milling process because the cutting tool can easily damage the surface of the material or break. The chip removal mechanisms are primarily influenced by the material type and its properties

followed by the tool geometry, scale of machining, and the primary process parameters (cutting speed, feed rate, depth of cut). The thickness of the removable material layer is limited; this is defined as the minimum chip thickness $\hbar m$.

Isopro is a mill-path generator and the CAD/CAM interface for the Quick Circuit QCJ5. Isopro is made specifically to be a user-friendly interface to drill, mill, route, and edit our circuit board designs. An understanding of computer aided manufacturing and Gerber files is required to use the Isopro software.

The T-Tech has a complete set of precision fine-grained carbide tools. The tool kit includes milling tools, a contour router, and various sized drill bits. We will be cutting out our prototype PCB boards on a FR-4 copper substrate board (see Figure 44). FR-4 is a composite material composed of woven fiberglass cloth and an epoxy resin binder that is flame resistant. The copper board we will be using is an 8 mil 1.0 oz 12” x 9” double sided FR-4.

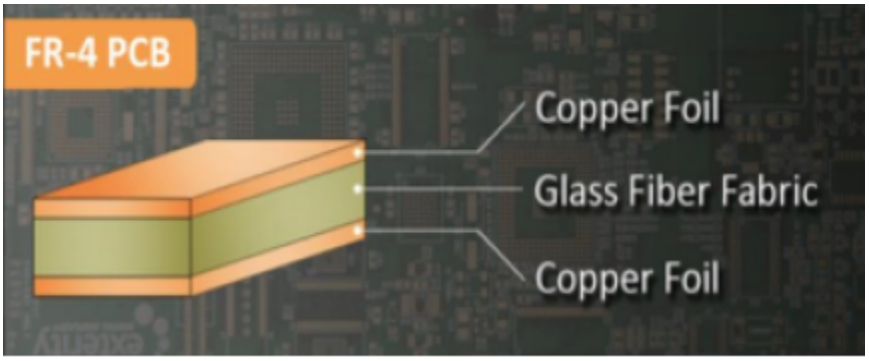


Fig. 44. FR4 Copper Substrate

The four available drill bit sizes that we carry in the milling lab as of date are 0.0320”, 0.400”, 0.0595”, and 0.125” as shown in Figure 45 from left to right respectively. We can clearly see the wide range of drill bit sizes we have at our disposal.

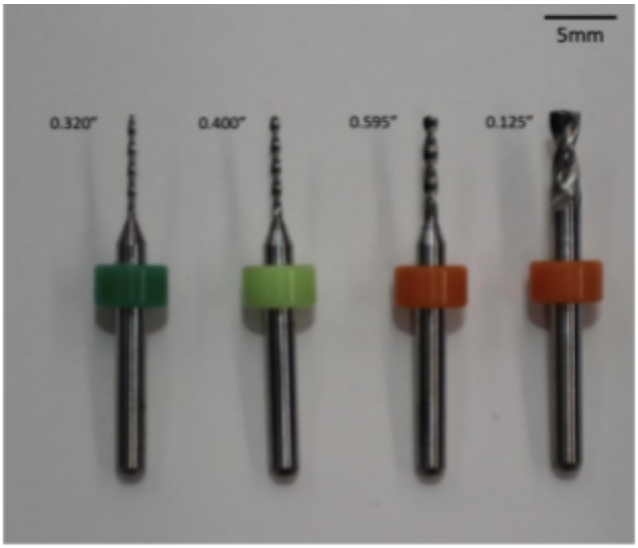


Fig. 45. Drill bits available in the lab

It is important to note the milling tool's pointed tip, as shown in Figure 46. This is significant because due to the pointed nature of the tool, we can control the width of our milled cut by the cutting depth of our tool in the negative z-direction.

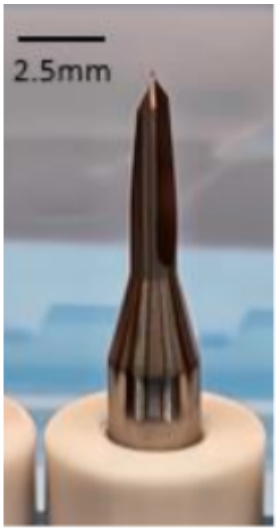


Fig. 46. T1 Milling Tool

In order to illustrate the process to go from a low-pass filter design I will provide an example of the process from a schematic all the way to a functioning prototype. In order to successfully test our design we need to be able to prototype a similar design first.

Before we use the Quick Circuit QCJ5, we must prepare the files we plan to import into Isopro properly. This will either involve converting a file from AutoCAD (*.dxf) to Isopro (.gbr) or from Eagle (.sch) to Isopro (.gbr).

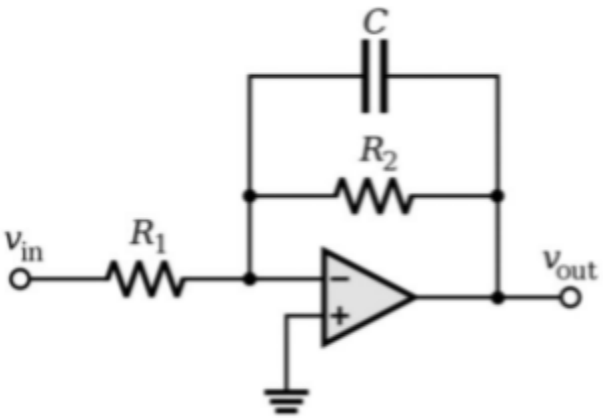


Fig. 47. Generic low-pass filter.

First, we would need to simulate the circuit in Multisim in order to confirm that the circuit will be behaving as expected. Below we verify that the design is indeed a low-pass filter by using an AC sweep.

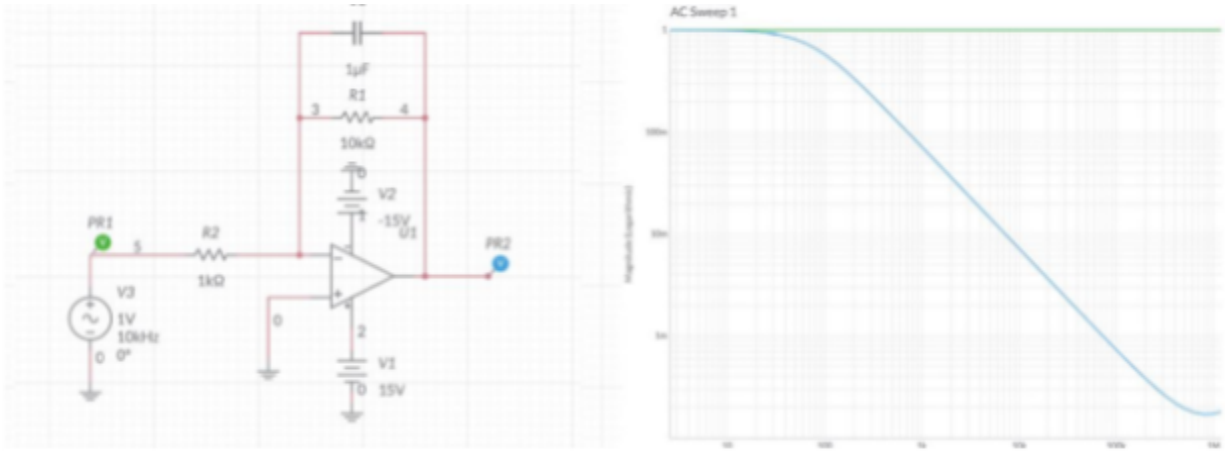


Fig. 48. Simulating the low-pass filter.

Next, we would need to design the circuit schematic in Autodesk Eagle. The LM741 op amp was used for this design.

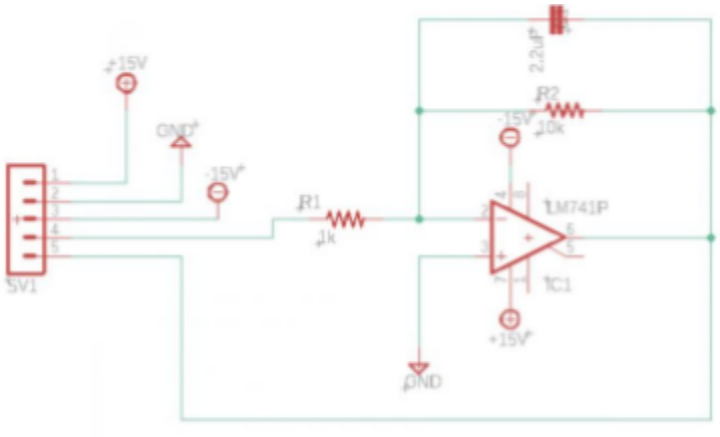


Fig. 49. Circuit design in Eagle.

Next, we proceed to convert the low pass filter design in Eagle to a .brd file. After arranging the board as desired, it should look like Figure 48. For more detail of how to correctly create the low-pass filter, reference the week 3 document for EEL 3926L.

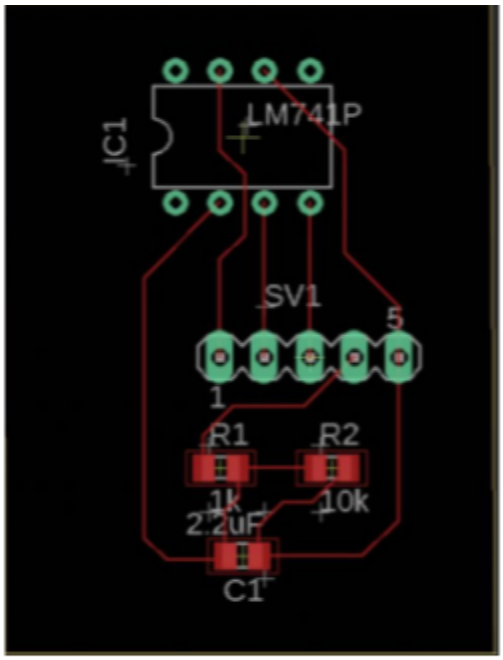


Fig. 50. Circuit in board form.

Once we have a satisfactory board layout that has passed the ERC check, we can now select File > Cam Processor > Process Job.

Now that we have properly prepared our design for importation into Isopro, we are now ready to start using the Quick Circuit J5 and Isopro to mill our design to completion.

Now that we are ready to use Isopro to prepare our design for milling we first will open Isopro on the computer in the milling lab. We should see the opening screen as shown in Figure 51.

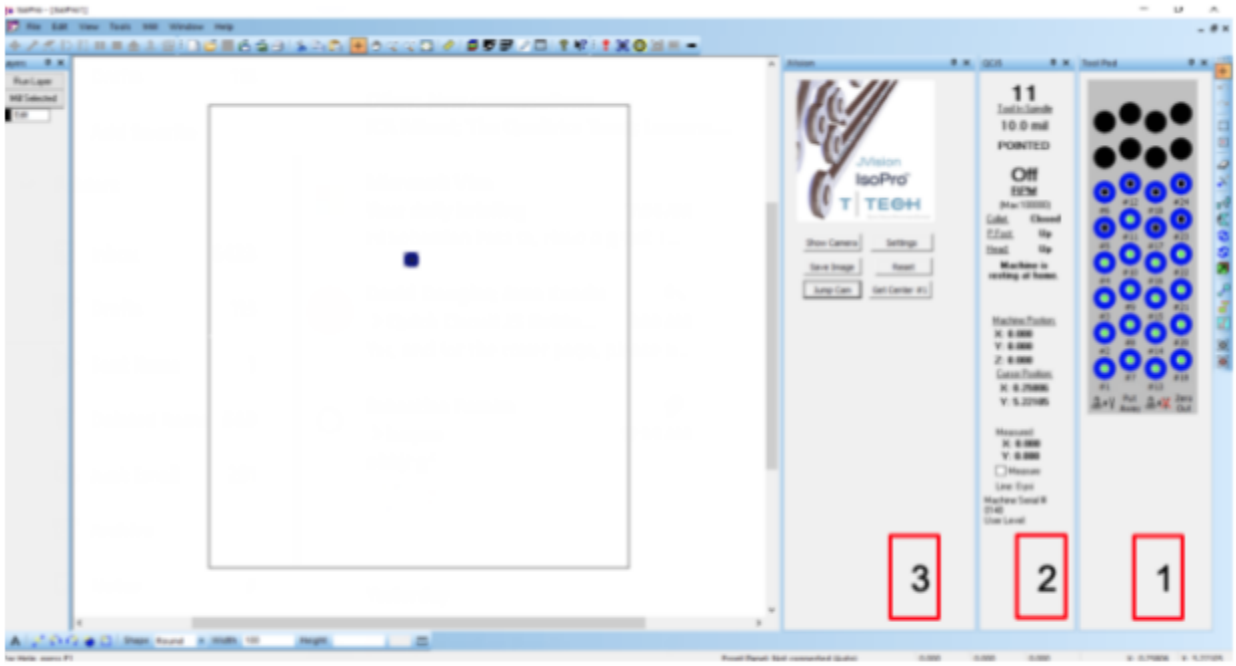


Fig. 51. Isopro home screen.

Once we are at this home screen we can go ahead and select “Mill” > “Initialize”. The Quick Circuit J5 should now initialize itself and place the spindle over the home position. While the machine initializes, let us quickly go over some of the prominent features that we see on the Isopro home screen. The tool pod, informational window, and camera window are marked by the numbered boxes from 1 to 3 respectively.

After opening Isopro, we can now select File > Import > Auto-Detect File(s), and select the Gerber files associated with our board. We can now see our board layout in Isopro.

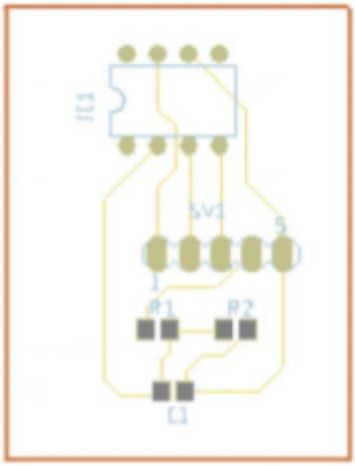


Fig. 52. Low pass filter opened in Isopro.

We next need to change the layer where the holes should be to a drill layer. We should now see the drill icon where the pins of the op-amp should be. It is useful here to hide any unnecessary layers to have a smooth workflow.

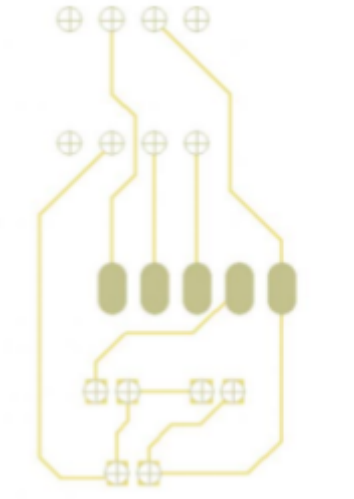


Fig. 53. Drill holes added.

Notice here that the Isopro does not insert drill holes for the 5-pin header. After testing multiple types of pin headers, it seems like Isopro does not register the holes needed for pin headers. We will have to put in the holes manually here. The most efficient way to do so is simply copy the holes created for the op-amp and place them where the holes for the 5-pin header should be. We also need to delete the drill holes that are located where the resistors and capacitors will be placed, as we will be using surface mounted components. We also need to delete the solder pads located on the 5-pin header.

Fig. 54. Drill holes added to 5-pin header.

Next, we want to isolate the copper_top.gbr layer (yellow layer). I have selected a 10-mil isolation. We then will hide the original layer leaving only the isolated layer (green). We can also create our board outline by creating a new layer and then using the rectangular tool. Our filter in Isopro should now look like Figure 55.

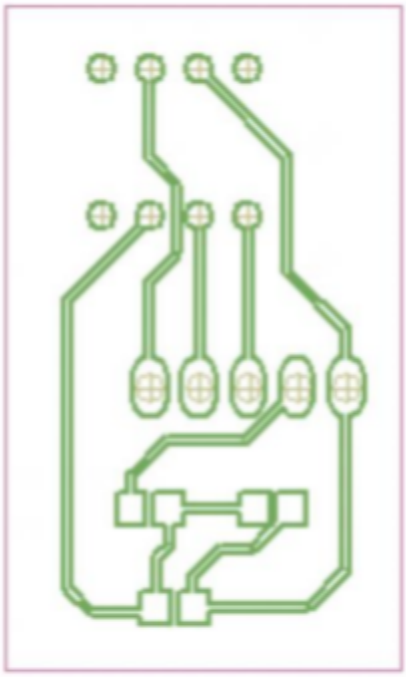


Fig. 55. Isolation created for components.

We now need to position the board in the desired location. Put the target over the circuit and do a material height check. Be sure to use the “Jump to Cursor” function described in the last section to make sure that the design is within the bounds of the copper board.

We are now ready to run our layers. At this stage insert the drill bit into the collet. We will first run the drill layer. Once you reach the “Manual Tool Change” window, simply press the “OK” button. For the depth of cut, we will set the drill to about 2 mm which is around 78 mil. We now can run our isolation layer. We will unload the drill bit and the QCJ5 will automatically pick up the milling tool.

Now we can proceed to cut out our board using the tool cutter located to the right of the Quick Circuit J5 and place our components. In order to guide our PCB design creation it could be useful to understand the limits of the milling machine. Notice the milled copper traces shown in Figure 56. It is important to observe how the pointed tool behaves as it cuts through the material. The figure demonstrates the up-milling face (highlighted by the red arrow) and the down-milling face (highlighted by the green arrow), where the direction of the feed is shown by the magenta arrow, where “f” is the feed rate, “a_e” is the width of cut, and “h_m” is the average chip thickness. As the tool moves forward while rotating clockwise, the cutting lip will engage the material. This begins the formation of the chip with a chip load of zero. As it moves forward the chip load increases until it reaches the center of the crescent. The tool then decreases its chip load back to zero leaving the green portion of the crescent (down-milling) minimum quality copper trace width that we can make with our currently available tools which is approximately 125µm. The red and green arrows correspond to the up milling and down milling respectively. The magenta arrow depicts the motional direction.

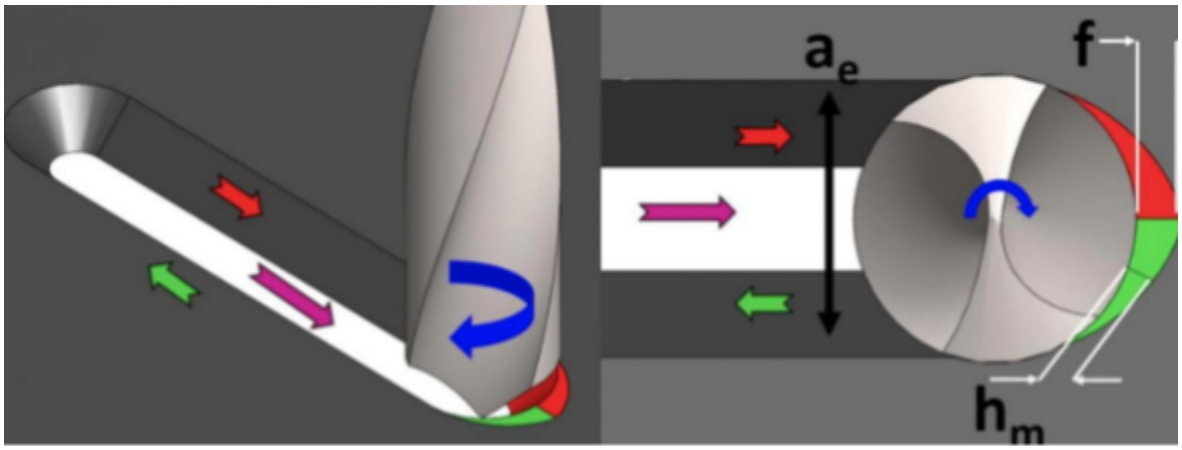


Fig. 56. Illustration of milling in detail.

Fig. 57. Highest resolution of the Quick Circuit J5.

7.3 Power Supply PCB

The power supply PCB includes the following elements: electronic components (those discussed in the hardware design section), 9V battery pack holders, and female pin headers. The electronic components were organized into three identical blocks, as the circuits for all three supply voltages are physically the same and operate in parallel. The PCB incorporated four 9V battery pack holders arranged side-by-side. These holders were through-hole components, so the positive and negative terminals of each battery were electrically connected to traces on the PCB, eliminating the need for additional jumper cables or wires.

Finally, the PCB includes 2.54mm female socket headers. There were a total of 25 headers, arranged into one four by six block plus one additional header. Each row in the four by six block corresponds to a certain voltage level generated by the circuitry, these being ground, +3.3V, +5V and +12V. Six pin headers were used for each voltage because the voltages must be sent out, via male-to-male Dupont wires, to all electronic components in the system that require a power supply. Each supply voltage level does not necessarily have five components connected to it, but having more headers than necessary allows for additional capabilities to be added if desired. Additionally, the last single header is used for the enable signal. This signal was originally a digital signal from the MCU that would control all three EN pins in the power supply circuit, therefore only one pin header was needed.

Figure 58 below shows a close-up 3D rendition of the power supply PCB and a photo of the power supply with batteries inserted. Drilled in the PCB were six holes per battery holder, four for mounting and two for the thru-hole leads. Two additional holes were added near the female header pins for mounting the PCB to the radar module. Note that each voltage level has its own indicator LED, which indicates if the circuit for that corresponding voltage is activated or not.

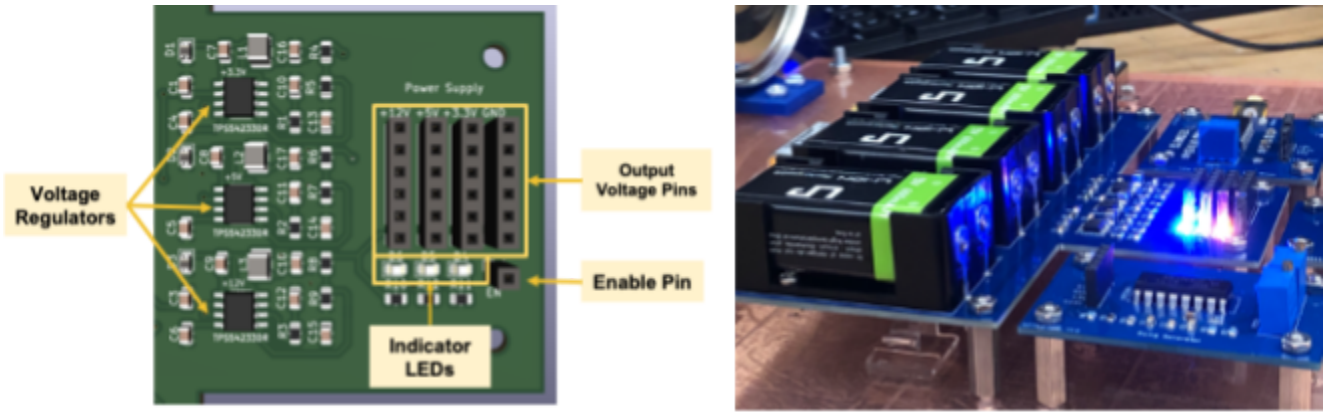


Fig. 58. Left: Power supply PCB 3D rendition.
Right: Power supply with batteries inserted.

7.4 Modulator PCB

Our modulator PCB consists of the electronics for the modulator circuit and a row of pin sockets for the input and output signals. The modulator device is a thru-hole component. The potentiometers were thru-hole as well (Bourn 3299 packages), and their resistance is adjusted by a small screw at the top of the package. Holes were added at the corner of the PCB to allow for mounting on the radar module. Figure 59 below shows a 3D rendition of the circuit board.

The five in sockets have been labeled independently for this PCB. This is because each socket is a different signal or voltage level, unlike in the power supply PCB where all sockets in a row were the same node. Note that the +12V power supply pin must be disconnected from the power supply to use the radar for velocity measurements.

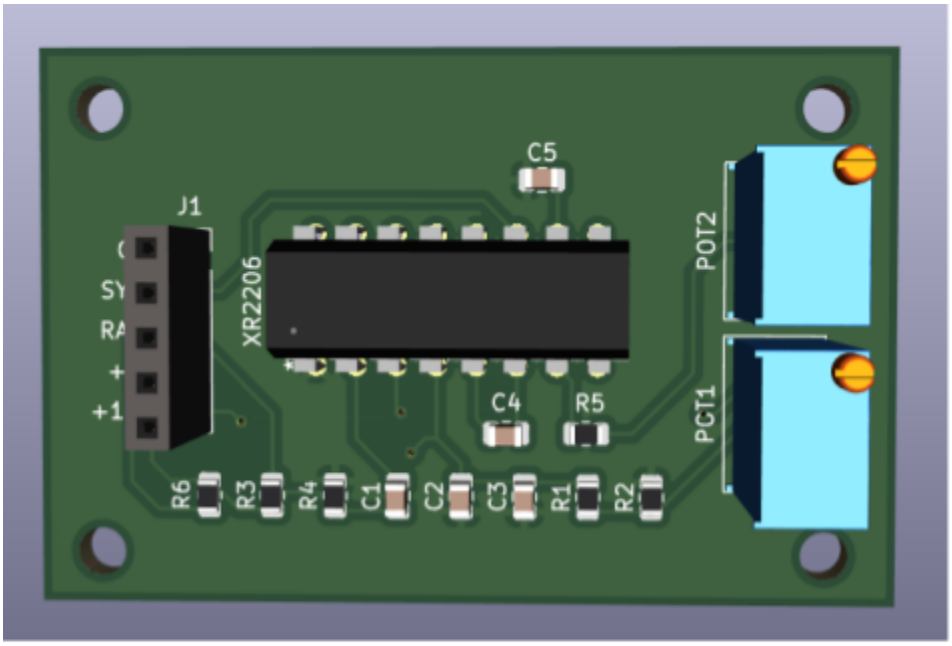


Fig. 59. Modulator PCB 3D rendition.

7.5 Gain Stage and Low Pass Filter PCB

The gain stage and low pass filter were combined into a single PCB. The primary reason for this is that the MCP6024 IC includes the operational amplifiers needed for both circuits. The PCB includes all the circuit elements, one row of pin sockets for the input voltages and a single pin socket for the output signal. One important difference between this PCB and the others is the inclusion of an SMA connector. The input to the gain stage, which is the input to this PCB, is coming from the mixer. The mixer's ports have SMA female connections. The easiest way to connect the mixer's output signal to the PCB would be with a male-to-male SMA cable. In order to do this, a female SMA connector was integrated onto the board.
Figure 60 shows the cross-section of an SMA connector. On the left, there are three distinct metal pieces: the top, the bottom, and the middle. The top and bottom pieces (equivalently, the outer pieces) are the ground leads. The middle piece is the signal lead. When assembling into the board, the two outer pieces were soldered to pads that were connected to the ground plane. The signal lead was connected to a trace that feeds into the gain stage electronics. The SMA connector used for our PCB is a horizontally-oriented female SMA connector.

Figure 61 shows a 3D rendition of the low pass filter and gain stage PCB. The only missing element is the SMA connector..

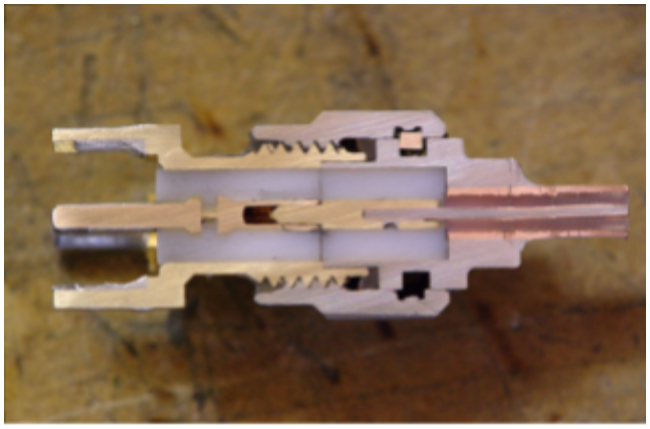


Fig. 60. Cross-section of an SMA connector.
Credit: TubeTimeUS.

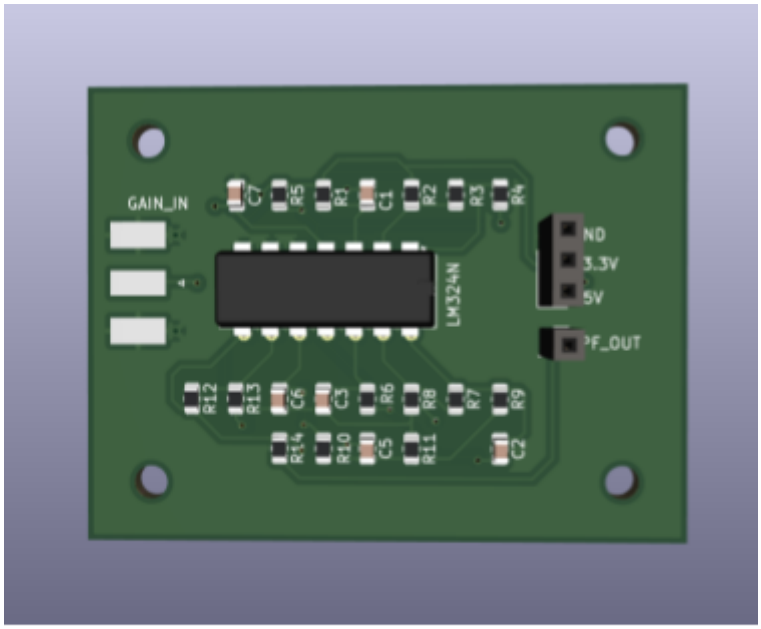


Fig. 61. Low pass filter and gain stage PCB
3D rendition

7.6 Antenna Fabrication

For our project, we used a circular waveguide antenna, with a used coffee can. The dimensions of the can is 5.25'' in length, 3.9'' in diameter. We drilled a hole into the can, about 1.8'' from the back wall of the can, into which a monopole antenna in the form of a 1.2" wire will go. The wire itself will be soldered into a female MSA connector. So long as the connection is solid (meaning no gaps or spaces between the can, the connector and the wire), this antenna assembly is able to send out the RF signal generated by the active RF circuits.

The significance of the circular waveguide antenna is that it helps redirect power in terms of the can based waveguide at the target of interest. The wire based monopole antenna will have radiation around the piece. When we placed this antenna within the antenna, the direct radiation and the reflected radiation are both sent out from the antenna from a quarter wave length at the metal wall. This helps enhance the radiation pattern.

8.0 Project Prototype Testing Plan

8.1 Required Equipment

There were several pieces of equipment that were necessary when testing our subsystems. Each piece of equipment either acts as an input to our system, measures an output of our system or simply measures characteristics of components. Calibrated lab equipment is necessary to verify that our subsystems were operating as desired.

8.1.1 Multimeter

The first piece of equipment needed is a multimeter. A multimeter is a device that can be used to measure several different parameters including DC voltage, AC voltage, capacitance, resistance, and current. The most important function of the multimeter is voltage measurement, as the voltage at different points of our circuits are known and should be at a certain level for the circuit to operate correctly. Multimeters will also be used to verify that our components have the correct characteristics. Circuit elements such as resistors and capacitors come with a nominal value, but their actual value can and should be measured. This helps better understand the operation of the constructed circuit, which will deviate at least slightly from the theoretical performance.

Multimeters were used during our PCB testing process. One of the biggest issues in circuit design is lack of connectivity, which is when two points are not connected when they should be. Using a multimeter helped verify that all points that should be connected were actually connected.

We primarily used the HMC 8012 Digital Multimeter that is available in the senior design lab. This multimeter is highly accurate and highly reliable. Handheld multimeters were used as well.

8.1.2 Spectrum Analyzer

Spectrum analyzers are especially useful in RF system testing. They can display the frequency spectrum of an RF signal, which is the graph of the frequencies present in the signal versus the magnitude of each frequency. Spectrum analyzers combine the dynamic range swept with vector signal analyzer capabilities. This in turn allows enough information to do tasks such as error vector magnitude, which is a measure of how accurate a wireless system can be seen. Much like circuit element nominal values, these parameters are often stated in a component’s datasheet, but it is a good idea to

verify them. All components will have characteristics that vary slightly from the designed nominal value.

For RF testing we used an R&S®FPC1000 Series Spectrum Analyzer. This device offers high-performance spectrum analysis up to 3GHz.

8.1.3 DC Power Supply

DC Power Supplies are used to generate constant voltages for use as inputs to a circuit. In our test procedures, DC power supplies take the place of batteries. The voltage generated by a power supply such as a battery will eventually decrease as the supply is used, so a DC power supply is used in a lab setting to ensure the voltage is constant. In our project, DC power supplies are used to generate the power needed for our active filters and create a DC offset for the circuit outputs.

Like many pieces of lab equipment, one primary advantage of using a DC power supply is the ability to quickly and easily generate different voltages for application to the circuit being tested. It may be advantageous to test different power supplies for a circuit to determine which one creates the best output signals. If batteries were used, not only would the voltage not be constant, but the voltage levels available would be limited to integer multiples of the voltage for an individual battery. It would be a hassle to have to generate additional voltages for testing purposes.

We used the Keithley 2230-30-1 Triple Channel DC power supply. The Keithley power supply provides two channels capable of producing up to +30V and up to 1.5A; with one additional channel capable of producing up to +6V. Each channel can be independently controlled to be on or off at any time. To aid with device-under-testing (DUT) the device has a timer capability that allows us to set up unattended tests that turn off the channels after a programmed time-interval. A USB can also be connected to facilitate instrument control, data logging, and analysis.

8.1.4 Oscilloscope

An oscilloscope is a device used to measure output voltages from a circuit. An important characteristic of the oscilloscope is that it can measure both the time domain and frequency domain versions of a signal. In the time domain, an oscilloscope is used to display and measure the shape of a signal. For a DC signal an oscilloscope would simply show a straight horizontal line in the time domain and a straight vertical line in the frequency domain. In this case, the device acts more like a multimeter. For AC signals, the oscilloscope allows the user to view the period and frequency composition of the signal being analyzed. There are a plethora of useful features on an oscilloscope, such as cursors for measurement, multi-signal computations, and the ability to toggle between AC and DC coupling, which either ignores the DC offset in a signal or leaves it in, respectively. For our applications, the oscilloscope is used to verify the gain of our gain stage, the frequency response characteristics of our low pass filter, and the signal shape generated by our modulator.

We used the Rohde & Schwarz RTM3004 Oscilloscope. This device not only provides us with an oscilloscope but also with a logic analyzer, protocol analyzer, and digital voltmeter. This allowed us to quickly and efficiently debug our electrical systems. We were also able to do logic-based testing with this device, which helped test our ADC circuit.

8.1.5 Function Generator

Function generators can create output signals of various shapes, frequencies and amplitudes. These signals can be used as input signals for our circuits during design verification. Nearly every circuit in our design modifies an input signal in a certain way; it does not just generate a signal. However, if each circuit required the output signal from the previous subsystem in order to be tested, we would have to verify the functionality of each subsystem in a sequential fashion, which would be a very lengthy process. Alternatively, we choose to use the function generator to simulate the output signal from the previous subsystem. Another advantage of initially using a function generator rather than using the output from the previous system is that the signal from the function generator can be easily modified. At the press of a button, the frequency, magnitude or shape of the signal can be changed to acquire a better understanding of how the circuit being tested operates. A more complete idea of the circuit performance can be developed this way.

We used the Tektronix Dual Channel Arbitrary Function Generator. The AFG3022B has 2 analog channels and has a 25MHz bandwidth. It has a maximum output frequency of 25MHz. Its maximum amplitude is $20V_{pp}$ into 50Ω. It also has a USB port on the front panel for waveform download.

8.2 Hardware Specific Testing

Hardware testing is to be programmatically implemented using Python and the “pyvisa” library that serves as a wrapper for the NI-VISA application programming interface. NI-VISA allows for communication with test equipment such as the network analyzer, DC power supply, function generator, and oscilloscope via USB or GPIB. By leveraging the capabilities of NI-VISA it is possible to issue SCPI commands to these devices, which allows for the setting of values and getting of measurements. By interfacing with these devices in this manner it allows us to design tests that require minimum interaction beyond initial composition while accumulating relevant data samples as quickly as possible. These tests will be verified against simulated data wherever possible.

8.2.1 Transceiver Test

Required equipment for executing the transceiver test would include the following: a spectrum analyzer to determine how much power is output in the receiver and the

transmitter; 2 DC power supplies to properly bias the VCO and LNAs and to perform a DC Sweep of the Vtune pin on the VCO; and a multimeter for continuity testing to ensure that none of the components are shorted and are properly getting biased to make sure the components are generating or amplifying the high frequency signal. The specific points of interest are shown on Fig. 63.

To test the radio frequency (RF) frontend, we must prepare the spectrum analyzer and connect the coaxial cable from it to our target of interest. We would also like to use a calibrated torque wrench to tighten the SMA connections from the spectrum analyzer to our ports of interest, for discontinuities that could occur when mechanically connecting it. This is important to ensure the test setup is repeatable to whomever is given to test this. Leakage is an important test consideration because of that, since specific components must be under a similar environment of what they would be when actually used.

Testing of active RF circuits is not a trivial matter and is a fundamental skill for those looking to be well-versed in RF test and design. All the theory in the world will not help us if the high frequency circuits that we may be testing do not work as we would like. One of the most important tools for high frequency testing is a spectrum analyzer. This device will allow us to measure the power seen through the components.

Spectrum analyzers are important devices for high frequency testing, especially when a vector network analyzer (VNA) is not available for usage. Commercial grade VNAs roughly cost at a starting price of $8,000, and require calibration procedures that may be complex to newcomers in the field. A few popular calibration techniques to prepare a VNA for testing are SOLT calibration & TRL calibration. SOLT calibration makes use of 4 different calibration tools rated for the frequency range of operation; short, open, load & through components that must be connected to the end of the coax cable. These kits also cost around $3,000, especially if we are going to the GHz range. TRL calibration is significantly cheaper, costing maybe $30-$60, but this would require us to design distributed element quarter wave transformers that would have to be matched to each specific component. These parts would also have to be chemically etched or machined. The software for this is accessible through the university by the means of Cadence ADS, but the risk of having reliably tested parts along with fabrication & inconsistencies from the actual product far outweigh the benefits.

For our spectrum analyzer, we must ensure that the target signal passes above the noise floor set by the RF attenuator. This signal is measured in dBm (power in miliWatts), because of its ability to measure large and small values in a more condensed format. Another benefit of using the log scale is the ability to add and subtract power instead of multiplying or dividing from cascaded systems as we see here. The tools used in our test setup come from the Senior Design Lab.

Fig. 62. FSUP 3GHz Spectrum Analyzer.

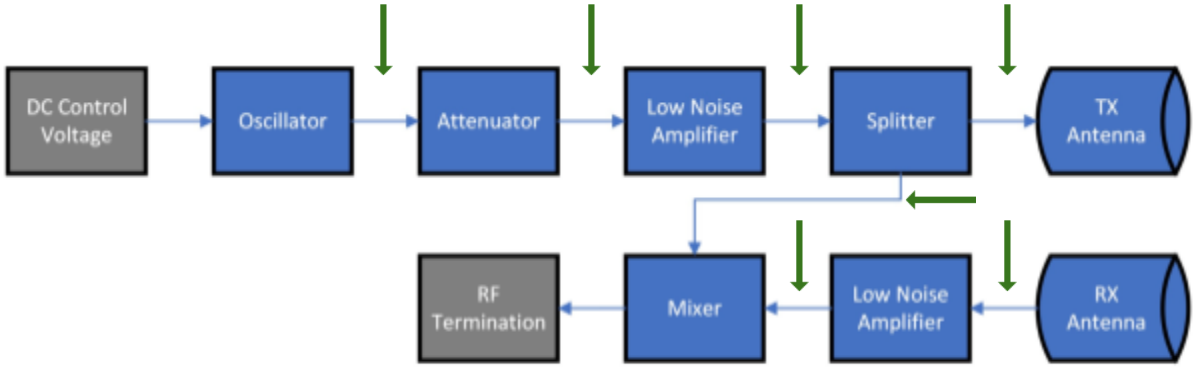


Fig. 63. Direct Conversion diagram for FMCW Radar.

8.2.1.1 RF Transmitter Testing

The transmittering system has a relatively straightforward testing procedure, on our RF front end we will disconnect the coax from the transmitter antenna from port 1 of the RF splitter and connect the coax from the spectrum analyzer to part one. We will of course make sure this connection is well fitted, given the possible issues that can arise as described previously. We will then connect the bias wires to the LNAs & VCO on the RF frontend. Next, we will connect the bias wire to the Vtune to help us perform the DC sweep on the oscillator. Once we turn everything on, the DC biasing for the power supply will be at 5 volts and then the Vtune will be swept through a range of 2V to 3.2V, in .2V increments.

The purpose of us testing the Vtune, is to ensure the power output remains relatively constant at 12 dBm as we shift frequencies in the ISM band (2.4GHz to 2.5GHz). We expect to operate between 2.4GHz to 2.49GHz based on our design requirements.

8.2.1.2 RF Receiver Testing

Similarly the testing of the receiving system has a similar setup. We will disconnect the coax from LNA2 that was going into the receiver antenna and connect the coax going

into the input of LNA2. Biasing will be applied similarly as described previously for only LNA1 and VCO, and same with the VCO pin of Vtune. We will sweep the Vtune pin from a range of 2V to 3.2V in .2V increments. A static velocity target with no velocity will be used as well, to see how much power is reflected back to the receiving antenna.

The receiving LNA should get a predicted power measurement of -22.6dBm. This will not be perfect and can have a decent margin of error based on what signals the antenna could potentially pick up outside of just the reflected transmission signal itself.

8.2.2 Power Supply Test

The power supply has two +9V alkaline batteries in parallel that are connected in series with another two +9V alkaline batteries in parallel. This arrangement allows for approximately 1200mAh of charge as well as two nodes at +9V and +18V. The +9V node is supplied to two separate buck converters that regulate the voltage to +5V and +3.3V, whereas the +18V node is supplied to a buck converter that regulates the voltage to +12V.

To test the power supply, fully charged batteries were inserted into all 4 battery holders. A multimeter was then used to verify that the proper voltage was being output by the +3.3V, +5V and +12V circuits with respect to the PCB ground. Additionally, a programmable load was used to verify that the circuit was capable of delivering the required amount of current. The load was connected to each circuit in turn and then programmed to pull the current level for each voltage (for instance, 200 + mA for the +5V circuit). Preliminary tests of this nature revealed that components had been selected that had current ratings too low for our application. The team was then able to select the correct components.

8.2.3 Modulator Test

To test the modulator we must first ensure that all of the components have been assembled properly onto the circuit and verify that there are neither short nor open components. The Keithley 2230-30-1 Triple Channel Power Supply must then be connected and turned on for DC biasing. The biasing for our XR- 2206 Waveform generator was +12V.

In order to generate our desired waveform within our low-frequency circuit design we needed a waveform generator. We chose the XR-2206 for this purpose. The XR-2206 is a monolithic function generator integrated circuit that can produce multiple waveforms such as sine, ramp, pulse, and square waves with both high stability and high accuracy. The amplitude and frequency of the waveform can be modulated with an external voltage. Instead of directly modulating the voltage we can use potentiometers to change the resistance within the circuit. The oscillator has a maximum frequency of 1MHz and has a sweep range of 2000:1.

We were able to physically test our modulator section of the low-frequency design using a breadboard, as shown in Figure 64.

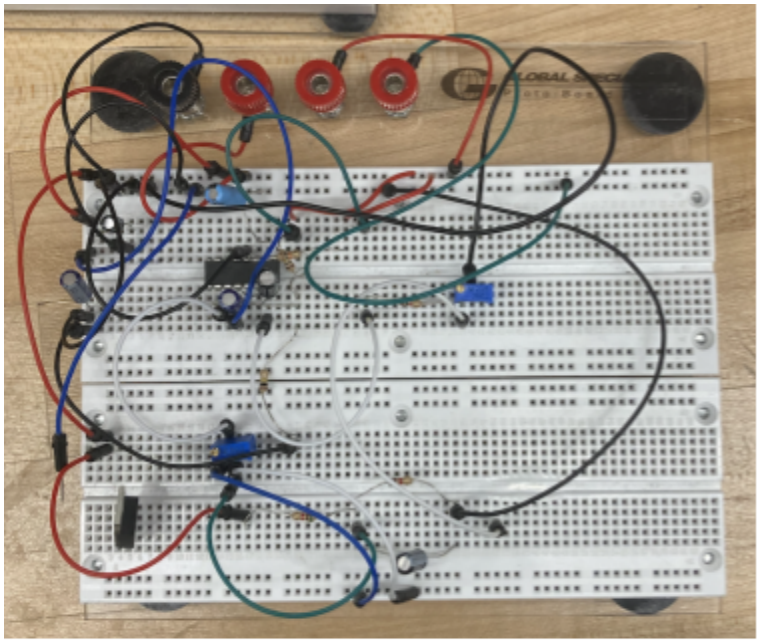


Fig. 64. Waveform generator testing.

After tuning the circuit by adjusting the potentiometers we were able to see the exact output of desired; as shown in Figure 65. The period of our generated ramp was 40ms as designed. The behavior of the ramp output was characterized by issuing SCPI commands via the NI-VISA interface. A USB2.0 Type A to USB2.0 Type B cable connected the oscilloscope to a computer, which issued SCPI commands that did the following: scaled the display to fit 10 ramp periods; set the trigger to the rising edge; and acquire the data points present on the display. Then using SciPy and PyPlot the time domain and frequency domain representation of this signal is compared to the ideal ramp waveform with a period of 40ms. These results can be seen in Figure 67 below.

Fig. 65. Ramp output of modulator with a period of 40ms.

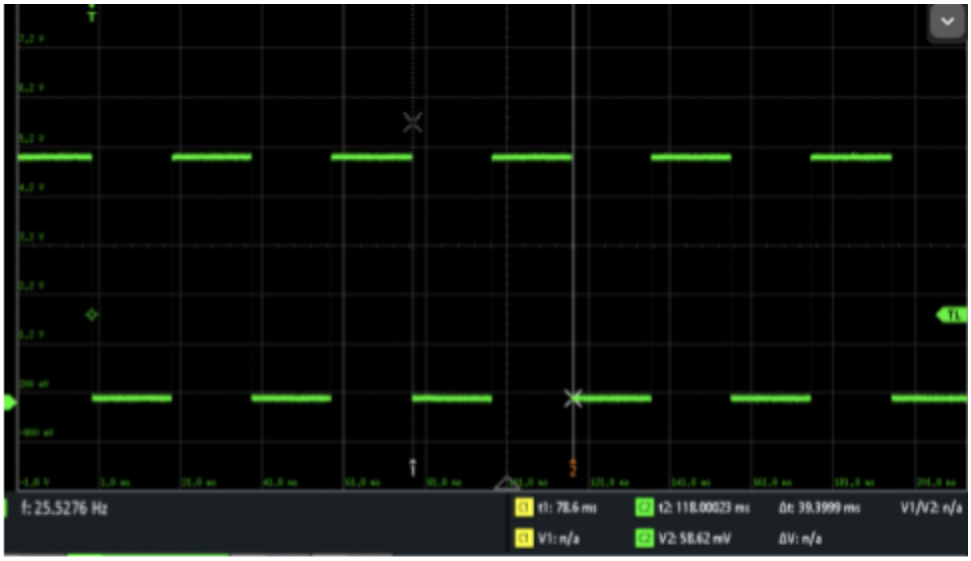


Fig. 66. Square output of modulator with a period of 40ms.

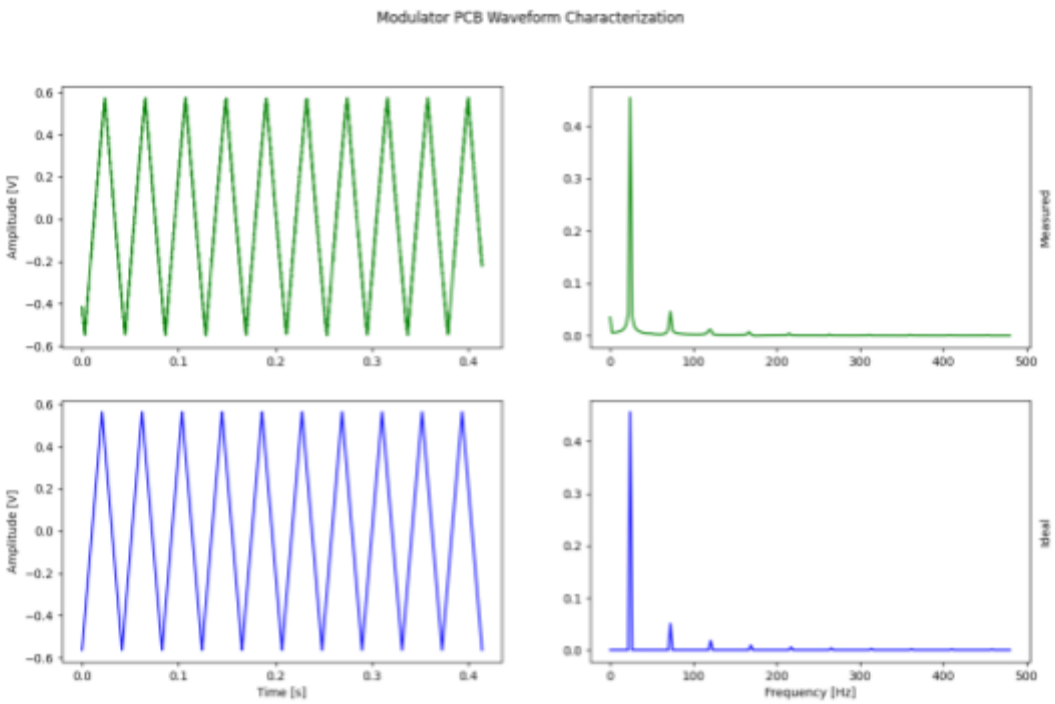


Fig. 67. Modulator characterization.

8.2.4 Gain Stage and Low Pass Filter Test

To test the gain stage we must first ensure that all of the components have been assembled properly onto the circuit and verify that there are neither short nor open components. Then the function generator is connected to the input, the oscilloscope is connected to the output, and the power supply is connected and turned on for DC biasing. The function generator and the oscilloscope are to be connected to the computer executing the test via USB2.0 Type A to USB2.0 Type B cables. The function generator must first have its function set to generate a sine wave with the SCPI command of “SOURce1:FUNCtion SIN”. An AC sweep is performed by implementing a loop that iterates through signal frequency values starting at 1kHz and stopping at a value that is greater than 1MHz, where each subsequent signal frequency value is multiplied by 1.5. At each iteration the function generator is to have its frequency set with the SCPI command of “SOURce1:FREQuency [frequency]” where “[frequency]” is the current frequency value. Upon sending this SCPI command to the function generator the testing computer must sleep the thread for approximately double the settling time in order to allow the signal to settle prior to reading measurements from the oscilloscope. Once settled, the frequency is measured from the oscilloscope with the SCPI command of “MEASure1:MAIN FREQuency” and the amplitude is measured from the oscilloscope with the SCPI command of “MEASure1:MAIN VOLTage:AMPLitude”. This data was then plotted with PyPlot to generate the AC sweep graph as shown in Figure 69.

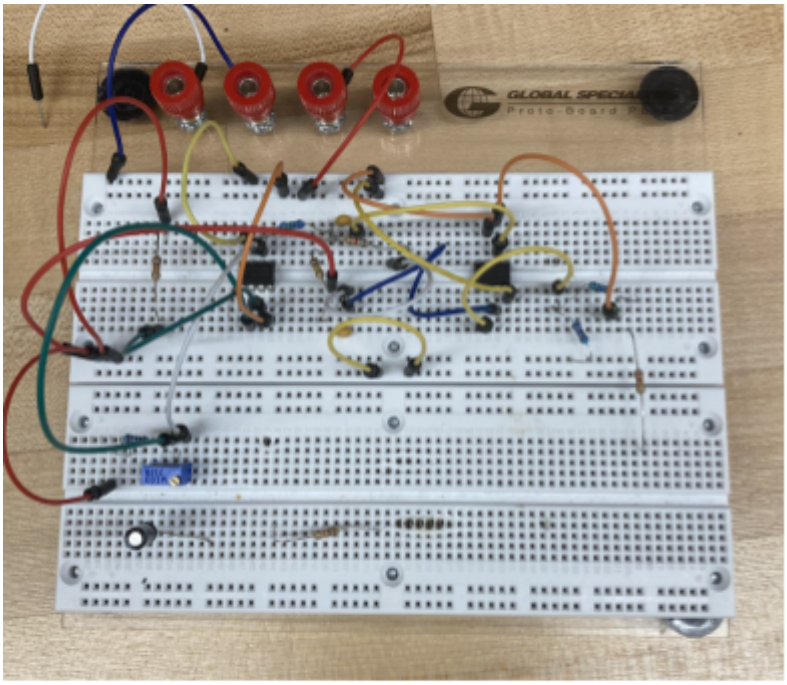


Fig. 68. Gain stage testing.

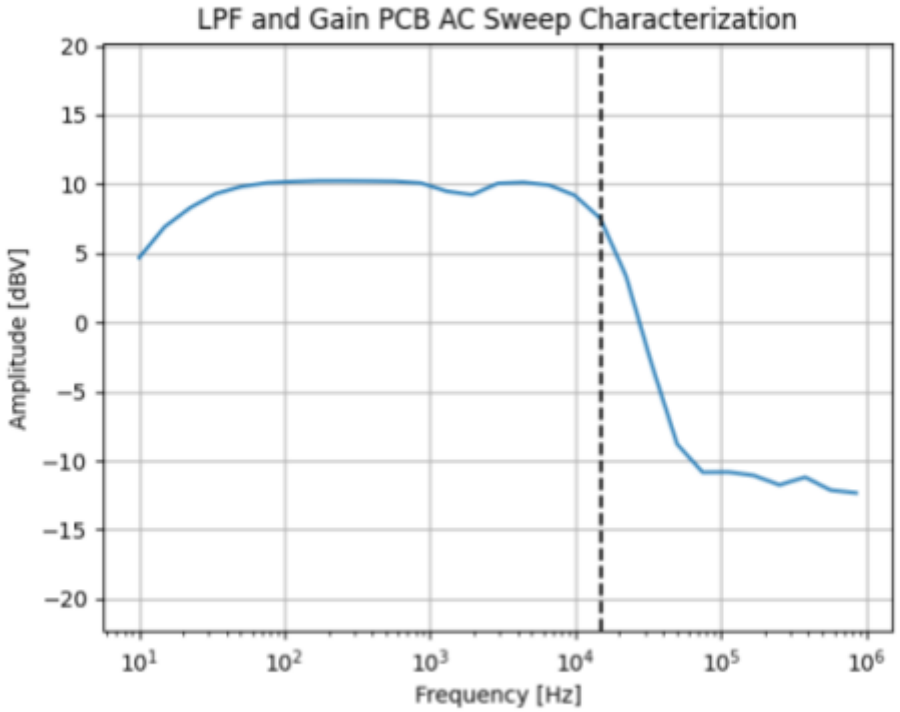


Fig. 69. Gain Stage and Low Pass Filter AC Sweep.

9.0 Administrative Material

9.1 Budget and Finance Discussion

One of the requirements for our project was that the overall value must be less than $800. Note that this was not the amount our team anticipated spending, as we were donated the components that constituted the bulk of the project's value. The table below breaks down our physical project assembly and shows how much each category is valued at.

Table 7

Project Cost Overview	
Category of Parts	Cost
Chassis	$20
Antenna Assemblies	$35
Printed Circuit Boards	$95
RF Circuit Packages	$440
Connectors and Cables	$95
Hardware	$15
Total Cost:	$700

10.0 Future Work

10.1 Hardware

10.1.1 Analog-to-Digital Converter

A dedicated ADC PCB was designed and manufactured for the project, however it had to be omitted due to time constraints. A PCM1802DBR from Texas Instruments was chosen targeting a 44.1kHz sampling frequency. This device is a 24-bit delta-sigma stereo ADC and yields accurate measurements by oversampling the input signals. This device is driven by the SCKI, or system clock input, and it can operate in either "slave" mode or "master" mode. In "slave" mode the device has its clock signals of LRCK (left/right clock) and BCK (bit clock) as inputs that the user must provide in order to

retrieve a bit output on DOUT. In “master” mode the device provides the clock signals of LRCK and BCK, which can then be used to trigger interrupts and collect digitized bit data from DOUT. We have opted for SCKI to be driven by a 22.5792MHz oscillator in order to achieve the sampling frequency of 44.1kHz. For the device to operate as “master” and have a sampling frequency of 44.1kHz we must set “INTERFACE MODE” to “Master mode (512 fS)” by setting the “MODE0” pin to HIGH and the “MODE1” pin to LOW. The “FORMAT” is set to “24-Bit, MSB-First, Left-Justified” by setting both “FMT0” and “FMT1” pins to LOW. From the interface timings shown below, the following observations can be made: a sample begins at the rising edge of FSYNC and ends at the falling edge of FSYNC; a new bit is ready to be read from DOUT at the rising edge of BCK; and the channel of the associated input is indicated by LRCK, with HIGH indicating the left-channel and LOW indicating the right-channel.

Fig. 70. PCM1802 interface timings. Credit: Texas Instruments.

Figure 71 below illustrates how the various power supplies, input signals, and output signals are to be inter-connected within the circuit. Our designed power supply provides the regulated +5V and +3.3V DC voltages, our IF signal is tied to VINL, our synchronization signal is tied to VINR, and our XLH536022.579200X 22.5792MHz oscillator provides the clock signal tied to SCKI. The 1uF capacitor C1 gives an 8 Hz cutoff frequency for the input high pass filter. The two 0.1uF capacitors C2 and C3 that are connected to VREF1 and VREF2 are used for power supply noise reduction purposes. The two 0.1uF capacitors C4 and C5 that are connected between VCC and GND as well as between VDD and GND are used as bypass capacitors, which inhibit noise from entering the analog-to-digital converter by bypassing to GND, yielding a cleaner DC voltage which may be present on the switching voltage regulators used by our power supply.

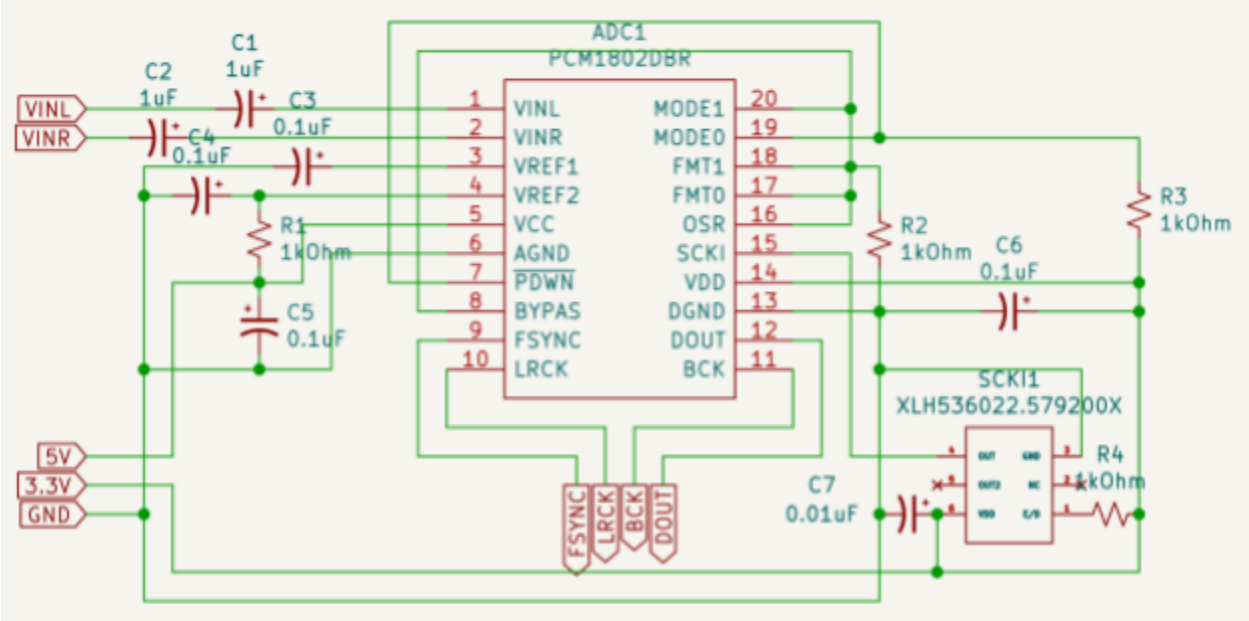


Fig. 71. PCM1802DBR analog-to-digital converter schematic.

One crucial component in the circuit is the crystal clock oscillator driving the ADC. We need a clock signal in order for the ADC to collect samples of the data at a high enough frequency to satisfy the Nyquist Sampling Theorem which states if a system uniformly samples an analog signal at a rate that exceeds the signal's highest frequency by a factor of at least two, then the original signal can be perfectly recovered from the sampled discrete values.

A crystal oscillator uses a piezoelectric crystal as a frequency selective element. Piezoelectricity is the ability of certain crystalline materials to convert mechanical energy into electrical energy. We will be utilizing the inverse piezoelectric effect which turns electrical energy into mechanical energy. This allows us to provide a stable clock signal to the analog to digital converter. A crystal oscillator relies on the slight change of shape of a quartz crystal under an electric field.

A crystal oscillator can be modeled using capacitors and inductors where the series resonance is given as

$$f_r = \frac{1}{2\pi\sqrt{L*C}}$$

And the parallel resonance is given as

$$f_p = \frac{1}{2\pi*\sqrt{L*C_s}} * \sqrt{1 + \frac{C_s}{C_p}}$$

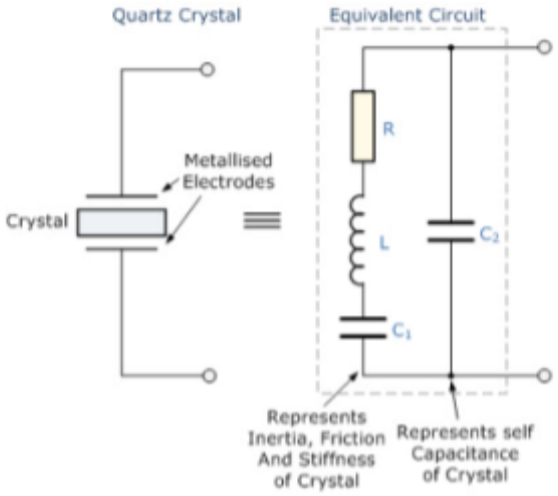


Fig. 72. Quartz crystal equivalent circuit.

Crystals must be designed to provide a load capacitance.

Usually bipolar transistors are used in the construction of crystal oscillator circuits. Since crystal oscillators are highly stable, have a high Q-factor, and are small, they are a more favorable choice for timekeeping over other types of resonators such as LC circuits.

In order to have a functional analog-to-digital converter we need a clock source. Originally we planned to build a crystal clock oscillator from scratch to drive the analog to digital converter. This will allow us to collect discrete samples from the continuous analog signal. During our market search we found a Renesas XL Low Phase Noise Quartz-based PLL oscillator that would provide this function for us. This is convenient as it would eliminate the need to design an entire crystal oscillator circuit. The Renesas XL is a ultra-precision crystal oscillator with 750 to 890fs phase jitter over a 12kHz - 20MHz bandwidth. The noise from this device is comparable to traditional bulk quartz and SAW oscillators. This device was an ideal choice due to its low cost, low noise, and wide frequency range. This is an active device and we would be supplying 3.3V from the power supply circuit to power the device.

In terms of physical implementation this device is directly integrated onto the circuit board for the analog to digital converter.

The analog-to-digital converter PCB consists of the following two ICs: the PCM1802DBR (24-bit 44.1kHz ADC) and the XLH536022.579200X (22.5792MHz clock oscillator). The XLH536022.579200X was chosen specifically to target the PCM1802DBR's sampling frequency of 44.1KHz, or 512 times greater than that of the sampling frequency. This oversampling is performed to improve both the resolution of

the analog-to-digital converter and the signal-to-noise ratio, yielding a more accurate measurement.

At the “VINL” and “VINR” pins 1µF capacitors are placed in order to target an 8Hz cutoff frequency of the high-pass filter of the analog-to-digital converter, which is computed given that the device has an input impedance of approximately 20kΩ. Two 0.1µF capacitors are placed at both “VREF1” and “VREF2” to ascertain that the references have low source impedances. Additionally, two 0.1µF bypass capacitors are placed at both “VCC” and “VDD” to filter out any noise from our power supply. The mode select pins of “~PDWN” and “MODE0” are tied to a LOW digital signal via a 1kΩ resistor and the pins of “BYPAS”, “OSR”, “MODE1”, “FMT0”, and “FMT1” are tied to a HIGH digital signals via a 1kΩ resistor. The XLH536022.579200X has a 0.01µF bypass capacitor placed at its “VDD” to mitigate power supply line noise.

Three female connectors are used to allow for input and output connections between our various PCBs. A 1x2 female header is used to connect the “LPF_OUT” to the “VINL” node and the “SYNC” to the “VINR” node, a 1x3 female header is used to connect the +5V, +3.3V, and GND of the power supply, and a 1x4 female header is used to connect the analog-to-digital converter’s output signals of “FSYNC”, “LRCK, “BCK”, and “DOUT” to the MCU for digitization.

A 3D rendering of the analog-to-digital converter PCB can be visualized in Figure 73 below.

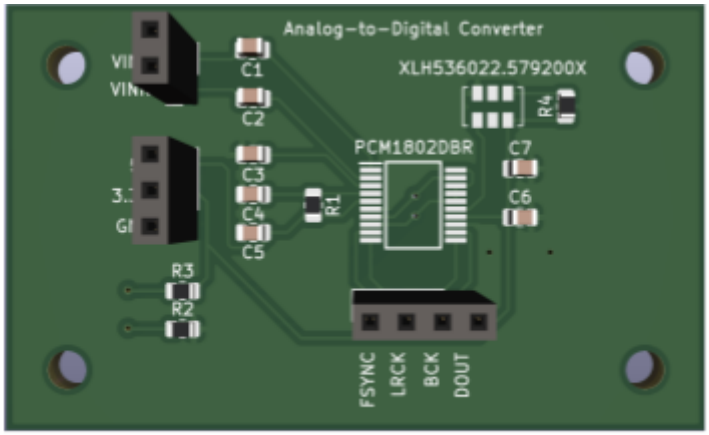


Fig. 73. ADC PCB 3D rendition

10.2 Software

10.2.1 Real-Time Processing

The timings of the generated signals are relatively fast, with sampling frequencies in the megahertz range and wait periods in the microsecond range. As such the burst data must be accumulated directly on the microcontroller that is ingesting the samples from

the analog-to-digital converter prior to transmission to the host device in lieu of transmitting individual samples. Each burst contains a number of chirps that is specified by the “chirps-per-burst” parameter, each chirp contains a number of samples that is specified by the “samples-per-chirp” parameter, the inter-chirp delay is specified by the “chirp period” in microseconds, and the inter-burst delay is specified by the “burst period” in microseconds.

These samples are obtained as serial data through an external interrupt-attached digital pin where a total of n interrupts would be triggered for an n-bit analog-to-digital converter. Each bit of the n-bit data sample is to be stored in a buffer with a size of $\lceil n / 8 \rceil$ bytes. For each of the n subsequent interrupts, the bits are accumulated in the buffer by left-shifting the buffer over by 1 bit then OR’ing the digital pin reading to the buffer. The process of filling the buffer with the n-bit analog-to-digital converter reading is visualized in the flow chart of Figure 74 below.

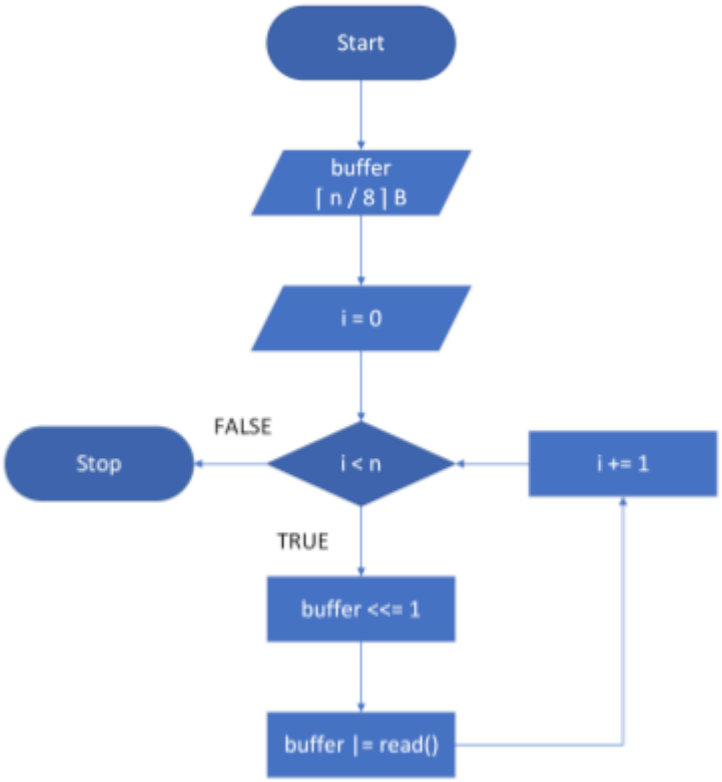


Fig. 74. Flow chart demonstrating the accumulation of serial analog-to-digital converter bit values into a buffer.

The minimum possible non-zero value that each sample can represent is constrained by the analog-to-digital converter’s bit resolution and maximum input voltage. For example, for an analog-to-digital converter with a bit resolution of 24-bits and a maximum input voltage of +5V, the analog value would be represented as a floating-point number in the

range of 0.0 to 5.0, with a minimum possible non-zero value of $5 / 2^{24} \approx 2.98 * 10^{-7}$, or a resolution of about +0.3μV.

These samples are then accumulated in the burst buffer whose size is determined by the size of each sample, the number of samples-per-chirp, and the number of chirps-per-burst. This size is constrained by the Static Random-Access Memory (SRAM) available to the microcontroller. For example, using an SRAM size of 32 kilobytes, reserving 50% of that SRAM for burst data, a sample size of 24 bits ($\lceil 24 / 8 \rceil = 3$ bytes), and a chirps-per-burst of 5, each burst could contain a total of $\lfloor SRAM * 0.5 / (sample\ size * chirps\text{-}per\text{-}burst) \rfloor = \lfloor 32 * 10^3 * 0.5 / (3 * 5) \rfloor = 1066$ samples-per-chirp. At the sampling frequency of $f_s = 96kHz$, the total amount of time to collect these 1066 samples would be $1 / f_s * samples - per - chirp = 1 / (96 * 10^3) * 1066 \approx 11.1ms$. With the inter-chirp period of 40ms as set by the modulator, the total amount of time to collect a complete burst would be approximately $11.1ms + 40ms * 5 = 211.1ms$.

10.2.2 Ripple Interface

The software design is critical to introducing aspects of modularity by offering a Software Development Kit (SDK) with our frequency-modulated continuous-wave radar module. This SDK is designed to expedite the application development process for end-users by providing an Application Programming Interface (API) that conforms to the Consumer Technology Association's (CTA)® Ripple standard. This standard was chosen for its emphasis on enabling inter-operation between hardware and software for radar systems. This SDK is to be run on a host device that must connect to our module via a USB2 interface.

At its core the API implementation of the Ripple standard offers a layer hardware abstraction to interface with our module. This includes a state machine specification that controls the states of the system and the configuration of the system's parameters that determine its modes of operation.

The state machine is extraordinarily simple in that it consists of four states and six transitions. The four states are the following: "OFF", "IDLE", "ACTIVE", and "SLEEP". The six transitions are the following: "TurnOn", "TurnOff", "StartDataStreaming", "StopDataStreaming", "GoSleep", and "WakeUp". The sensor is initialized to the "OFF" state where it consumes the least amount of power and does not produce any amount of data. Calling the "turn_on" method triggers the "TurnOn" transition that transitions from the "OFF" state to the "IDLE" state, which indicates that the sensor is prepared for operation. It is from within this state that configurations may be activated and deactivated. Calling the "go_sleep" method triggers the "GoSleep" transition that transitions from the "IDLE" state to the "SLEEP" state, where power consumption is minimized but configuration settings are retained, and calling the "wake_up" method triggers the "WakeUp" transition that transitions from the "SLEEP" state back to the "IDLE" state. Calling the "start_data_streaming" method triggers the

“StartDataStreaming” transition that transitions from the “IDLE” state to the “ACTIVE” state, where the sensor begins transmitting and receiving radio waves using the activated configuration settings, and calling the “stop_data_streaming” method triggers the “StopDataStreaming” transition that transitions from the “ACTIVE” state back to the “IDLE” state. To discard all configuration settings and deactivate the device, the “turn_off” method must be called to trigger the “TurnOff” transition that transitions from the “IDLE” state to the “OFF” state. This state machine is visualized in the diagram of Figure 75 below.

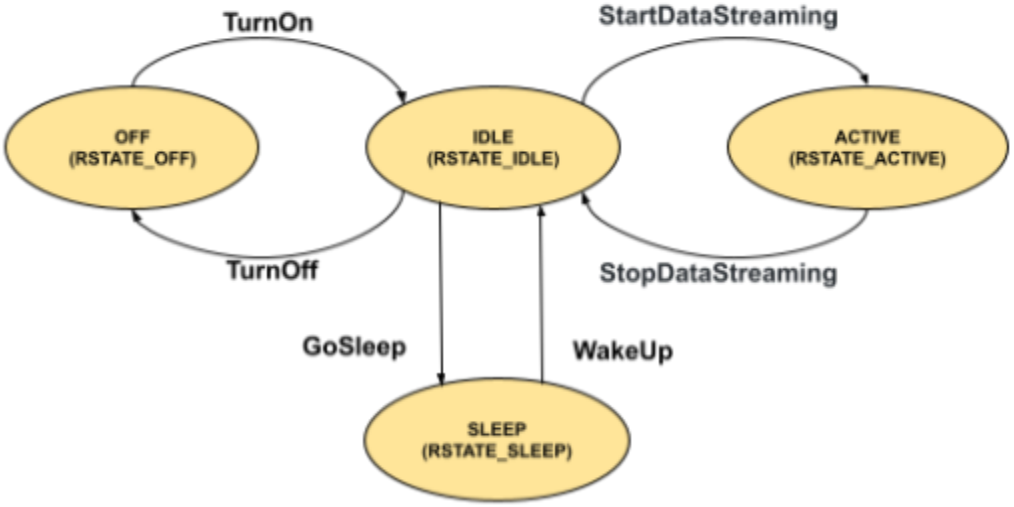


Fig. 75. The Ripple state machine diagram. Credit: Consumer Technology Association.

The API allows for the definition of up to 256 configurations via unsigned byte slot identifiers, however we will enable only one slot (one configuration) for our project. These configuration parameters consist of the three following groups: main parameters, transmitter parameters, and receiver parameters.

The main parameters group consists of the following parameters: the afterburst power mode determines the power mode of the module following the burst period; the inter-chirp power mode determines the power mode of the module between chirp periods; the burst period specifies the period between subsequent bursts in microseconds; the chirp period specifies the period between subsequent chirps in microseconds; the chirps-per-burst specifies the number of chirps contained within a single burst; the samples-per-chirp specifies the number of analog-to-digital converter samples contained within a single chirp; the lower frequency specifies the frequency at which the transmitter antenna begins the emitting of its signal; the upper frequency specifies the frequency at which the transmitter antenna ends the emitting of its signal; the transmitter antenna mask specifies which transmitter antennas are currently enabled; the receiver antenna mask specifies which receiver antennas are currently

enabled; and the analog-to-digital converter sampling frequency specifies the rate at which analog samples are digitized.

The transmitter parameters group consists of the following parameters: the power specifies the transmitter antenna power emission in decibels.

The receiver parameters group consists of the following parameters: the variable gain amplifier specifies the signal gain in decibels; the high pass filter gain specifies the filter gain in decibels; the high pass filter cutoff specifies the cutoff frequency in kilohertz.

The Ripple standard defines two interfaces that the developer must implement to facilitate bi-directional module-to-host communication, which consists of a sensor interface and a sensor observer interface. The sensor interface directly communicates with our board via USB2 to modify & retrieve parameter values, transition between states, and retrieve burst readings. The sensor observer interface contains callbacks to be notified of modified register values and be notified of new burst readings to be processed.

The sensor interface stores the aforementioned configuration parameters to be communicated with the module. These configuration parameters of a slot can be modified and retrieved with “set” and “get” methods, which include the following: “set_main_param”, “get_main_param”, “set_tx_param”, “get_tx_param”, “set_rx_param”, and “get_rx_param”. Once the specified slot has its configuration parameters set, the parameters can be communicated to the module with the “activate_config” method if it is in the “IDLE” state. With the configuration activated data streaming may begin by calling the “start_data_streaming” method. When this method is called a thread is spawned independently of the main thread in order to communicate with the module to retrieve new bursts. This allows for seamless data transmission and data processing.

Prior to turning on the sensor the user may register a sensor observer, which contains the “on_burst_ready” callback. As the name indicates, it is called when a burst is ready to be read from the sensor. As such, the user may call “read_burst” on the sensor to retrieve the burst format as well as the raw data as a sequence container of bytes. This data contains the measured power of the received signal which may be used for a variety of purposes, such as velocity measurement, ranging measurement, and synthetic-aperture radar mapping.

10.2.3 Module-Host Data Transmission

Module-host data transmission is facilitated by the USB2 serial communication standard employing the request-response message pattern. In this pattern the host populates and sends a request structure to the module, which in turn processes the request, populates a response structure, and sends the response back to the host. The request structure consists of an 8-bit unsigned integer “command” field that designates the command to be processed, a 16-bit unsigned integer “size” field that specifies the size of the subsequent buffer field in bytes, and an 8-bit unsigned integer array “buffer” field

allocated to the size specified by the “size” field. Similarly, the response structure consists of an 8-bit unsigned integer “status” field that specifies if the processed request was either a success or a failure, a 16-bit unsigned integer “size” field that specifies the size of the subsequent buffer field in bytes, and an 8-bit unsigned integer array “buffer” field allocated to the size specified by the “size” field. The “command” field values of the request are chosen by the programmer and the “status” field values of the response of “SUCCESS” and “FAILURE” are 1 and 0, respectively. Alternatively, the user may implement custom status values. These structures and their fields are more clearly visualized in the Table 7 below.

Table VII
Request and Response Data Structures

Request Structure	
Type	**Field**
uint8_t	command
uint16_t	size
uint8_t []	buffer
Response Structure	
Type	**Field**
uint8_t	status
uint16_t	size
uint8_t []	buffer

Our project will implement the following request commands to be processed by the module: “SET_MAIN_PARAMS”, “SET_TX_PARAMS”, “SET_RX_PARAMS”, “SET_STATE”, and “READ_BURST”. The values corresponding to these commands are stored in an enumeration with the following values: “SET_MAIN_PARAMS” is 0; “SET_TX_PARAMS” is 1; “SET_RX_PARAMS” is 2; “SET_STATE” is 3; and “READ_BURST” is 4.

The “SET_MAIN_PARAMS” command sets the main parameters on the module. The request is expected to contain the following data: a command field storing the value of the “SET_MAIN_PARAMS” enumeration element; a size field storing the value of $4\ bytes\text{-}per\text{-}parameter\ *\ 15\ parameters\ =\ 60\ bytes$; and a buffer field storing the values of the parameters “AFTERBURST_POWER_MODE”, “INTERCHIRP_POWER_MODE”, “BURST_PERIOD_US”, “CHIRP_PERIOD_US”, “CHIRPS_PER_BURST”, “SAMPLES_PER_CHIRP”, “LOWER_FREQ_MHZ”, “UPPER_FREQ_MHZ”, “TX_ANTENNA_MASK”, “RX_ANTENNA_MASK”, and

“ADC_SAMPLING_HZ”. If this size expectation is met then the parameter values stored in the buffer are applied and digital pin output values associated with the parameters are modified. On success a response is generated containing the following data: a status field storing the value of “SUCCESS”; a size field storing the value of 0; and a buffer field that is empty. On failure a response is generated containing the following data: a status field storing the value of “FAILURE”; a size field storing the value of 0; and a buffer field that is empty.

The “SET_TX_PARAMS” command sets the transmitter parameters on the module. The request is expected to contain the following data: a command field storing the value of the “SET_TX_PARAMS” enumeration element; a size field storing the value of $4\ bytes\text{-}per\text{-}parameter\ *\ 1\ parameter\ =\ 4\ bytes$; and a buffer field storing the value of the parameter “POWER_DB”. If this size expectation is met then the parameter values stored in the buffer are applied and digital pin output values associated with the parameter are modified. On success a response is generated containing the following data: a status field storing the value of “SUCCESS”; a size field storing the value of 0; and a buffer field that is empty. On failure a response is generated containing the following data: a status field storing the value of “FAILURE”; a size field storing the value of 0; and a buffer field that is empty.

The “SET_RX_PARAMS” command sets the receiver parameters on the module. The request is expected to contain the following data: a command field storing the value of the “SET_RX_PARAMS” enumeration element; a size field storing the value of $4\ bytes\text{-}per\text{-}parameter\ *\ 3\ parameters\ =\ 12\ bytes$; and a buffer field storing the value of the parameters “VGA_DB”, “HP_GAIN_DB”, and “HP_CUTOFF_KHZ”. If this size expectation is met then the parameter values stored in the buffer are applied and digital pin output values associated with the parameter are modified. On success a response is generated containing the following data: a status field storing the value of “SUCCESS”; a size field storing the value of 0; and a buffer field that is empty. On failure a response is generated containing the following data: a status field storing the value of “FAILURE”; a size field storing the value of 0; and a buffer field that is empty.

The “SET_STATE” command directly assigns the state of the module. The state values are stored in an enumeration with the following values: “OFF” is 0; “IDLE” is 1; “SLEEP” is 2; and “ACTIVE” is 3. The request is expected to contain the following data: a command field storing the value of the “SET_STATE” enumeration element; a size field storing the value of $1\ byte$; and a buffer field storing the value of the state enumeration element of either “OFF”, “IDLE”, “SLEEP”, or “ACTIVE”. If this size expectation is met then the state is set to the value that is stored in the buffer and the following events will occur for each of the states: in the “OFF” state the module is completely powered down; in the “IDLE” state the module is powered on, is ready to have configurations set, and is ready to be activated; in the “SLEEP” state the module enters a low-power mode where the configuration settings are retained; and in the “ACTIVE” mode the module begins actively transmitting and receiving data. On success a response is generated containing the following data: a status field storing the value of “SUCCESS”; a size field storing the value of 0; and a buffer field that is empty. On failure a response is generated containing

the following data: a status field storing the value of “FAILURE”; a size field storing the value of 0; and a buffer field that is empty.

The “READ_BURST” command reads the burst current stored within the module’s internal burst buffer. The request is expected to contain the following data: a command field storing the value of the “READ_BURST” enumeration element; a size field storing the value of 0; and a buffer field that is empty. On success a response is generated containing the following data: a status field storing the value of “SUCCESS”; a size field storing the size of the burst buffer that is $\lceil n / 8 \rceil * samples\text{-}per\text{-}chirp * chirps\text{-}per\text{-}burst$ bytes where n is the amount of bits provided by the analog-to-digital converter; and a buffer field storing the analog-to-digital converter samples. On failure a response is generated containing the following data: a status field storing the value of “FAILURE”; a size field storing the value of 0; and a buffer field that is empty.

10.2.4 Ranging and Velocity Computation

Implementations such as velocity extraction, range extraction, or synthetic aperture radar mapping must be responsive if they are expected to provide real-time updates. In order to achieve this the highly-optimized Eigen linear algebra library is leveraged to handle these computations hastily. Using Eigen’s Fast Fourier Transform (FFT) class it is possible to extract both the velocity and ranging information from a radar burst. The Fast Fourier Transform computes the Discrete Fourier Transform but many orders of magnitude faster by taking advantage of the periodicity of sinusoids. By identifying where these signals overlap it is possible to reduce the overall number of multiplications necessary to compute the Fourier transform. This reduction in multiplications is substantial yielding a complexity of $O(N\ log_2 N)$ compared to the $O(N^2)$complexity of the DFT. For large data sets this reduction is immense as the growth of N^2 rapidly outpaces the growth of $N\ log_2 N$. For example, for an $N = 100$ the ratio of computations of the DFT compared to the FFT is $(100^2)/(100 * log_2 100) \approx 15$, and for an $N = 1000$ the ratio of computations of the DFT compared to the FFT is $(1000^2)/(1000 * log_2 1000) \approx 100$. These discrepancies between $O(N^2)$ and $O(N\ log_2 N)$ are more clearly visualized in Figure 76 below.

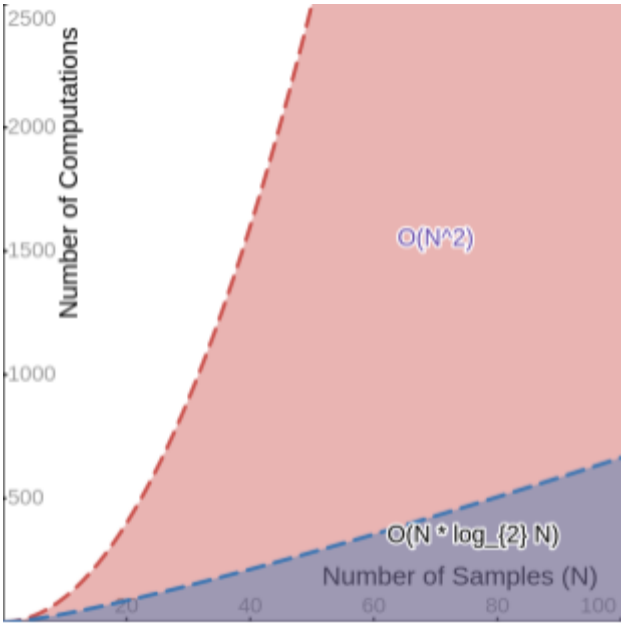


Fig. 76. FFT versus DFT number of computations.

A separate class for ranging and velocity computation will ingest burst readings from the sensor observer. Applying the FFT to the columns of the burst data matrix whose columns denote the chirp index and whose rows denote the sample index it is possible to extract the ranging information. Then, by applying the FFT a second time to the rows of the previous FFT-transformed data matrix it is possible to extract the velocity information. The final result is a matrix whose rows contain ranging data and whose columns contain velocity data. It is then possible to refine this data by applying the Constant False Alarm Rate (CFAR) algorithm to filter out noise. The CFAR algorithm averages neighboring cells to a test cell to establish an interference baseline, where if this baseline is exceeded then noise is assumed to be present and ignored. This ranging and velocity extraction implementation is visualized in the Figure 77 below.

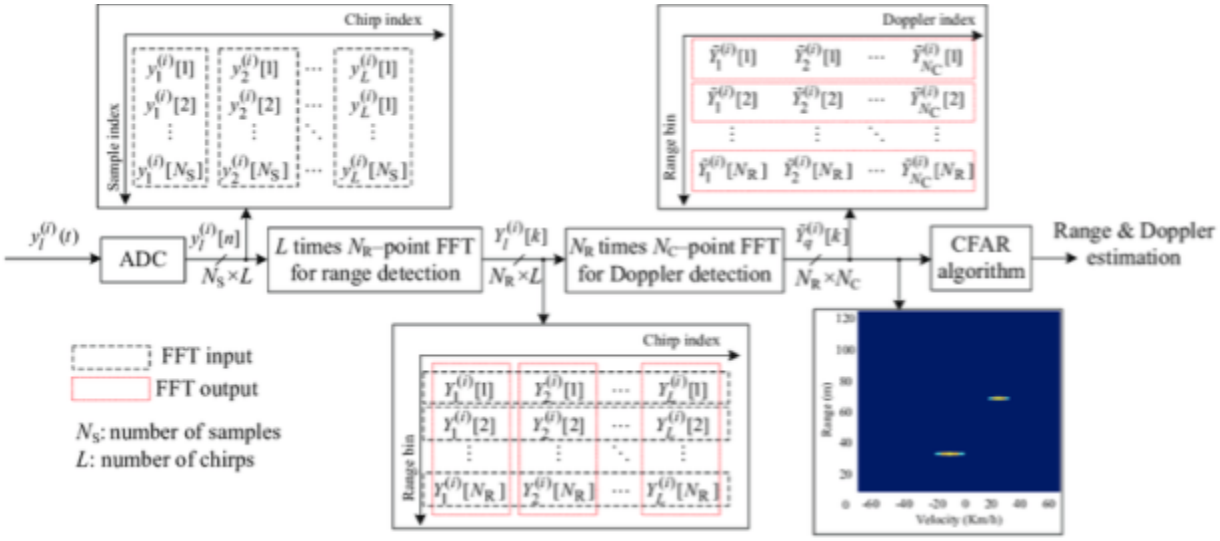


Fig. 77. Ranging and velocity extraction from FMCW burst data. Credit: Kim, Bong-seok & Kim, Sangdong & Jin, Youngseok & Lee, Jonghun [15].

10.2.5 Graphical User Interface

A Graphical User Interface will be implemented to simplify interacting with the FMCW radar module. The Visualization Toolkit will be used to visualize the ranging & velocity data and to implement widgets such as buttons & text boxes. It will have buttons to change between the “OFF”, “IDLE”, “SLEEP”, and “ACTIVE” states of the state machine, and display which of the states is currently active. It will also have sliders to modify parameter values constrained within their ranges, which can only be modified when not in the “ACTIVE” state. Given this behavior, the user will be locked out from making modifications to the parameters, but can still see what their values are currently set to.

The ranging & velocity data will be visualized in a 2-dimensional graph that is updated in real-time. The ranging values will be in units of meters and represent values along the Y-axis and the velocity values will be in units of meter-per-second and represent values along the X-axis. These power values will be color-coded with dark blue at the low end of the spectrum and bright yellow at the high end of the spectrum for easy visualization. Additionally, the GUI may implement a third dimension of time with units of seconds. This would allow for 3-dimensional visualization over a set period of time by maintaining a first-in first-out queue of range & velocity data. This would allow for easy identification of vehicles that may be accelerating or decelerating as they pass by.

An example rendering of the aforementioned layout and its features is demonstrated below in Figure 78. This rendering is merely an example and not reflective of the final product.

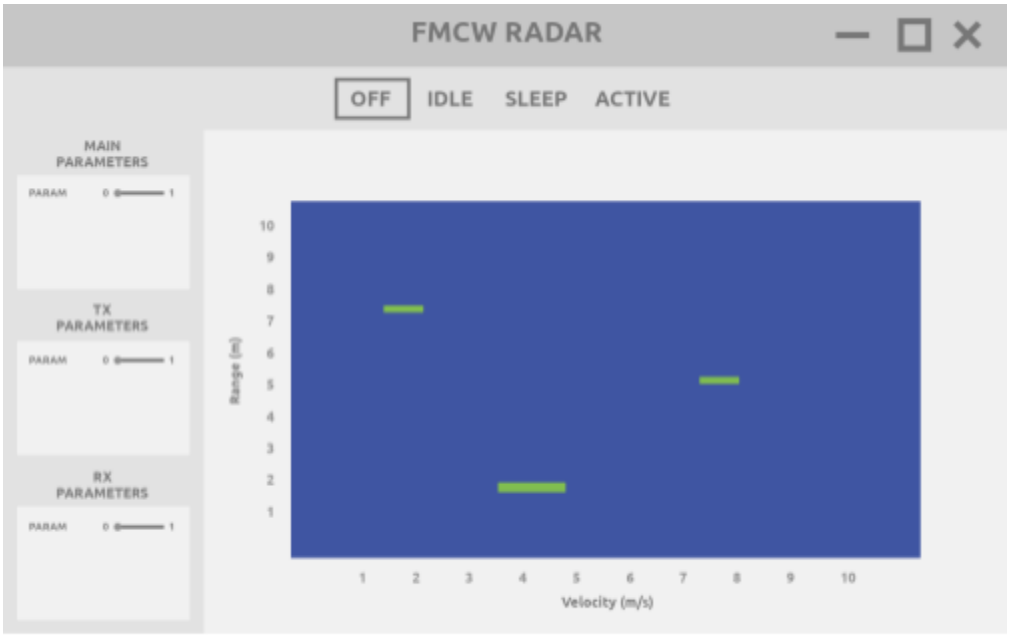


Fig. 78. The GUI concept for interacting with the module.

9.0 Conclusion

Our team has made significant progress since the beginning of Senior Design. We began with the general concept of a radar application. Our desire to demonstrate our knowledge of multiple electrical engineering sub-disciplines and create a quality consumer product led us to solidify our project as a frequency-modulated continuous-wave radar module with multiple applications and a customizable software interface. This project uses RF engineering, integrated circuits, electronics, digital signal processing and coding, which covers many different areas of electrical engineering. This allows each member of the team to demonstrate their understanding and capabilities in their area of specialization.

After obtaining a donated, partially-built radar module from our sponsor Dr. Xun Gong, our team outlined a series of goals to aim for. Our primary goal is to use our radar module to measure the velocity of vehicles driving on a street near the engineering building at UCF. One of our stretch goals is to expand the capabilities of the software and output range readings. Lastly, we have a stretch goal of using the velocity readings, the range readings, or both as the input to a control system with external hardware.

In addition to technical goals, our team has a set of administrative goals that will facilitate the technical design, test and integration processes. We will meet regularly, provide updates between members with regard to progress on the technical aspects of the project, document our design changes, and keep a good record of our project remonstration results.

To reach these goals, our team will need to finish designing the radar module provided to use by Dr. Xun Gong, design a USB2 interface between the module and the host device in our system, develop a user-friendly API, construct and test our prototype, make any necessary modifications, and finally demonstrate our project.

A set of requirement specifications has been outlined to guide our system design. These requirements are related to the size, power consumption, accuracy and versatility of the system. In order to meet the specifications, our design will need to be balanced, as improving the system in one area may worsen the system in another area. The project's house of quality shows the interdependency between various characteristics of the system.

Our project is based on MIT's laptop-based radar, and our team performed extensive research to understand the operation of the baseline system. Background information related to radar technology, remote sensing, microwave propagation, antennas, transceiver architectures, and pulse-doppler processing are all relevant to our project. Additionally, research was performed to investigate how MIT's baseline system design could be improved, particularly by implementing real-time signal processing and using a USB interface between the host device and radar system. All of the research combined resulted in a set of components that would be used in our design, including a microcontroller, analog-to-digital converter, mixer, splitter, amplifier, oscillator and modulator. A complete system block diagram was then established which outlined how signals and information would move through our system. The diagram was easily divisible into three distinct subsystems: the RF module, the RF data processing, and the implementation.

The design of each subsystem is subject to various constraints. Some of these constraints are industry standards, such as the C++ programming language, the physical characteristics of alkaline batteries, and the dimensions of coaxial connectors. Other constraints are specific to our project, such as time constraints related to our course deadlines, health constraints related to RF transmission safety, and financial constraints created by the current economic environment. These constraints must be taken into consideration during the system design, from the initial design and through subsequent design iterations.

The hardware design process is broken up into the following subsystems and circuits: the power supply, the modulator circuit, the RF subsystem, the gain stage, the low pass filter, and the analog-to-digital converter circuit. Each system or circuit has its own functionality and specifications. The circuits being designed will be assembled on PCBs, while the majority of the RF subsystem consists of antennas and pre-assembled circuits within block housings.

The software design consists of receiving and processing the signal from the RF subsystem. Real-time processing is accomplished by receiving a set amount of data per period and performing computations on just that dataset. The Ripple radar standard is used to develop the software. The software graphical user interface enables easy

control of the radar module and acquisition of the computed velocity and range values at any given instant.

The project prototype is already partially complete. The only remaining elements are the PCBs. Two versions of these PCBs will be constructed during the testing phase of the project. The first version will be manufactured using a milling machine. The PCBs from the machine will be used for quick, small-scale design verification. Once designs are verified, PCBs will be manufactured by JLCPCB. The majority of components such as resistors and capacitors will be assembled prior to our team's receipt of the board, and our team will complete the assembly phase by soldering the remaining components.

Each element of the system will need to be tested, with the tests corresponding to the parameters that need to be verified. Several pieces of lab equipment will be used to verify that our subsystems and circuits are working as desired, including multimeters, oscilloscopes, DC power supplies, and network analyzers. Software-driven test procedures will be used to generate complete analysis reports and provide concrete, quantitative test results. The software testing consists of verifying that the USB interface is operational and the computations in the software are accurate.

Once our individual subsystems have been verified, the integration process will begin. There may be difficulties in the integration process that require design changes. The integration phase often encompasses intermittent redesign phases until the system is capable of functioning as a whole unit. At this point, it is important to return to the requirement specifications and verify that the system has met them. If a requirement has not been met, the system may need further modification or the requirement itself may need to be updated.

The final step in the process is the demonstration. During our demonstrations, it will be important to record as many details as possible about the performance of the system. The requirement specifications can be used as the guidelines for measuring system performance. Ultimately the system will be rated based on how many specifications it is able to meet during demonstration.

Although the focus of this project is primarily on the technical aspects, our team has made an intentional effort to expand our focus beyond this. Engineering in the industry encompasses aspects of business as well, and our team's goal is to produce a quality, marketable consumer product. Our ultimate goal by the end of Senior Design is to have a product rather than just a device. It will be user-friendly, accurate, reliable, and versatile. Further development in the future can lead to an even better product.

Our team will continue to track our progress as we complete the design phase of our project this December and move into the testing phase starting in January. We will constantly evaluate the quality and performance of our system to ensure our end result is satisfactory.

11.0 Appendices

11.1 References

[1] “IEC 60086-1:2021,” *IEC Webstore,* June 17, 2022. [Online]. Available: *webstore.iec.ch/publication/60968*. [Accessed Nov. 3 2022].

[2] “ANSI C18.1M, Part 2-2019,” *ANSI Webstore*. [Online]. Available: *webstore.ansi.org/Standards/NEMA/ansic181mpart2019*. [Accessed Nov. 3 2022].

[3] “IEC 61169-15:2021,” *IEC Webstore*. [Online]. Available: *https://webstore.iec.ch/publication/62310*. [Accessed Nov. 3 2022].

[4] “ISO/IEC 14882:2020 Programming Languages - C++,” *ISO*. [Online]. Available: *www.iso.org/standard/79358.html*. [Accessed Nov. 3 2022].

[5] “ISO/IEC 9899:2018 Information Technology - Programming languages - C,” *ISO*. [Online]. Available: *www.iso.org/standard/79358.html*. [Accessed Nov. 3 2022].

[6] “Language Reference,” *Arduino*. [Online]. Available: *www.arduino.cc/reference/en/.* [Accessed Nov. 3 2022].

[7] “Ripple,” *Consumer Technology Association.* [Online]. Available: *www.cta.tech/Resources/Standards/Ripple.* [Accessed Nov. 3 2022].

[8] “IEC 62680-2-1,” *IEC.* [Online]. Available: *webstore.iec.ch/preview/info_iec62680-2-1%7Bed1.0%7Den.pdf.* [Accessed Nov. 3 2022].

[9] “Standard Commands for Programmable Instruments (SCPI),” *IVI Foundation*. [Online]. Available: *https://www.ivifoundation.org/docs/scpi-99.pdf*

[10] “VPP-4.3: The VISA Library,” *IVI Foundation*. [Online]. Available: *https://www.ivifoundation.org/downloads/Architecture%20Specifications/vpp43_2022-05-19.pdf*

[11] “FCC Online Table of Frequency Allocations,” *Federal Communications Commission,* July 1, 2022. [Online]. Available: *transition.fcc.gov/oet/spectrum/table/fcctable.pdf.* [Accessed Nov. 3 2022].

[12] “What are the ISM Bands, and What Are They Used For?,” *Military-Aerospace Electronics,* Feb. 19, 2019. [Online]. Available: *www.militaryaerospace.com/directory/blog/14059677/what-are-the-ism-bands-and-what-are-they-used-for.* [Accessed Nov. 3 2022].

[13] “RF Safety FAQ,” *Federal Communications Commission.* [Online]. Available: *www.fcc.gov/engineering-technology/electromagnetic-compatibility-division/radio-frequency-safety/faq/rf-safety#Q6.* [Accessed Nov. 3 2022].

[14] “Programming Chirp Parameters in TI Radar Devices,” *Texas Instruments*. [Online]. Available: https://www.ti.com/lit/an/swra553a/swra553a.pdf

[15] “Low-Complexity Joint Range and Doppler FMCW Radar Algorithm Based on Number of Targets,” *Kim, Bong-seok & Kim, Sangdong & Jin, Youngseok & Lee, Jonghun*. (2020). Sensors. 20. 10.3390/s20010051.

[16] “Transmission Line Model,” *Microwaves101.* [Online]. Available: *www.microwaves101.com/encyclopedias/transmission-line-model.* [Accessed Nov. 22 2022].

[17] “Build A Small Radar System Capable of Sensing Range, Doppler and Synthetic Aperture Radar Imaging,” *MITOpenCourseware.* [Online]. Available: *ocw.mit.edu/courses/res-ll-003-build-a-small-radar-system-capable-of-sensing-range-doppler-and-synthetic-aperture-radar-imaging-january-iap-2011/pages/projects/.* [Accessed Nov. 4 2022].

[18] Vortex. “Police Radar: How it Works & How to Beat It,” *Vortex Radar, Nov. 9, 2017.* [Online]. Available: *www.vortexradar.com/2017/11/police-radar/.* [Accessed Nov. 4 2022].

[19] Shane Cloude, *An Introduction to Electromagnetic Wave Propagation & Antennas.* Springer New York, NY. 1996.

[20] “Publication Number: 558074,” *Federal Communications Commission, April 2, 2019.* [Online]. Available: *https://apps.fcc.gov/oetcf/kdb/forms/FTSSearchResultPage.cfm?switch=P&id=21124*. [Accessed Dec. 6 2022].