FMCW Radar Module

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***Abstract*— This paper gives an overview of the requirements, design, manufacturing, and test and evaluation of the FMCW Radar Module, the project for UCF Senior Design Group 16 (Fall 2022-Spring 2023). The objectives that need to be achieved in order for the team's goals to be met are discussed, followed by a system functionality description and a deeper dive into each of the subsystems. The paper concludes with the tests that must be performed to verify the requirement specifications are met.**

***Keywords*— FMCW radar, radio frequency, signal processing, antenna, modulator, voltage-controlled oscillator, Fourier transform, ISM band, low-pass filter, analog-to-digital converter, serial peripheral interface, STM32 Nucleo, Ripple API standard**

I. Introduction

Radar systems are a diverse class of remote sensing technology. Transmit frequency and power, antenna design, transmit power, data processing structure and many other system characteristics may be customized to suit the needs of many different applications. In particular, the use of compact, low power, and easy to use radar systems are making their way into the lives of everyday consumers. By finding a balance between ease of use and the ability to customize the system, our team has developed a Frequency Modulated Continuous Wave (FMCW) radar module. that allows everyday consumers to view real-time velocity and range readings for objects in dynamic environments.

II. Goals and Objectives

Our team has three goal categories for the FMCW radar module. Category I involves post-measurement data processing. This means that signals from the radar module will be recorded, the radar will be turned off, and then the recorded signal will be run through a program to produce the desired measurements. The Category I goals are to produce range readings for people walking in an Engineering I hallway and to produce velocity readings for cars traveling on Pegasus Drive.

The Category II goals are exactly the same as the team's Category I goals, except rather than recording the radar signals and post-processing them, the radar signals will be processed in real time. This means the range readings for people walking in an Engineering I hallway and the velocity readings for cars traveling on Pegasus Drive must be generated and displayed in real time.

Category III, the final goal category, involves using the real time Category II results as the input to a control system. This control system can be of any nature, whether this be hardware, software, embedded in the FMCW radar module or external. The idea is to create a reactive system that visualizes changes in the radar module's maximum detected velocity and maximum detected range at any given moment.

There are several objectives that must be achieved in order for these goals to be met. The first objective is to update the low-frequency portion of MIT's Laptop Based radar, the design for which is available online. Our team has been donated an already assembled, operational version of the high-frequency subsystem for this design. As the bridge between the high-frequency subsystem and the data processing subsystem for the FMCW radar module, it is important that key aspects of the low-frequency subsystem are properly updated such that it best suits our overall system design.

Additional objectives our team must achieve include the following: updating MIT's MATLAB code for post-measurement range and velocity generation; designing PCBs for the system electronics; assembling, integrating, and testing

individual subsystems; conducting an iterative system integration, culminating in a final system integration and test; designing a USB interface between the radar module and host device; designing a functional, user-friendly API for real-time module control and signal processing; and designing a control system that is driven by the FMCW radar module output measurements.

III. Requirement Specifications

There are both qualitative and quantitative requirement specifications that our project should meet to guarantee optimal operation. The qualitative requirements are that the power supply should be portable and integrated into the module; the frequency of operation should be within an ISM frequency band to avoid the need for an FCC license to operate the device; and the connection between the radar module and the host device must be USB-A. The USB interface is to allow the radar module to easily plug into most laptop or desktop host computers.

In addition to these qualitative requirements, the quantitative requirements for the project are shown in Table I.

Table I
Quantitative Requirement Specifications

System Characteristic	Value
Measurement Error	+/- 2 meters
Maximum Operating Distance	≥ 50 meters
Cost	≤ $800
Physical Volume	≤ 0.5 cubic meters
Operating Frequency	≥ 2 GHz
Output Power	≥ 10 milliwatts
Software Lag Time	≤ 3 seconds
Weight	≤ 3 kilograms

IV. System Overview

Defining and aligning with our standards will ensure that our project will remain safe and reliable during operation. We primarily needed to consider our hardware standards for the radar subsystem, the software standards for the software system, and the hybrid standards for the data processing system.

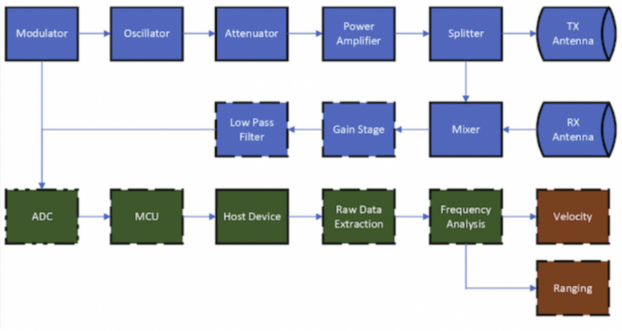

Figure 1: Overall System Diagram

A. Antenna System

Our antennas are made of cans with an embedded wire carefully placed inside of the can. If a wire is placed on a metal wall, the antenna radiation will have a phase shift of 180 degrees. If we want our radiated energy to be efficiently directed in a specific direction, we would place our antenna a quarter-wavelength away from the metal wall as shown in Figure 2, causing the phase shift to be 360 degrees. This antenna system would function as a circular waveguide in TE11 mode.

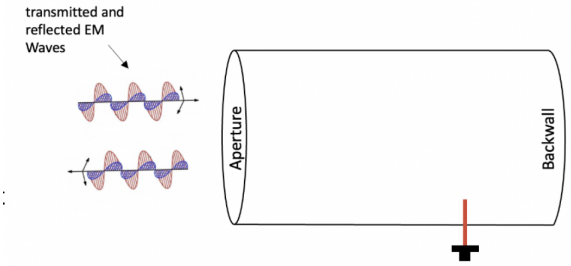

Figure 2: Antenna Representation

B. RF Subsystem, High Frequency

The high-frequency RF subsystem is a series of components that changes either the frequency or the power of the input signal. This series includes the

transmit and receive antennas, which introduce power and frequency changes of the signal via environmental interaction. Both the input to and the output from the high-frequency RF subsystem are connected to the low-frequency RF subsystem. In particular, the input to the high-frequency RF subsystem is a varying voltage from the modulator circuit, to be discussed in the next section.

Figure 3 shows the integrated circuit packages used in the high-frequency RF subsystem. The input from the low-frequency RF subsystem is fed into the oscillator (upper left). The signal splits off to the transmit antenna (upper right) from one port of the splitter. The receive antenna feeds into the LNA at the bottom right of the figure, and the output of the high-frequency RF subsystem comes from the mixer at the bottom.

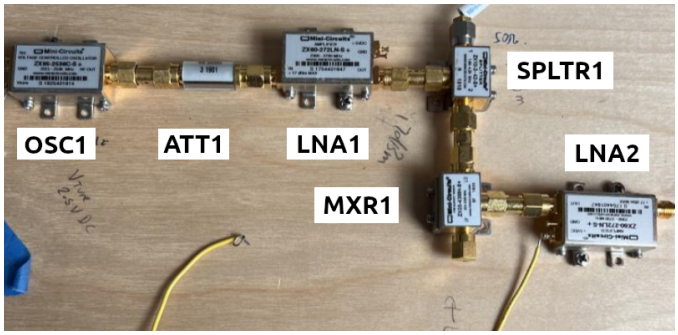

Figure 3: High-frequency RF Subsystem Integrated Circuits

B. RF Subsystem, Low Frequency

The low-frequency portion of the RF subsystem consists of the modulator circuit, the low-pass filter and the gain stage. The modulator circuit generates the driving signal for the oscillator in the high-frequency RF subsystem. The gain stage and low pass filter are used to process the output signal from the RF mixer. Figure 4 shows the printed circuit boards used for the low-frequency RF subsystem. Note that the gain stage and low pass filter share an IC and are therefore on the same board.

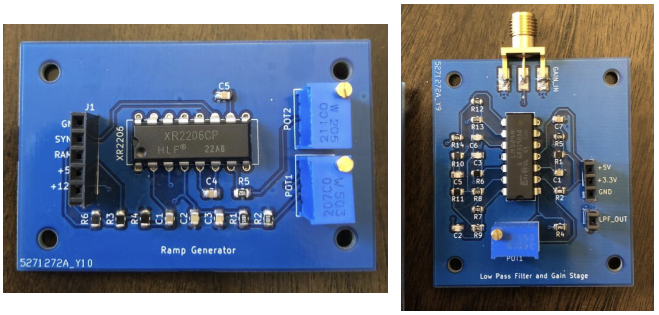

Figure 4: (left) Modulator PCB; (right) Low Pass Filter and Gain Stage PCB

D. Additional Constraints

The main restraints concerning our system components were cost, PCB design consideration and complexity.

The high cost of the RF signal processing components will be the cause of the majority of the cost restraint of the system. Regarding our PCB design considerations, we needed to be mindful of factors such as interconnectivity, sizing, and proper power supply. Additionally, an SMA connector will be connected to the gain stage/low pass filter, so we have to make sure the interface is properly made.

V. RF Subsystem - High Frequency

The high-frequency portion of the RF subsystem is a modified direct conversion transceiver architecture that uses a voltage controlled oscillator (VCO) to initially generate a high frequency signal. That signal is both attenuated and amplified before being sent to the transmit antenna. The signal re-enters the system through the receive antenna and is then compared to the transmit signal by the use of a mixer.

A diagram of this system is shown below in Figure 5. The oscillator, driven by the modulator circuit's output voltage, generates a high frequency signal. The oscillator is followed by an attenuator which weakens the signal strength before it is input to the power amplifier. This is to prevent any damage to the amplifier, in the event the signal is too strong. We are then presented the splitter which splits the signal between the mixer and the transmission antenna, concluding the transmission portion on the RF front end.

Next is the receiving portion of the high-frequency RF subsystem. The input signal is from the receive

antenna. Because the signal loses significant power as it travels through and interacts with the environment, the signal is immediately amplified by the second LNA in the system. Once the LNA amplifies this signal, it is downconverted by the mixer. The mixer effectively subtracts the original signal frequency from the received signal frequency. The output of the mixer is sent to the low-frequency RF subsystem for processing.

The components used for the high-frequency RF subsystem are commercial parts manufactured by Mini Circuits. Cost and packaging contributed significantly to the selection of these parts. They were readily available at no cost to the team from Dr. Xun Gong of UCF's ECE Department, and the lines between each part are 50 Ohm impedance matched. Potential alternatives included using RF PCBs or even fabricating our own circuit packages using distributed elements, but these could prove to be risky due to potential issues achieving the necessary specifications. Using the Mini Circuits parts provides stability and reliability within the RF subsystem, with the added benefit of allowing the team to focus on ensuring the RF parts are adequately tested and properly integrated into the system.

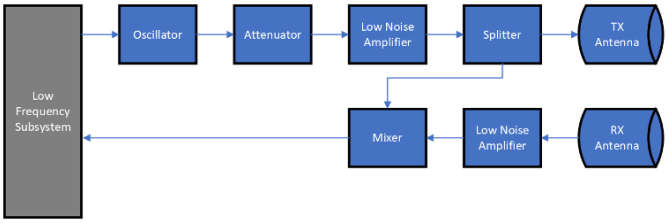

Figure 5: RF Subsystem- High-Frequency

VI. RF Subsystem - Low Frequency

As seen previously in Figure 5, the low frequency portion of the RF subsystem is critical to guide our overall transceiver architecture to both control the system and acquire the information being received.

As previously mentioned, the modulator circuit (Figure 6) generates the control voltage for the entire high-frequency RF subsystem. The IC chosen for the modulator circuit is the XR2206 function generator chip. The output ramp from this IC drives the voltage-controlled oscillator between two frequency limits: 2.402 GHz and 2.495 GHz, the limits of the 2.4 GHz ISM band. In order to do this, the ramp signal generated by the modulator must span from 2V to 3.2V, based on the characteristics of the oscillator.

The gain stage and low pass filter circuits, shown in Figures 7 and 8 respectively, are used to further process the received signal once it exits the mixer. They are used to ensure the information in the received signal is adequately preserved and amplified, which makes analyzing the signal in the digital domain much easier. The gain stage is used to increase the peak-to-peak voltage level of the signal from the mixer, and a low pass filter of the Sallen-Key topology is used to remove most frequencies above 15 kHz. Sallen-Keys are generally considered to be an easier topology to use since they require fewer components to create and are easier to tune based on different component values.

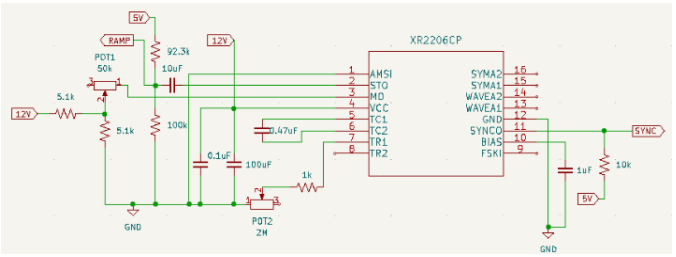

Figure 6: Modulator Circuit Schematic

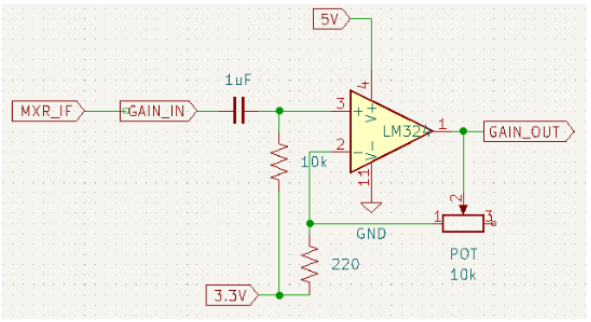

Figure 7: Gain Stage Schematic

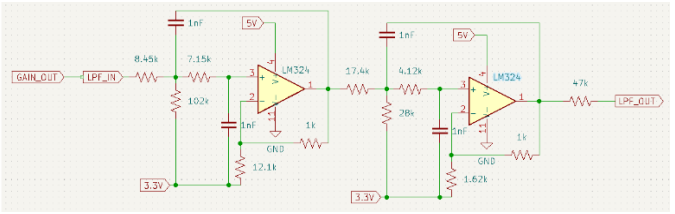

Figure 8: Low Pass Filter Circuit Schematic

VII. Data Processing Subsystem

Given that the low pass filter attenuates intermediate-frequency signals exceeding 15kHz, analog-to-digital conversion (ADC) of the filtered signal would require a sampling frequency of at least twice that of 15kHz. To satisfy this sampling frequency requirement, the filtered IF signal and sync signal are digitized by an external sound card with a sampling frequency of 44.1kHz, a 16-bit output, and a full-scale voltage of $\frac{4}{\sqrt{2}}$Vpp. Given this full-scale voltage the signal resolution is $\frac{4}{\sqrt{2}}/2^{16}/10^{-6} = 43.16\mu V$.

In our FMCW radar architecture velocity and ranging estimates are obtained by analyzing the "chirps" within a given "burst" using the fast Fourier transform. "Chirps" are composed by sweeping the TX frequency with the triangular waveform generated by the modulator, where sets of chirps comprise "bursts". Given the modulation period of 40ms and the sampling frequency of 44.1kHz, there are 1764 samples-per-chirp. With the ADC's sample size of 16 bits, each chirp has a size of 3528 bytes. These samples are produced by the left channel of the sound card. The composition of a burst may be visualized in Figure 9 below.

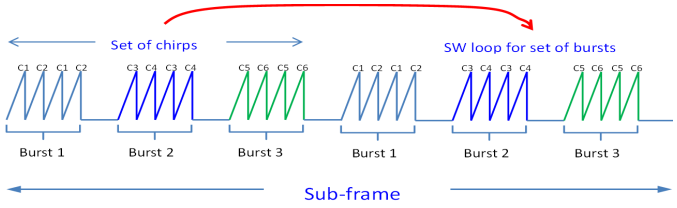

Figure 9: FMCW chirps and bursts

VIII. Software

Burst readings were acquired by activating the FMCW radar module and connecting a 3.5mm TRS jack to a computer for processing. These readings are stored in the WAV audio format to be read using two separate MATLAB programs: one for visualizing range readings; and one for visualizing velocity readings.

The ranging algorithm extracts the filtered IF signal from the left channel and the sync signal from the right channel of the audio recording. The rising edges of the sync signal are used to identify and extract the chirps from the filtered IF signal. These extracted chirps are inserted as rows into a chirp matrix. Neighboring chirps in the chirp matrix are subtracted for clutter attenuation purposes. The clutter-attenuated chirp matrix then has the inverse fast Fourier transform computed along its columns. The data in the chirp matrix is converted to the logarithmic scale by converting from V to dBV. This logarithmic data is plotted in a Range-Time-Intensity colormap as shown in Figure 10.

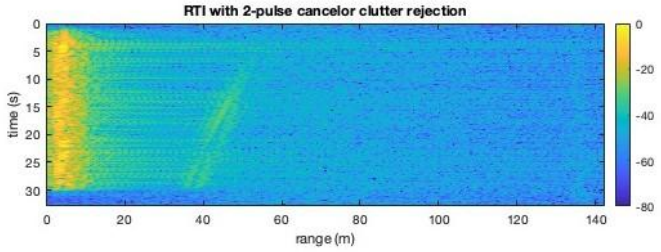

Figure 10: Range-Time-Intensity colormap

The velocity algorithm extracts the filtered IF signal from the left channel and the sync signal is excluded, as the data is acquired by tying the VTUNE pin of the voltage-controlled oscillator to a DC voltage. The samples-per-burst value is computed given the known sampling rate, samples-per-chirp, and chirps-per-burst. Bursts are extracted from the filtered IF signal and inserted as rows into the burst matrix. The inverse fast Fourier transform is computed along the columns of the burst matrix. The data in the burst matrix is converted to the logarithmic scale by converting from V to dBV. This logarithmic data is plotted in a Velocity-Time-Intensity colormap as shown in Figure 11.

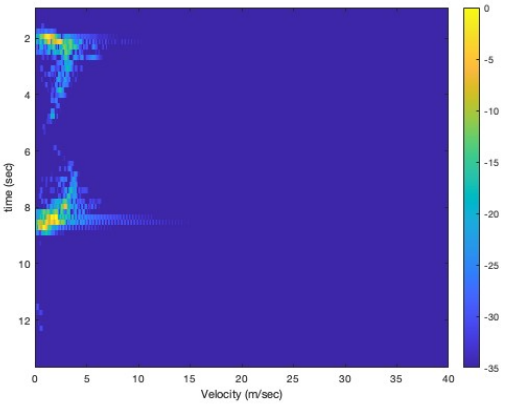

Figure 11: Velocity-Time-Intensity colormap.

IX. Power Supply

The power supply for the system, by the corresponding requirement specification, must be portable and integrated within the radar module. To meet this requirement, the power supply will be batteries on a printed circuit board. The supplied voltage and current must now be addressed.

A power analysis of the system components shows that three voltages are required: +3.3V, +5V and +12V. Additionally, the maximum total current being pulled is approximately 200 mA. In order to meet the 30 minute minimum runtime requirement, this means the power supply must have a capacity of at least 100 mAh. The chosen power supply will be 4 9-volt batteries in the configuration shown in Figure 12.

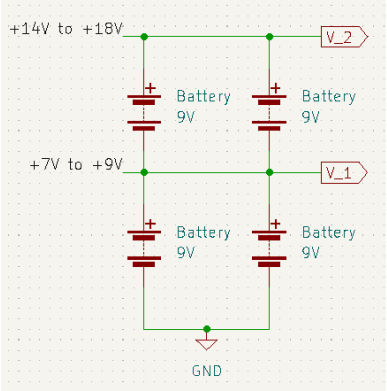

Figure 12: Battery Configuration

Each pair of 9-volt batteries provides 1200 mAh of capacity, allowing for approximately 6 hours of runtime for the radar module.

In order to provide +3.3V, +5V and +12V to the various system components, the two voltage levels V_1 and V_2 shown in Figure 12 must be dropped down. The integrated circuit that will be used for this purpose is the TPS5423, a buck voltage regulator with over 90 percent efficiency and a maximum output current of 2 amps. This is more than sufficient for our application.

+3.3V and +5V are generated from the first voltage level V_1. +12V is generated from the second voltage level V_2. The three voltage regulation circuits are in parallel. Aside from the resistors in the power supply circuits that determine the output voltage, it is important to note that the Schottky diode and inductor in each circuit can limit the maximum output current. Our circuits are limited to approximately 390mA due to the maximum current specification of the selected inductors.

X. Manufacturing and Assembly

A major aspect of the project manufacturing is the printed circuit boards. All boards (with the exception of the STM32 Nucleo development board) will be manufactured by JLCPCB and then subsequently assembled by our team.

To assemble the radar module, the following parts must be assembled, prepared or acquired as necessary: the five PCBs that have been discussed in earlier sections, the STM32 Nucleo development board, the Mini Circuits high-frequency RF circuit packages, the desired male SMA to male SMA connectors, the cantennas, a 30” by 30” by 0.25” plastic sheet, a plastic enclosing box with hinge brackets (optional), M3 standoffs with nuts, M3 bolts with nuts, #4 bolts with nuts, 2 copies of the 3D-printed antenna mounts designed by our team, 26 gauge wire, 22 gauge wire, heat shrink tubing, copper tape, 3 semi-rigid male to male SMA cables, and assorted length Dupont jumper wires for inter-PCB connections.

The first step of assembly is to attach the antenna mounts to the cantennas with the M3 bolts and nuts (see Figure 13). The next step is to assemble the Mini Circuits RF circuit packages as previously described in Section V - RF Subsystem - High Frequency. 26 gauge wire is wrapped around all the pins. Heat shrink is used to connect the 3 wires coming from the oscillator to 22 gauge wire, which is compatible with the PCB pin headers. Depending on the selection of right angle versus straight connectors, the orientation may be different, but Figure 13 shows an example using all straight connectors. The next step is to arrange all of the PCBs, the STM32 Nucleo and the cantennas on the plastic sheet around the Mini Circuits components as desired. The orientation of the cantennas should be as seen in Figure 13, the input of the LPF/Gain stage PCB should have sufficient clearance for the SMA input cable, and the power-in mini-USB port of the STM32 Nucleo should be easily accessible, as this port connects the module to the host device. Once the orientation of

all the components is decided, holes are drilled through the plastic sheet where all the necessary mounting holes must be. The circuit boards are mounted to the plastic chassis using the M3 standoffs and nuts, the antenna mounts are mounted using M3 bolts and nuts, and the Mini Circuit RF circuit packages are mounted using #4 bolts and nuts. All bolts and nuts should be tightened properly.

Lastly, the electronics and antennas are connected per the system design using Dupont wires, the 22 gauge wires from the oscillator, and the SMA cables. The optional plastic enclosure goes over everything except the antennas and is locked into place with brackets, which may require additional hardware.

To reduce potential issues caused by static electricity, one may choose to cover all surfaces of the plastic pieces in copper tape or anti-static spray.

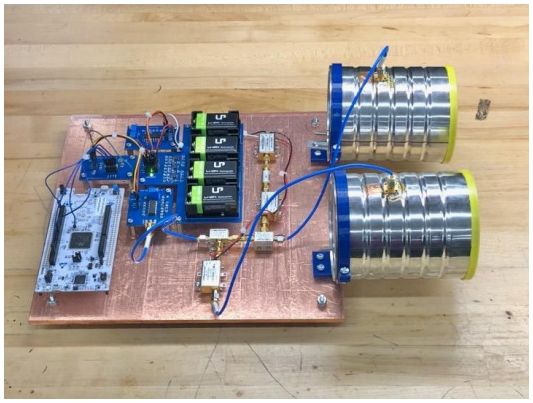

Figure 13: Assembled FMCW radar module

XI. Test and Evaluation

In order to ensure our system is functioning properly, there are two sets of tests our team must perform. The first set of tests is specific to each subsystem; they are to verify that individual PCBs and components are operational. The second set of tests will be for testing the entire system; they are to evaluate the overall performance and ensure requirement specifications are met.

We have already completed tests for the Gain Stage/Low-Pass Filter PCB, Modulator PCB, and high frequency RF components. The PCBs are all confirmed to be operational using Virtual Instrument Software Architecture (VISA) and Standard Commands for Programmable Instruments (SCPI) commands, which configure and extract data from the bench test equipment, namely the Rohde and Schwarz RTM3004 Oscilloscope and the Tektronix AFG3022B Function Generator. These test programs are written in Python using the PyVISA library and the data is plotted using both the Matplotlib and Scipy libraries.

The testing procedure for the high-frequency RF components involves the use of an additional piece of test equipment, the FPC1000 Spectrum Analyzer. This device is used to measure the output power and output frequency of the high-frequency RF components.

There are three sets of measurements taken for the high-frequency RF subsystem. The first set of measurements is the output signal from the splitter. Both the output frequency and output power are measured as the voltage at the Vtune pin of the oscillator is swept in 0.2 increments from 2V to 3.2V. The expected power and frequency can be determined from the RF component datasheets.

The other two sets of measurements are the output of the receive antenna and the output of the mixer, with the same DC sweep being performed at the Vtune pin of the oscillator.

The Low Pass Filter and Gain Stage PCB is confirmed to be operational by performing an AC sweep of the input and extracting the output waveform characteristics from the oscilloscope. Figure 14 below shows the AC sweep characterization of our LPF/Gain Stage PCB, which shows the filter does have a 15 kHz cutoff frequency as desired.

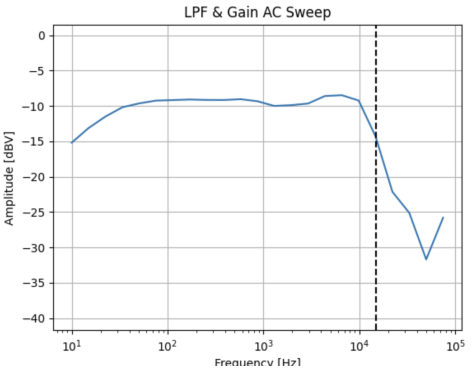

Figure 14: Characterizing the LPF and Gain AC Sweep

The Modulator PCB operation is verified by extracting the output triangle waveform and comparing it with a software-generated ideal waveform. Both the time domain and frequency domain representations are displayed in Figure 15.

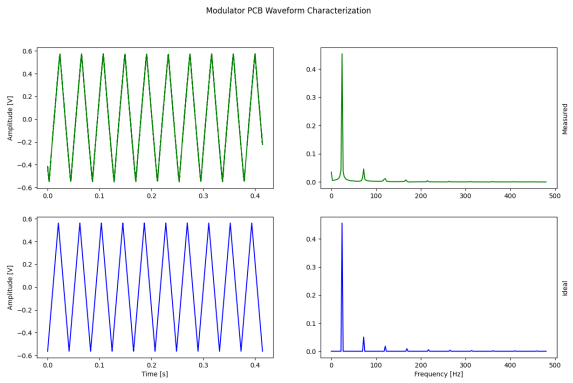

Figure 15: Modulator PCB Waveform Characterization

The power supply PCB is tested by measuring the voltage levels between its ground node and the +3.3V, +5V and +12V nodes. Additionally, a programmable load is used to verify the power supply is able to provide at least 150 mA of current, which is the current needed for our system to operate in its fully active state.

As aforementioned, additional tests are to be performed for the entire system to ensure the requirement specifications have been met. The physical volume and weight are easily determined with a measuring tape and scale, respectively. The operating frequency and transmit power are both determined by the splitter output, the test for which already measures these characteristics. The maximum operating distance and measurement error will be determined by using the device on targets of known velocity and/or range. A surveyor's wheel can be used to measure the actual distance between the module and a series of static targets. The series of measurements generated by our software can then be compared to the actual measurements to determine the measurement error. One of the targets must be at least 50 meters away to see if the maximum distance requirement is met.

A similar approach will be used to verify the velocity readings are accurate. Rather than using a surveyor's wheel to get the accurate measurements, a radar gun will be used.

The software lag time requirement will be verified by measuring two or more static targets in a single environment and rapidly turning the radar module from one target to the next. The lag time can be determined by how long it takes the software to generate the new, correct reading.

XII. Future Work

A. Digital Signal Processing

A dedicated ADC PCB was designed and manufactured for the project, however it had to be omitted due to time constraints. A PCM1802DBR from Texas Instruments was chosen targeting a 44.1kHz sampling frequency. This device is a 24-bit delta-sigma stereo ADC and yields accurate measurements by oversampling the input signals. To obtain the 44.1kHz sampling frequency the system clock was chosen to be 512 times greater, or 22.5792MHz, for which the XLH536022.579200X oscillator from Renesas Electronics was selected. The PCM1802DBR has a full-scale voltage of 3Vpp, such that the device has a resolution of $3/2^{24}/10^{-6} = 0.18\mu V$. The ADC schematic can be seen in Figure 16 below.

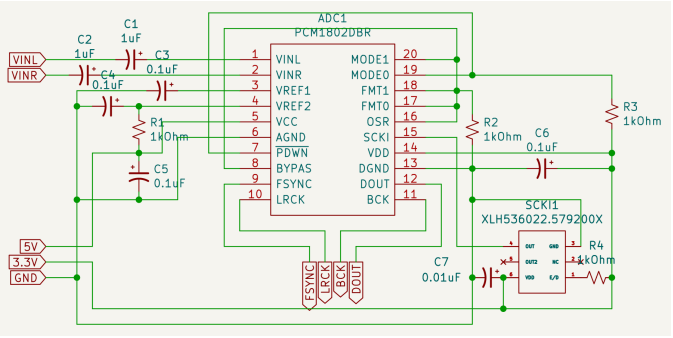

Figure 16: ADC Circuit

The ADC is configured to operate in "Master mode (512 fS)", where the pins "FSYNC", "LRCK", "BCK", and "DOUT" are outputs. As seen in Figure 17 below, "FSYNC" indicates that a sample is present for reading, "LRCK" indicates that the sample is for the left channel when HI and for the right channel when LO, "BCK" is the bit

clock where each rising edge indicates that a new bit is available for reading, and “DOUT” is the data output.

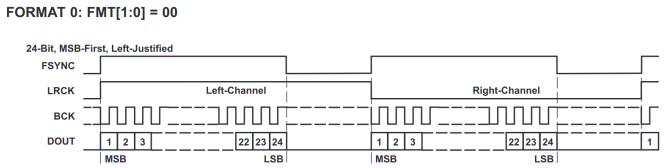

Figure 17: ADC Output Signals

To communicate with two separate Serial Peripheral Interface (SPI) receive-only slave mode devices, which are for the left and right channels, the output digital signals $F = FSYNC$ and $L = LRCK$ from the ADC must be converted to two separate “slave select” (SS) signals. The “left slave select” (LSS) is obtained with the Boolean expression $F \wedge L$ and the “right slave select” (RSS) is obtained with the Boolean expression $F \wedge \neg L$. To achieve this an SN74ALS804AN 6-gate NAND driver from Texas Instruments is used. The equivalent Boolean expressions using NAND operations are shown below.

$$LSS = \neg[\neg(F \wedge L) \wedge \neg(F \wedge L)]$$
$$= F \wedge L$$
$$RSS = \neg[\neg(F \wedge \neg(L \wedge L)) \wedge \neg(F \wedge \neg(L \wedge L$$
$$= F \wedge \neg L$$

The ADC SPI circuit is shown in Figure 18 below. As indicated by the Boolean expressions for both “LSS” and “RSS”, only 5 of the 6 NAND gates are used. The resulting outputs are the following: “LSS”, “LCLK”, and “LMOSI”; and “RSS”, “RCLK”, and “RMOSI”.

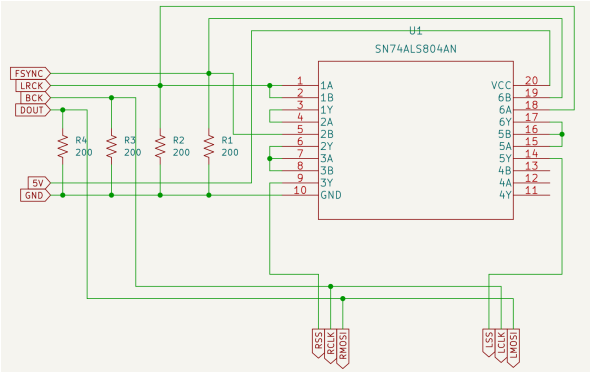

Figure 18: ADC SPI Circuit

The ADC PCB is confirmed to be operational by extracting the output data from an oscilloscope and converting the data to signed, scaled decimal values in Excel. Figure 19 shows an example test result, confirming that the analog waveform characteristics are preserved after digitization.

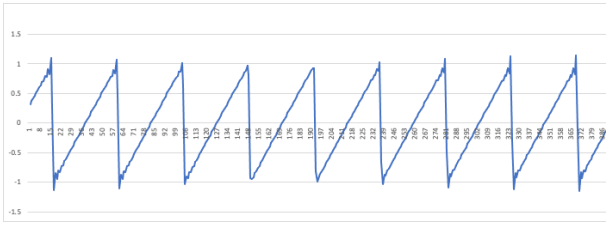

Figure 19: Digitized 1 kHz, 2 Vpp Ramp

B. Software

A Source Development Kit (SDK) that implements the Ripple API standard from the Consumer Technology Association was implemented but unused due to the omission of the dedicated ADC PCB. Ripple is an open radar API standard that enables hardware-software interoperability for consumer radar applications and allows for the deployment of unique configurations to the radar module that determine its modes of operation. Ripple specifies a state machine for controlling which state the device is in at any point in time. The state machine consists of four states and six transitions. The four states are the following: “OFF” (the device is completely powered down), “IDLE” (the device is idle and may either become active or enter a low-power mode), “SLEEP” (the device is in a low-power mode), and “ACTIVE” (the device is actively transmitting and receiving). The six transitions are the following: “TurnOn” (“OFF” to “IDLE”), “TurnOff” (“IDLE” to “OFF”), “GoSleep” (“IDLE” to “SLEEP”), “WakeUp” (“SLEEP” to “IDLE”), “StartDataStreaming” (“IDLE” to “ACTIVE”), and “StopDataStreaming” (“ACTIVE” to “IDLE”). This state machine is visualized in Figure 20.

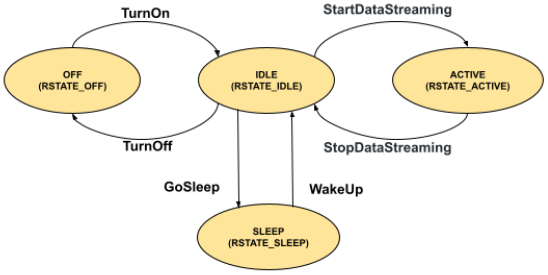

Figure 20: The Ripple state machine

This state machine is managed on the STM32H7A3ZI microcontroller. When the state machine is active, the microcontroller enables both SPI receive-only slave mode devices for the left and right channels, where the left channel consists of the radar signal and the right channel consists of the modulator synchronization signal. Each rising edge of the modulator synchronization signal indicates the start of a new chirp, which is configured as an external interrupt to begin a Direct Memory Access (DMA) data transfer. The number of chirps to be acquired is specified by the "chirps_per_burst" parameter. When this quantity of chirps has been acquired, the burst may be read from the STM32 module by the host.

Host-Module communication is facilitated using USB control data transfers and bulk data transfers. Control data transfers are used to configure the module's parameters, activate and deactivate module configurations, and transition between states. Bulk data transfers are used to read burst data from the module.

A graphical user interface (GUI) will demonstrate usage of the FMCW radar module SDK. This GUI will be implemented using the Visualization Tool Kit (VTK) and will allow for module control and velocity and ranging visualization in the form of a heatmap. Velocity and ranging may be extracted by performing a two-dimensional fast Fourier transform on the burst data. A mock-up of the proposed GUI is visualized in Figure 21.

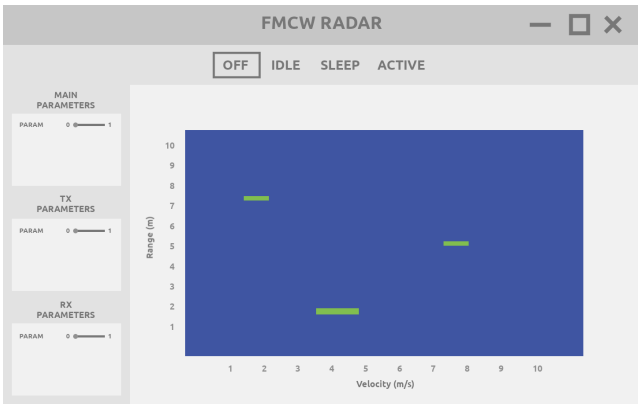

Figure 21: FMCW radar GUI

Acknowledgment

The team would like to thank Dr. Xun Gong of UCF's Electrical and Computer Engineering department for donating the Mini Circuits components and antennas used in the high-frequency RF subsystem.

This project is based on the Massachusetts Institute of Technology's Laptop-Based Radar for ranging, doppler, and SAR applications. The design and supporting documentation can be found in the corresponding MITOpenCourseware.

Team Members

Mikayla is currently a senior at the University of Central Florida. She will be graduating with a Bachelor of Science in Electrical Engineering and a minor in Intelligent Robotic Systems in Spring of 2023. After graduation, she will be working as a summer intern at Northrop Grumman Corporation. She plans to pursue a master's degree in Electrical Engineering at Florida State University in Fall of 2023.

Casey Sanchez will be graduating from the University of Central Florida with a Bachelor of Science in Electrical Engineering in Spring of 2023. He is a loving husband and father of three children: Fynn, 6; Ezra, 2; and Adalyn, 1. He has interned at Renesas Electronics as a Test Engineer where he has an offer pending graduation.

Sebastian Peralta is a senior at the University of Central Florida. He will be graduating with a Bachelor of Science in Electrical Engineering in Spring of 2023. He is currently an intern at NASA Goddard Institute of Space Studies, and is excited to see what the future will bring.

Fahim Ahmed is a driven and accomplished electrical engineer who will be completing his Bachelor of Science in Electrical Engineering (BSEE) at the University of Central Florida in Spring 2023. He has gained valuable industry experience in RF and Electrical systems through his work at Northrop Grumman and Exolith Lab, where he has contributed to the development of cutting-edge technology. This summer, Fahim will be interning at MIT Lincoln Laboratory, further expanding his knowledge and skills in the field. Looking to the future, he is excited to pursue his Masters in Electrical Engineering this fall at UCF, as he continues to advance his career in the field.