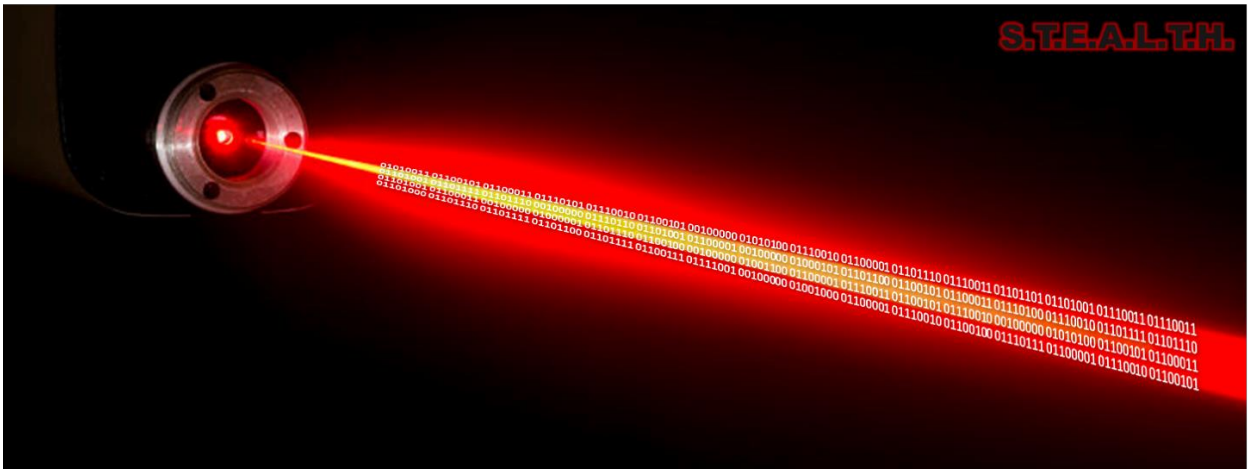
Senior Design 2 Final Draft

# S.T.E.A.L.T.H.

Secure Transmission via Electronic And Laser Technology Hardware

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# 1.0 Executive Summary

In the era of information, the capability to transmit and receive information is critical. In a world full of malicious actors, proactive vigilance is required to keep sensitive information out of the wrong hands. Different information communication use cases require different approaches to keeping information safe. One such potential method is optical communication, which carries with it some unique benefits over more commonly used wireless communication protocols. A point-to-point free space optical communication system offers high potential wireless range. Moreover, a directed optical system offers inherent resiliency to detection and signal interception.

We propose the creation of a self-contained free space optical communication system that is optimized to be light weight, low power, and compact. Optimization of these parameters enables the inclusion of such a system on aerial platforms to aid in meeting their communication needs. The primary objective of this system is to successfully communicate information from one microcontroller to another optically via laser amplitude modulation. The scope of the envisioned finished product does not include alignment, beam directing, and testing on aerial platforms, but rather should serve as a ground-based proof of concept whose parameters are constrained to be compatible with the requirements for potential inclusion in a drone payload.

In this report we outline the design and planning process for S.T.E.A.L.T.H. We will first lay out the background of information on the evolution of telecommunication technology to reach the point of free space optical solutions. This includes definition of what types of new problems can be solved by the further evolution of such technologies, which S.T.E.A.L.T.H. hopes to contribute to. Next we will specify the goals we wish to accomplish with the S.T.E.A.L.T.H. system in addition to a statement of the design objectives, requirements, and constraints that must be met to successfully reach our goals. Following the project layout, we will discuss preliminary research that was done to investigate similar and tangential technologies. Finally, we will explain how our technology investigation and research has informed our part and component selection strategy, and how those components will fit into the overall system design in order to develop a fully realized free space optical communication system prototype.

# 2.0 Project Description

In order to solve the requisite problems to complete the design process, we had to first establish what we could expect those problems to be. This required laying out our goals for system functionality and capability in addition to specifying the requirements the system must achieve to meet those goals as well as associated standards.

# 2.1 Project Motivation

Throughout their history, advancements in telecommunication devices have had great impacts on shaping the world as we experience it today. Telecommunications play a vital role in our everyday lives. We have a tendency to interface with advanced protocols so often without even realizing it nowadays that we likely take for granted how far technology had to progress to get to where it currently is. So many steps had to be taken for humanity to go from the telegraph, to the landline telephone, to the complex and compact wireless devices we use today. The use of optics in communication is not even knew, as for some time fiber optic communication networks have allowed numerous places around the world to enjoy faster internet speeds than previously available. The validation of the benefits of sending information via an optical signal has led us to a newer frontier in the realm of telecommunications: the domain of modern day free space optical communications. The goal of such a communication protocol is to enjoy the benefits experienced by using fiber optics to communicate bits of information using light, while also eliminating the need for a physical wired link. This evolution is nearly analogous to the jump from wired phones to cell phones.

Free space optical communication systems already exist however, but they are often designed for a fixed point to point link, such as in the case of so-called ‘last mile” systems. As a result of not needing to move around, these systems can be quite large, heavy, and sometimes even have higher power consumption needs relatively speaking. Similarly, to cellphones who were able to take steps since their inception days in order to progress towards a smaller, more portable, and convenient form factor, S.T.E.A.L.T.H seeks to provide a solution that moves optical communication systems in a similar direction. This portability could allow S.T.E.A.L.T.H. to solve a multitude of new problems associated with other technology becoming increasingly portable, but still having their own communication needs that ideally shouldn’t have to result in a great sacrifice to form factor. Furthermore, as technology advances, the ability of malicious actors to intercept and interfere with communication and data transmission becomes greater. S.T.E.A.L.T.H., as well as other free space optical communications systems benefit from the point-to-point nature of their optical links, inherently increasing security of the link as a function of difficulty to intercept.

## 2.2 Goals and Objectives

The core application or “problem to solve” behind the motivation of our proposed S.T.E.A.L.T.H. system, is to enable small aerial platforms such as fixed wing UAV’s to communicate wirelessly while enjoying the range, data speed, and security benefits of a point to point optical link. With that use case in mind, the S.T.E.A.L.T.H. system has been designed with the following goals and objectives to accommodate those associated needs:

-The system should be compact enough to be portable. This enables the system to be used for multiple types of applications including retrofitting to be mounted onto moving platforms.

-Similarly, in order to achieve portability, the system needs to be lightweight. Especially in the case of use in aerial platforms, the system must meet the weight requirements of a given payload in order to be considered a viable solution.

-The system should be able to transmit data accurately. This means that the estimated Bit Error Rate (BER) of the system must meet some minimum requirement to ensure the integrity of data on the receiving end.

-Operation of the system must be eye safe. Any system intended for outdoor use that could potentially be shined upwards must meet requirements to not only be safe to the user, but also potentially other people caught in the line of site. This is especially true for, but not limited to, the case of pilots of manned aircraft.

-The receiving end of the system must be sensitive enough to detect a signal from a comparatively small amount of irradiance at range so that the beam can be allowed to diverge to a large cross section at range to alleviate pointing requirements.

-The system must be able to be run off of a mobile power source. For our particular use case, the system should be designed to be compatible with a 24V Lithium Ion drone battery.

# 2.3 Requirement Specifications

The following table shows the requirements that were identified by the team. These requirements will form a basis for testing and measurements to check that the system is successful.

**Table 1:** Requirements for S.T.E.A.L.T.H. system and brief descriptions

| Requirement | Description |
|---|---|
| Weight | System shall weigh no more than 1 kg |
| Power Consumption | System shall consume no more than 2000 mW |
| Volumetric Footprint | System must fit within 500 $mm^3$ |
| Propagation Range | System shall successfully send and receive data over a distance exceeding 3 m |
| Wavelength | Beam wavelength will be within the infrared telecom band |
| Laser | System shall use a DFB directly modulated laser that emits light at 1550 nm |
| System Operating Frequency | System shall operate within the frequency range of 900 MHz to 1.5 GHz |
| Daylight Operation | System must be able to overcome the solar flux of 12 nm surrounding the 1550 nm wavelength |
| Optics | System requires collecting aperture of at least 50 mm in order to collect sufficient optical power |
| Electronics | System requires power amplification circuits between microcontrollers and photonic components |
| Battery | Design system to run off a drone battery that operates at 24 V at 5 mA |
| Component Housing | Design and 3D print housing for electronic, photonic, and optic components |

# 2.4 House of Quality

In Figure 1 below you will find the house of quality diagram, this helps focus our engineering efforts and visualize the association of marketing and engineering requirements. This house of quality figure shows the end goals of the consumer, this is where practical thinking comes in, everyone wants low cost and high performance, and fast. This is typically an unobtainable goal; this is the reason the house of quality exists. It bridges the gap between engineering and marketing showing the tradeoffs and relations between specific goals and realistic development. Some of our required objectives, seen on the left-hand side are, low power consumption, long range, and versatility. The engineering requirements can be found along the top of row, these outline what design goals we need to hit with consideration of the system in its entirety. This is done in the mind frame of being the designer of the system. These include weight, dimension, and the signal to noise ratio requirement. These are key goals that need to be met and weighed against the marketing requirements. The accuracy and versatility component will affect the power consumption and size sections as accuracy is the most important. Each set of specifications, engineering against marketing have conflicts and benefits. This is the importance of the house of quality to discuss what needs to be sacrificed to make the product marketable and feasible.


| Marketing Requirements | Engineering Requirements | | Weight | Dimensions | Power Consumption | Signal to Noise Ratio | Range |
|---|---|---|---|---|---|---|---|
| | | | - | - | + | + | + |
| | Component Cost (Low) | - | ↑ | ↑ | ↓↓ | ↑ | ↓↓ |
| | Line Of Sight Requirement | - | ↓ | ↓ | ↑↑ | ↑↑ | ↑↑ |
| | Secure | + | 0 | ↑ | ↑ | 0 | 0 |
| | Long Range | + | ↑↑ | ↑↑ | ↑↑ | ↑↑ | ↑↑ |
| | Component Power Requirement | - | ↑↑ | ↑↑ | ↑↑ | ↓↓ | ↑↑ |
| | Microcontroller Versatility | + | ↑ | ↑ | ↑ | 0 | 0 |
| | IR Laser | + | ↑ | ↑ | ↑↑ | ↑↑ | ↑↑ |
| | Target | | 500g | 150mm^3 | ~20W | 10Db | 1km |

| Legend : | |
|---|---|
| Strong Positive Correlation | ↑↑ |
| Positive Correlation | ↑ |
| Neutral Correlation | 0 |
| Strong Negative Correlation | ↓↓ |
| Strong Negative Correlation | ↓ |
| Positive Polarity | + |
| Negative Polarity | - |

**Figure 1:** House of Quality Diagram

# 3.0 Research Related to Project Definition

When working on the Divide and Conquer report, the team worked on a preliminary hardware block diagram that included the relevant components at the time of writing. The hardware requirements have not changed significantly since the Divide and Conquer assignment and the block diagram is shown in the figure below. This hardware block diagram also provides a breakdown of what each team member will focus on when researching for the project.

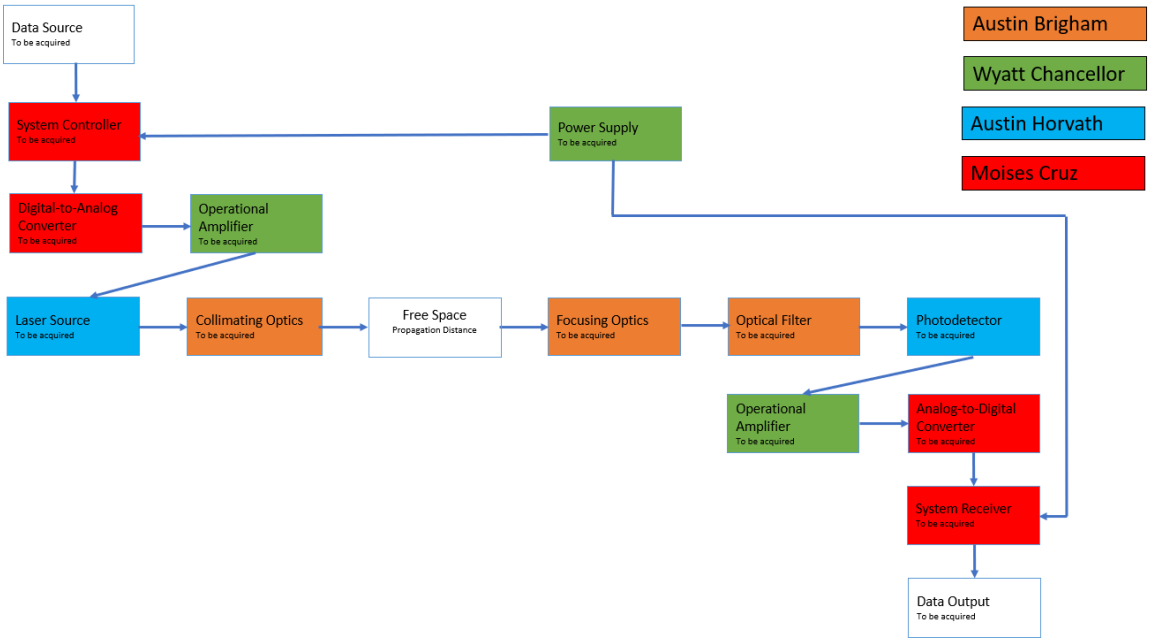



**Figure 2:** Hardware Block Diagram

This section will include similar products that exist, relevant technologies, component and parts selection, and any architectures and related diagrams. This will dive into preliminary research topics in hopes to find ideas, relevant technologies, and areas that can be improved upon from existing products. It will also investigate product selection reasoning and preliminary designs.

# 3.1 Existing Similar Projects and Products

In this section the search for similar products is shown and the reasoning for selecting that product is shown through explanation. As sources were found we choose the one with as much available information as possible into specification and design material. Typically, industrial vendors divulge as much information as possible to the public in hopes an engineer will find and apply their product to a project. In the following sections the reasoning will be explained of what we gained by researching these existing products.

### 3.1.1 Koruza

The existing products we have come across have primarily been for industrial use. Such as the Koruza, this system is meant for point-to-point communication and only contains the systems necessary for an optical link. This was a good starting point as there aren't many products that are publicly available for drone or aerial applications. The company also has made their first version of the product an open-source project. This allowed us to research into specific components and see how they reached the end goal of a functional system.

Interestingly, the Koruza achieves its up to 1 Gbps optical link using a laser with a stated transmitted optical power of only 0-0.5 dBm (1-1.12 mW). This small amount of power is enough due to the limited pointing requirements of a fixed system such as the Koruza, who can afford to have and even benefit from using a laser with a small divergence angle of only 0.05 mrad (0.0029 degrees), which enables very small losses to irradiance at the advertised maximum reliable operation distance of 150 meters. The lasers used by the Koruza are lower power than ours by about a factor of 20, however our system is planned to have a divergence of 1 mrad, about 20 times that of the Koruza, to assist with pointing at range. Given that irradiance scales inversely with the square of the radius, which is proportional to divergence, the Koruza ought to have a higher irradiance at a given cross section along the beam making it easier to collect more power with their fixed system given the significantly lower pointing needs.

The Koruza has two models, one using a matched pair of laser diodes at 1330 nm and 1550 nm, and one using a matched pair of laser diodes at 1270 nm and 1310 nm. One of these laser diodes in the former model uses the same wavelength as our system sets out to, however all of the other operating wavelengths are shorter than ours. That is worth mentioning because importantly they are also shorter than 1400 nm, which is often cited as a threshold under which lasers are considered less eye safe.

The Koruza system is built around the Open Systems Interconnection (OSI) model, which characterizes the communication functions of telecommunication systems without worrying about how the systems themselves are built. In other words, OSI is a model that standardizes communication methods and ensures that there is interoperability between a variety of communication systems, regardless of hardware structure. The Koruza system uses a Raspberry Pi Compute Module 4 hardware. Such a powerful microcontroller is what enables it to process information at high speeds. This module allows engineers and programmers to use the powerful Raspberry Pi hardware and software and stack their own custom systems and solutions. It gives more options from a design standpoint.

For power requirements specifically this was a decent starting place as it allowed for analyzation of the power budget through components. We found that they utilized power over ethernet (POE) 24VDC (Volts Direct Current) for supply power

and a load of 3 watts. Which was beneficial as the design constraints require to be supplied from a 24VDC battery from a drone. Although this product contained more communication components than ours required, such as network switches and fiber couplers, it provided the team a good basis of understanding what is at play in a fully realized point-to-point free space optical communication system.

### 3.1.2 TereScope

Another existing product is the MRV TereScope series. This product is another industrial application technology. This system is marketed to city scape clients with needs of having multiple geographical locations connected to the same network. Touting security this system doesn't require a third party provider for the link to a remote server. This means that software security is not required in that link, therefore improving connection speeds overall. The power budget was very similar to the Koruza in being able to operate at 24VDC and having a load of 6 watts. This source focused more on engineering specifications with little design information. This benefited the team to be able to more thoroughly understand what parameters need to be thought of.

### 3.1.3 MOSTCOM

This next system is the most high-end design of the system found, it is for mobile mounting with transmission ranges of up to 20km. Has transmission speeds of up to 10Gbps. This appears to be for military application and has a power load of 80 watts. This product is an example of a system to strive for. The high-power load is due to the fact of the articulating base it has. Our system will be stationary in our mounting, reducing the load substantially for our design.

One existing system is made the Russian company MOSTCOM. They have a wide range of point-to-point free space optical communication products that include stationary terminals, space terminals, mobile terminals, and underwater terminals. This is a very established company, with partners including NASA, Massachusetts Institute of Technology, and NVision Group.

Their stationary terminal is made for outdoor use in applications like enterprise connectivity and outdoor wireless access. The different models have data rates that range from 1 Gbps to 30 Gbps. With a maximum propagation distance of 4400 m to 1500 m. The systems have a power consumption ranging from 46 W to 49 W. All of the systems weigh in at 9.4 kg. While these systems have large enough data rates, they are already preassembled and weigh too much for any applications of our project.

Their space terminals are made for outer space use in applications like intersatellite communication and in the Space-Earth channels. Since these

systems are made for space, the two products have the longest propagation distances of any product found of 5000 km and 50000 km. The 5000 km system has a data rate of 10 Gbps (with an available upgrade to 100 Gbps). The system weighs in at 16 kg, with a power consumption of 60 W. The 50000 km system has a data rate of 1.25 Gbps. It weighs in at 50 kg, with a power consumption of 100 W. These systems are will not be considered because our project is for on-earth operations.

The mobile terminals are made for high-speed communication channels between mobile objects, such as planes/jets, UAS, ships, and cars. This system also comes with armored cover up to 1 m thick. It are designed to be able to operate in almost any climate temperature ranging from -50 C to 60 C. The terminal has a maximum propagation distance of 20 km and weigh in at 20 kg. it has dimensions 300x570x300 mm, and power consumption of 80 W. While this system is the closest to our project design, it weighs too much for any applications we might want to put our system in. If we had access to a full-size military drone, then this would be considered; but we do not.

Not much is given for MOSTCOM's underwater terminals, as it is their newest system. They created this product to have applications in control of unmanned underwater vehicles as well as having a team of these vehicles being able to communicate with each other. The system had successful data propagation and receiving distance of 15 m. Our system is designed to operate out of water and at much longer distances, so the underwater terminals will not be considered.

## 3.2 Relevant Technologies

In the relevant technologies section, we will explore and compare our proposed system to existing solutions. These solutions include fiber optic, copper, and standard radio frequency communications. We will compare data transmission rates, losses over our goal distances, power required to transmit over these distances, along with some pros and cons compared to our proposed system.

### 3.2.1 Fiber-optic Cables

Fiber-optic communication is a method of sending information from one point to another via an optical glass-based fibers. This information is sent into the fiber in the form of modulated light pulses that can come from an LED or laser. The signal must be modulated to carry specific information. Fiber-optic communication has been slowly replacing copper cables as it has multiple advantages such as much higher bandwidth, can cover longer distances, and is immune to electromagnetic interference. Bell Labs achieved a world record bandwidth-distance of 100 petabit*kilometer per second using fiber-optic communication. These cables were first developed in the 1970s and have revolutionized the telecommunications industry. However, integrating fiber-optic into cities has proven to be quite a

challenge because of how much infrastructure needs to be built to support the demand of largely populated areas. But as time goes on, big cities are slowly coming into the fiber-optic age. In recent years, rolling out fibers to homes has actually dropped below the price of running copper-based networks. This is because the technology needed to mass production of fiber cables has been commercialized. The figure below shows a simple diagram of fiber-optic communication.

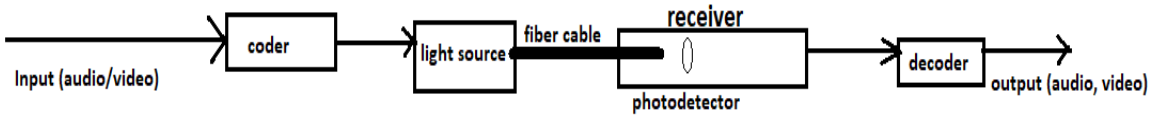



**Figure 3:** Fiber Optic Standard Configuration

Fiber optic communication today is the overall best form of hardwired communication. With speeds widely available today commonly reaching over 1Gbps. With higher speeds of 100Gbps applied in server rooms and larger network handling. Fiber optics also require less power to transmit data than other methods of data transmission. Typically fiber optic signals need to be boosted every 100 kilometers or less. [howstuffworks] In comparison our system aims to transmit 1Gbps through free space with an IR laser. With a distance of 1km. The optical output power of our system will need to be greater as there are more atmospheric conditions to deal with. A benefit to our system is the low cost of labor and materials. Fiber optics provided the ground work for a mobile system, from data handling protocols to laser development. In our design we will utilize systems similar to systems in fiber optic networks. [otelco]

## 3.2.2 Free-space Optical Communication

Free-space optical communication (FSO) is an optical communication method that utilizes light waves in free space, i.e. air, a vacuum, and outer space to transmit data. This differs from fiber-optic communication because is does not use a solid as the propagation medium. In 1880, Alexander Graham Bell and his assistant Charles Sumner Tainter created the photophone. This device basically functioned as a normal telephone, however, it used light to transmit the acoustic data rather than an electrical signal. Moving forward to the invention of lasers in the 1960s, these new devices would revolutionize FSO. As technology progresses, there are more and more practical applications for FSO where fiber cables are not feasible.

### 3.2.3 FSO vs. Fiber-optic

FSO does not need a medium to propagate, while fiber-optic communication requires a fiber cable. As of right now, no permit is requires to use FSO, but fiber cables require permits and permissions for digging to lay the cables. Installation of FSO systems is relatively quick and easy compared to installing fiber cables, which requires a multitude of equipment and infrastructure. Maintaining an FSO system is easy because it is only two terminals, the transmitting side and the receiving side. Maintaining a fiber cable can be extremely difficult because the cables are usually buried, especially for cables that are laid across oceans. FSO use a lot less material than cables, and usually cost less as a result. Companies that produce FSO systems usually make stationary and mobile systems. Each of these are easier to move than fiber cable systems, which once laid, cannot be moved. As of right now, fiber cables are capable of much higher data rates than FSOs. However, as technology progresses, FSO data rates are slowly catching up to fiber cables. FSO systems are coming to be capable of long-distance data transmission, whereas for a fiber cable to reach these distances, optical repeaters are needed to counteract signal attenuation. The main advantages of FSO systems is the price for the performance, but the signal can technically be intercepted, which makes this method slightly less secure. The main advantages of fiber-optic communication is that it is not susceptible to electromagnetic interference and it cannot be intercepted, meaning this method is more secure than FSO. However, signals sent through fiber cables are difficult to terminate.

### 3.2.4 Copper – Ethernet

When working with a high-speed optical system, it's relevant to look at previous technologies that have been in use to enable fast transmission of data. One such medium of transmission is copper cables. It is, however, more reliable than free-space transmissions since signals are connected directly through the copper. Today, more and more internet systems are moving away from copper and transitioning to fiber, which is a glass medium used to transmit light, instead of electricity.

Copper communication is the most devolved communication technology still being the most utilized today. Data transmission speeds can reach up to 40Gbps with new CAT8 cables today. [cablesandkits] The downside is that this can only be supported up to a maximum length of 30 meters.[fiberopticshare] Even the lower grade cables such as CAT6 ethernet cables have a data transmission speeds of 1000Mbps with distances of a maximum of 100m.[showmecables] Our proposed system will be able to transmit at comparable speeds of a CAT6 cable with ten times the distance.

## 3.2.5 Radio Frequency

This section will investigate Bluetooth, WiFi, and cellular transmission collectively. For Bluetooth the top of the line offers 2mbps up to 40m. That is why it is typically used for low power and low data rate transmission, like keyboards and headphones.[headphonesty]

WiFi technology has come along way with speeds reaching up to 40Gbps at 60GHz. In some industrial applications this can be broadcasted from between 300-500 meters in a focused beam.[60ghz]

Today's cellular speeds are slow even though they have come a long way relatively. In 2019 it was reported that the 5G network had three transmitting frequencies. The 600-700MHz band offered 30-250Mbps over hundreds of square miles from the tower. The next band at 2.5-3.5GHz can support 100-900Mbps over several square miles. The final band between millimeter wave / 24-39GHz with transmission speeds up to 1-3Gbps but only a one mile radius from the tower.[venturebeat]

The proposed design would not only be faster at our specified distances, it requires less power, and the signal is point-to-point. In the frame of security, the other signals are broadcasted over large areas, anyone with a powerful enough antenna and in proximity they will be able to pick that signal up easily. With the proposed design our IR laser system would be more power and error efficient and more resistant to being intercepted.

## 3.2.6 Controllers

Processing of data will be carried out by a microcontroller or an FPGA. A microcontroller is an integrated circuit that includes a central processing unit, memory, and an assortment of peripheral devices. Microcontrollers are an accessible way to design embedded systems by providing it instructions usually written in high-level languages like C/C++ or Python. They have a fixed hardware structure, meaning that all the attached components on the board, like the processor, memory, and I/O devices are predefined.

Field programmable gate arrays (FPGA) are circuits that are designed to be configured by the end-user after manufacturing. The architecture is different from a microcontroller in that an FPGA consists of configurable logic blocks, look-up tables, multiplexers, and flip-flops that allow the system to be configured depending on specific needs. This means that the hardware is specifically programmed on the device, rather than writing software like engineers would do with a microcontroller. FPGAs are programmed using hardware description languages like Verilog or VHDL. The choice of controller will be broken down in later sections.

### 3.2.7 Serializers & De-Serializers

With today's rapidly growing technologies, there is a desire to improve transmission speeds. New systems are able to use integrated circuits called serializers and de-serializers as a way to facilitate data transmission over a single line and reduce the number of input and output pins, as well as improving speeds of the serial stream. The serializer and deserializer will be employed in this design to increase transmission speeds from the system controller and the laser.

### 3.2.8 Analog-to-Digital Converter

In electronic systems, an analog-to-digital converter (ADC) is a block that converts an analog signal, such as audio or light, and translates it to a digital signal. This circuit will enable the S.T.E.A.L.T.H. system to convert the data transmitted from the laser (a light source) into a digital signal that can be interpreted by a microcontroller or an FPGA.

### 3.2.9 Digital-to-Analog Converter

Complementary in function to the ADC, a digital-to-analog converter (DAC) is a block that converts a digital signal into an analog signal. A digital signal is one that can be interpreted by computers, composed solely of 1's and 0's. Many components, however, are analog and cannot interpret digital information. Examples include speakers, which require an audio signal. Modulation of the laser used by the S.T.E.A.L.T.H. system might also need a DAC to function properly.

## 3.3 Strategic Components and Part Selection

This section will cover the decision making in our component selection process. The house of quality plays a role in our design by giving us parameters to keep in mind while designing. The following sections include major portions of our design including, parameters that were taken into consideration, and part comparison for each system goal. The first step in designing the S.T.E.A.L.T.H system is to research every aspect of it. This includes a combination of electrical, photonic, in optical parts.

### 3.3.1 Microcontroller Power Supply

In this sub-section multiple iterations of designs were created in hopes to find an optimal component that was also available for purchase. Each iteration was done with different parameters from the house of quality in consideration. This was done until a design was found that best satisfied most of the parameters. The power supply will be a typical 24VDC drone battery. For this system the design output

parameters are a 5VDC supplying 3A. This is sufficient to power the microcontroller and the associated components required for the system to function properly. This is also the largest load of our project coming to 15W. This means that this circuits efficiency is the most important parameter to design to achieve. With high circuit efficiency it will reduce the amount of excess power drain on the battery which will prolong the overall run time of the system. This is critical for the end stretch goal of being an aerial mounted system.

# 3.3.1.1 Design Option No.1

**Figure 4:** DC/DC Step-down Regulator TPS56637RPAR

The DC/DC step-sown regulator in this design is the TPS56637RPAR, this was chosen initially in hopes of being able to supply multiple circuits with one unit. Therefore, creating a smaller overall footprint for the power supply PCB for the 4 required circuits. The footprint of the supply circuit for just the microcontroller is at 229mm$^2$. The efficiency of the circuit is 93.7% with a BOM cost at $3.96. The efficiency of this circuit is critical as it is the largest load. Therefore, it was the most important parameter to satisfy. If multiple components end up being powered through this circuit at different voltage output levels the footprint will roughly grow by 100mm$^2$ per load fed. This is one of the leading options. This product was selected for its wide range of voltage input and output capability and 6A output capability, with our system being battery operated it is important to have the system be efficient through all possible voltage conditions. This component also had a 100% duty cycle meaning it would be cable of handling a continuous load without any down time.

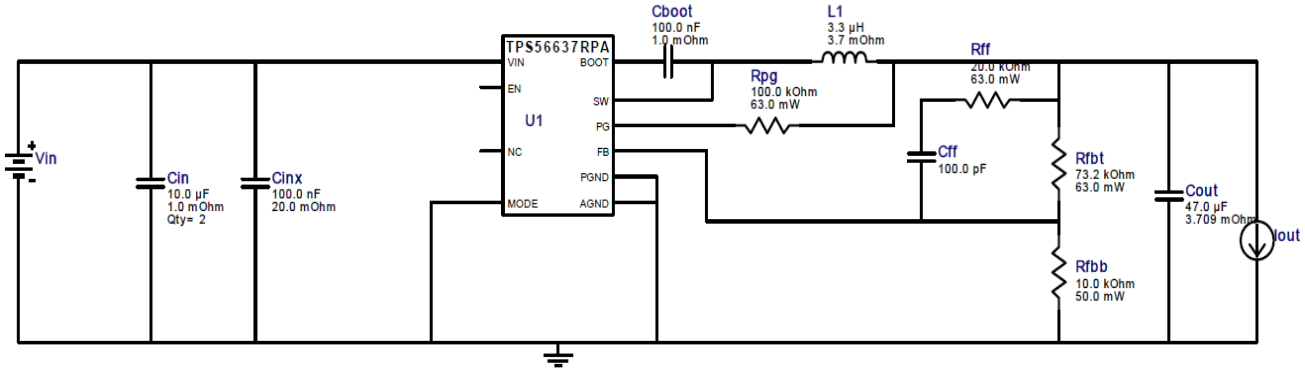



**Figure 5:** Power Design Option No.1 Circuit

# 3.1.1.2 Design Option No.2

**Figure 6:** DC/DC Step-down Regulator TPS552882RPMR

This next component was chosen as it had some integrated controls that might be helpful, and once again with aims to power more than one system. The TPS552882RPMR from TI is produced for automotive applications so it can handle a wide range of input and output voltages from 2.7V to 36V input, and 0.8V to 22V outputs. Along with a large maximum output current of 3A. This was a great fit for a whole system application along with a programmable switching frequency from 200kHz to 2.2MHz which is within our range of modulation that will be required. This component and associated circuit has a large footprint of 624mm$^2$ . This is almost too large of a footprint for just this circuit when we consider the other components that are going to be involved. This design produced an efficiency of 97%, making it the most efficient of the selections. The added footprint value is not worth the efficiency drain as the max load compared to the battery life there is room to spare. The price of this option came to $4.73 making it the most expensive of the options due to the two transistors.

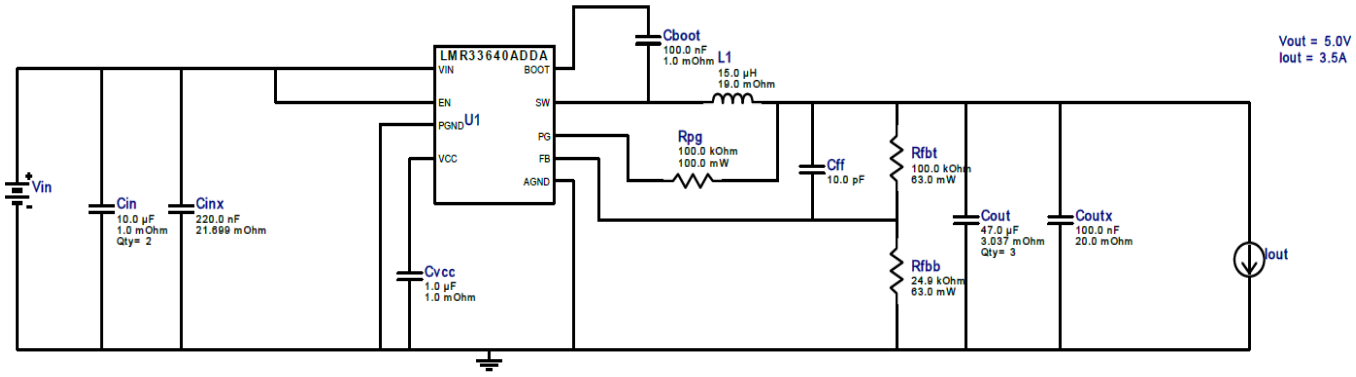



**Figure 7:** Power Design Option No.2 Circuit

# 3.1.1.3 Design Option No.3

Our final design for the microcontroller power supply circuit was controlled by available parts. The component chosen was the DC/DC step down regulator TPS54332DDAR from Texas Instruments. This circuit worked well for being the

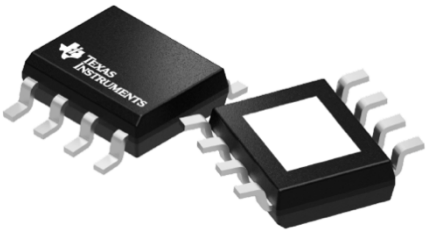



**Figure 8:** DC/DC Step-Down Regulator TPS54332DDAR

last resort option, it is a very small component which is good for size constraints. With a total BOM cost of $2.60, and the overall efficiency came to be 81.899%. The footprint of this circuit was kind of large at 384.0mm$^2$. As you can see there is an open EN pin below, this pin can either be configured to turn on through a command from the microcontroller, by floating the pin, or with a simple resistor circuit with a switch for manual control. For this application since the microcontroller is the load being supplied by it, the controller would not be able to send a signal to its own supply. Therefore the circuit will be controlled via a manual switch. This switch will act as the main switch to turn the component on as everything else will be configured to turn on via microcontroller GPIO signals. The final output at Iout below will be connected to a two pin plug that will then terminate to the 5V input power pins at the microcontroller. The Vin on the left will be supplied through a common bus on the combined power supply PCB that will be supplied from the drone battery. The metallic pad on the bottom of the converter is a thermal pad to keep the component at optimal temps. The PCB will be configured to this and additional heat shrinks will be supplied if needed.

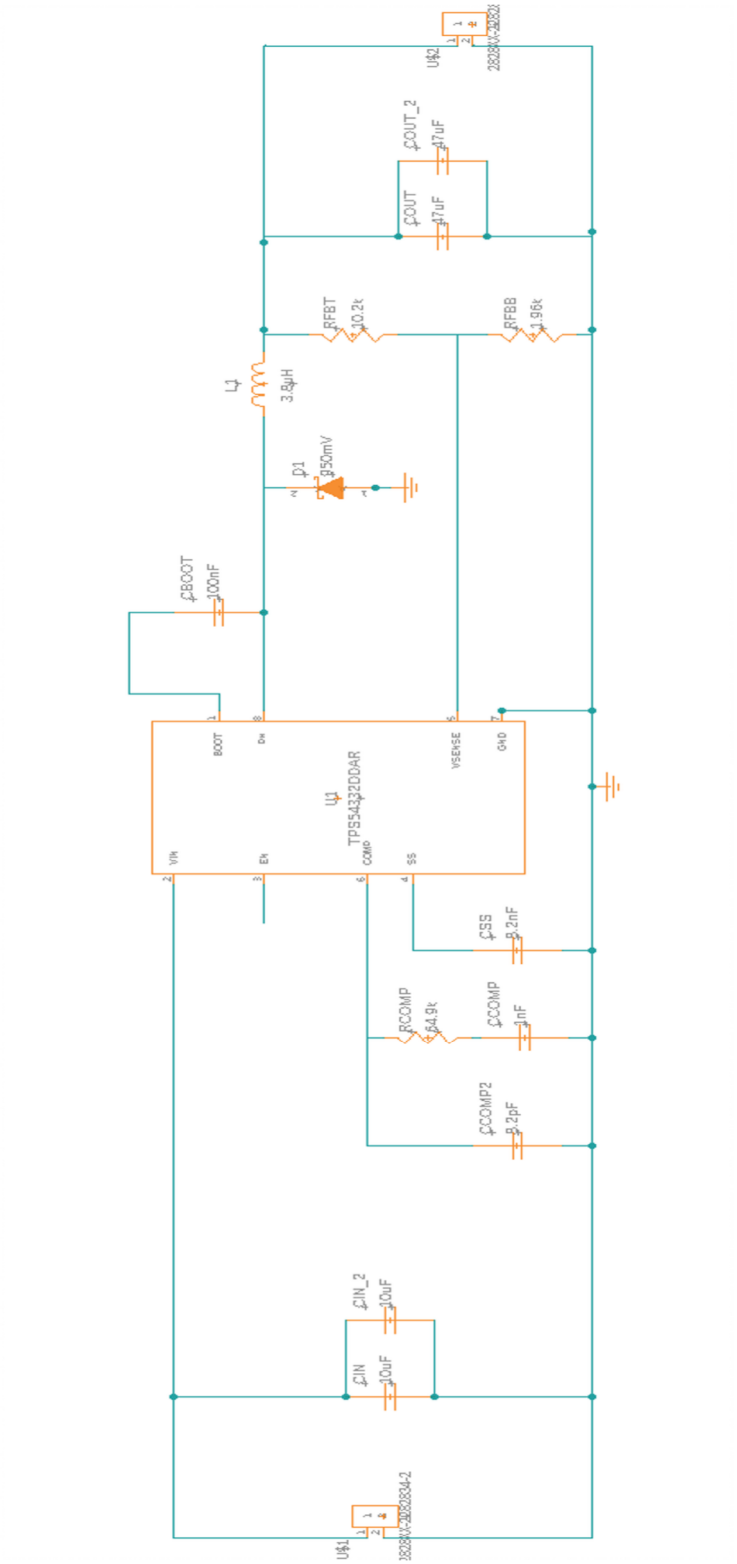



**Figure 9:** Microcontroller Final Power Supply Design

As you can see in the figure on the previous page, we have integrated pins to connect the battery input and the current output to the microcontrollers GIPO pins for power. The final PCB will be discussed later in the design section of the report.

# 3.3.2 Laser Power Supply

Similar to the previous section this portion overwent multiple iterations of design. For the laser power supply circuit efficiency was not a main concern as the maximum load is only 180mW at 1.2V. With the laser needing multiple surrounding components such as lenses it was critical to have as small as footprint as possible. With the global microchip shortage, part sourcing proved to be a more difficult task than anticipated. This has caused many of the circuits to less than optimal. This power circuit will act as the main supply only for the laser supply as the laser needs to modulate between 600MHz and 1.5GHz to achieve the necessary data transfer rates for our proposed speed. The control circuit will consist of a voltage controlled current source with a transistor able to switch at the required frequency.

# 3.3.2.1 Design Option No.1


**Figure 10:** DC/DC Step-down Regulator TPS552882RPMR

For this design I took into consideration of using the same component as one of the microcontroller power circuits with hopes of powering multiple devices with a single component to reduce overall sizes of electrical components. The TPS552882RPMR from TI is produced for automotive applications so it can handle a wide range of input and output voltages from 2.7V to 36V input, and 0.8V to 22V outputs. For this circuit I focused on the parameter of efficiency as size constraints would be reduced overall with a common component. This voltage converter prefers higher voltages for maximum efficiency, so the efficiency was not optimal at 70.21%. As aforementioned this is not outside reasonable as the load of the laser is relatively low. The overall bill of material cost is reasonable at only $4.50. This is high comparatively speaking but with it serving multiple loads the overall cost is

reduced. A design concern is whether the switching frequency of the power supply will be a factor with the control circuit mentioned earlier.

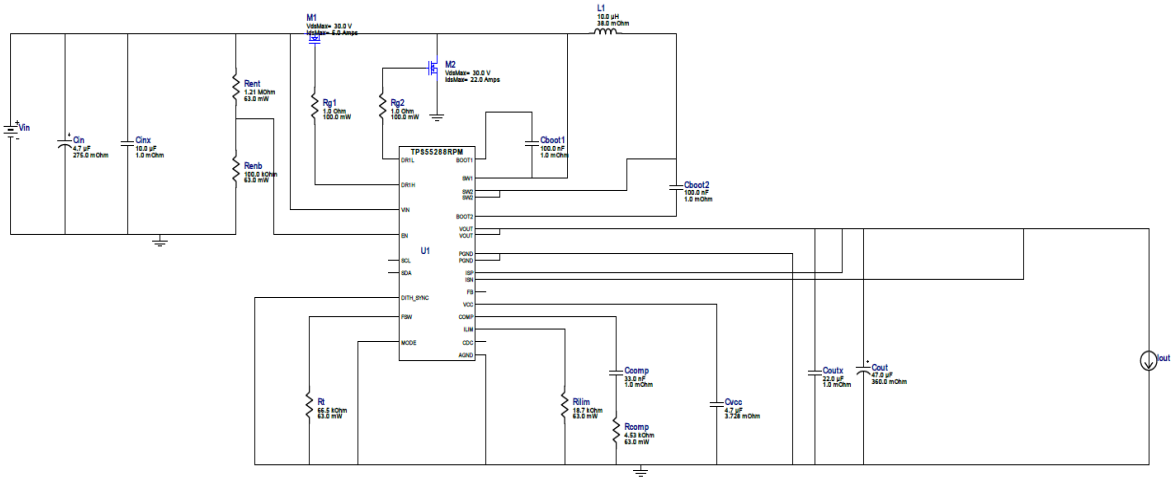



**Figure 11:** Laser Power Design Option No.1 Circuit

# 3.3.2.2 Design Option No.2

**Figure 12:** DC/DC Step-down Regulator TPS57040QDGQRQ1

For the final design option, it was chosen to focus purely on minimizing footprint. With no regard of availability, the TPS57040QDGQRQ1 was selected. This chip is advertised as a light load efficient module which fit the application. The complete circuit obtained a 190mm$^2$ overall footprint. With a BOM cost coming to a total of $5.38 this was on the more expensive end as the quality was also on the higher end. This is the smallest footprint design option making it something to consider if it were not for the long lead time. As seen below the “On order” shipping date is not until the end of January 2023. As senior design ends in the spring of 2022 I did not see the benefit of placing an order or considering this component any further.

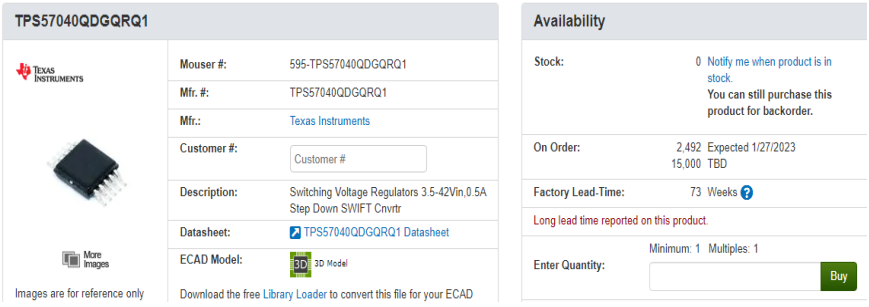



**Figure 13:** Component Availability Example

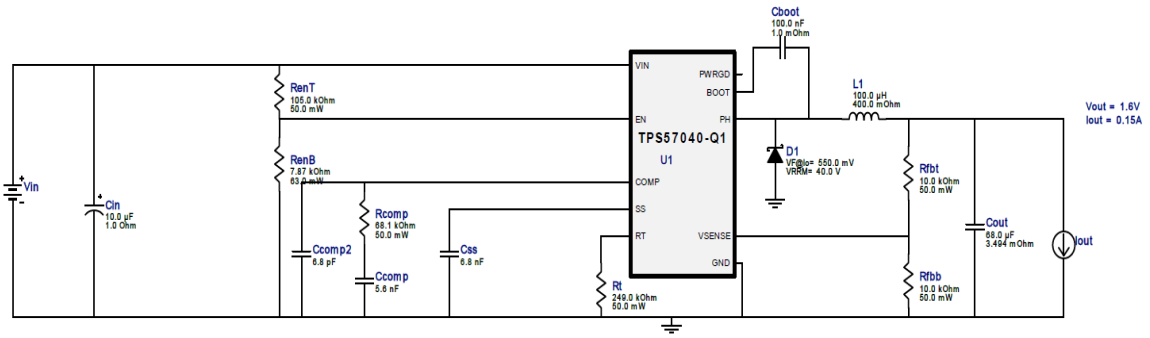



**Figure 14:** Laser Power Design Option No.3 Circuit

This was meant to showcase the lack of available quality components. Various designs would have made this circuit between 60-70% with a 100% duty cycle. With the available components the duty cycles are around 50-70%. Although the smaller duty cycle would be enough in a prototype setting of testing, in a consumer product this would not be acceptable due to the nature of the system running 100% of the time.

# 3.3.2.3 Design Option No.3

**Figure 15:** DC/DC Step-Down Regulator LM43600PWPR

Our final design for the laser power supply circuit was controlled by available parts as the previous section was. For this design the component selected was the DC/DC step down regulator LM43600PWPR from Texas Instruments. This circuit worked well for being the last resort option, it is a very small component which is good for size constraints. With a total BOM cost of $2.53, and the overall efficiency came to be 70.144%. The footprint of this circuit was fairly small at 197.0mm$^2$. There is an EN pin below for controlling the on or off state of the device, this pin can either be configured to turn on through a command from the microcontroller, or with a simple resistor circuit connected to Vin. For this application since the microcontroller will be on in when this system will be. Therefore the circuit will be controlled via a input voltage from the microcontroller GPIO pins. The final output at Iout below will be connected to a two pin plug that will then terminate to the 1.5V input power pins either directly to the laser or through a current modulator. The Vin on the left will be supplied through a common bus on the combined power supply PCB that will be supplied from the drone battery.

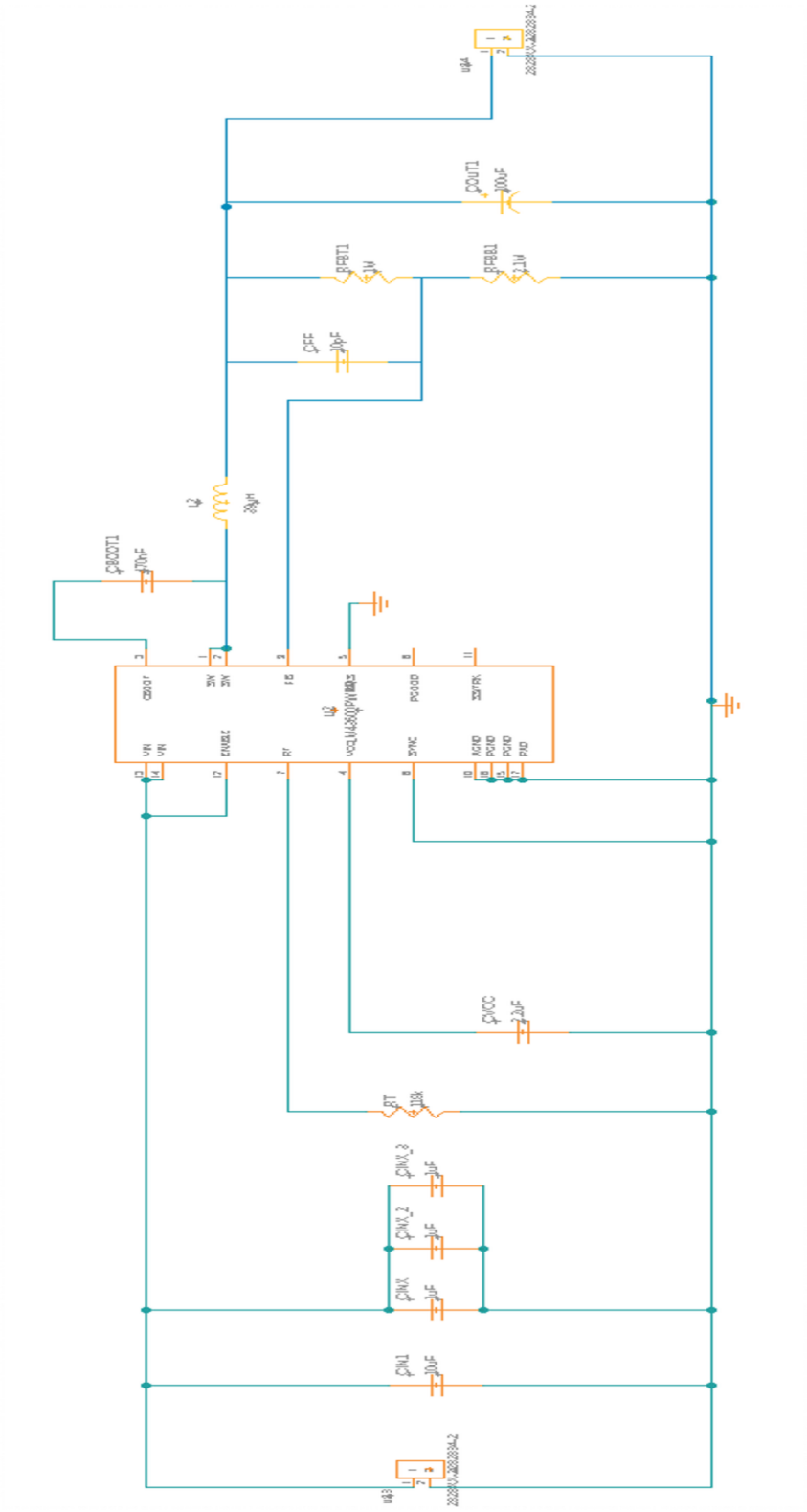


**Figure 16:** Final Laser Power Design Option No.3 Circuit

# 3.3.3 Thermoelectric Cooler Power Supply

The thermoelectric cooler (TEC) is integral to the laser as the output optical power is strongly affected with small changes in temperature. As these types of lasers are typically utilized on a bench top environment the controller typically regulates everything. In our application it was required to design each section individually. The TEC utilizes the piezoelectric effect which uses two dissimilar conductive materials and run current through them to create a temperature difference between the top and bottom surfaces.

As mentioned, this is usually controlled through a benchtop controller so a control circuit will be required to regulate the temperature measured via resistance at the thermistor. This will be covered in section XXXX. The TEC requires 1.4A at 2.5VDC giving us a load of 3.5W. This is the second largest load behind the microcontroller, and it is mounted on the laser. With that in mind the parameters of efficiency and footprint were optimized.

# 3.3.3.1 Design Option No.1

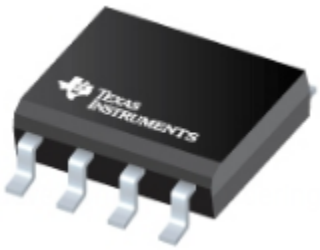


**Figure 17:** DC/DC Step-down Regulator TPS54332DDAR

The DC/DC step-sown regulator in this design is the TPS54332DDAR. This selection was based purely on availability of the component. This design came with a bill of material cost at $2.01. With a modest efficiency at 73.1% and a footprint of 213mm$^2$, this was the best middle ground between efficiency and footprint constraints. The optimized design for efficiency would only yield a 1.9% increase, and it would bring the footprint to a massive 769mm$^2$. This is a scenario where it is important to design with functional intention and reference the house of quality frequently.

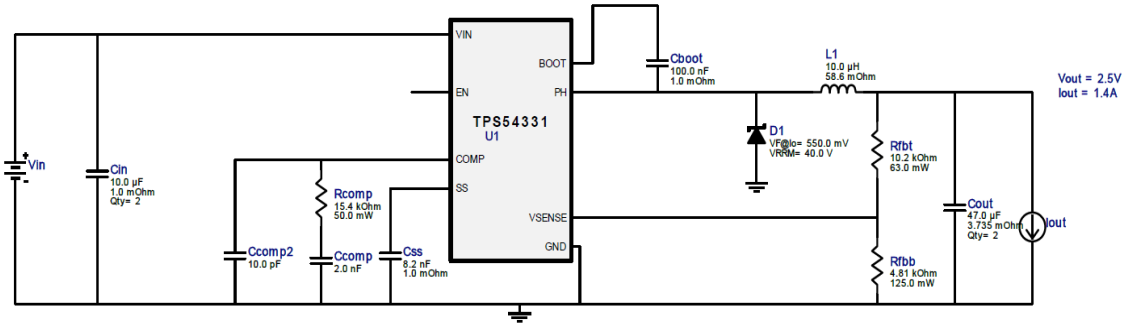



**Figure 18:** TEC Power Design Option No.1 Circuit

# 3.3.3.2 Design Option No.2

In this following design, I disregarded availability and investigated the best fit component in production. This brought me to the LM60430ARPKR, this unit is either a fairly new component to TI or they have not made any images available on there website. With this component footprint and efficiency would not be a concern. With a smaller footprint of 165mm$^2$, at that size this circuit would still outperform the available part by over 20% in efficiency. The LM60430ARPKR would operate at 93.4% efficiency. The bill of materials price comes to the a slightly higher value at $2.46 making it a much better option for the price increase if it were available.

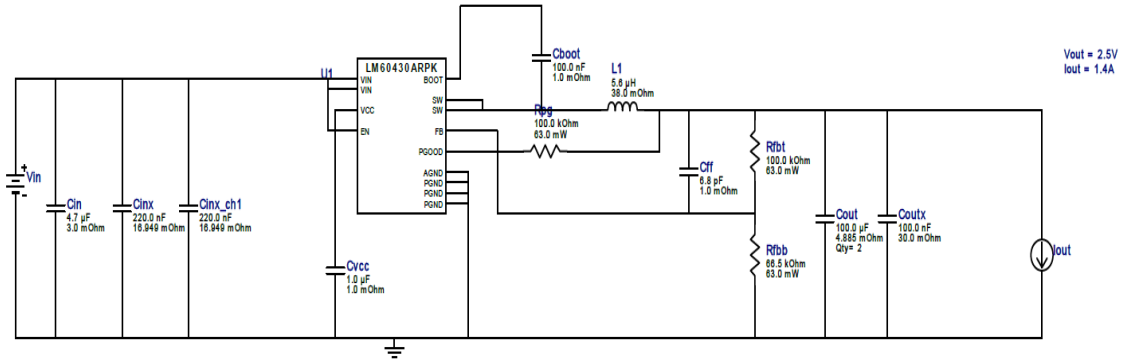



**Figure 19:** TEC Power Design Option No.2 Circuit

# 3.3.3.3 Design Option No.3

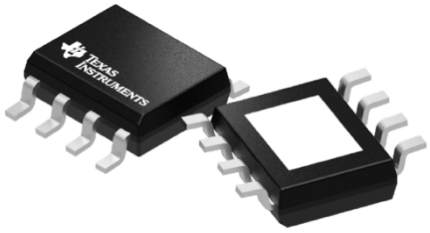


**Figure 20:** DC/DC Step-Down Regulator TPS54332DDAR

The selected final design for the TEC power supply circuit was dictated by the parts availability crisis in the microchip industry. For this design the component selected was the DC/DC step down regulator TPS54332DDAR from Texas Instruments. This design was comparable to our initial designs so this was not a bad component to be stuck with. The BOM cost came to be $2.01, and the overall efficiency came to be 73.094%. The footprint of this circuit was a decent size at 213.00mm$^2$ taking space constraints into consideration. EN pin on this device can be controlled through a pulldown voltage of 1.25V to disable it and anything above that to the value of Vin. For this application I intend to use a potentiometer and the integrated thermistor in the laser TEC. This will control the

input voltage to shut down above 3.5V. When the thermistor heats up this will cause the resistance to drop and the voltage will increase above 3.5 to the desired temperature. The temperature can be controlled with the potentiometer to adjust for the current environmental conditions. The Vin on the left of the circuit will be from the battery supply bus on the common PCB. The Iout will deliver 2.5V with 1.4A directly to the TEC. The benefit of this component is the high switching frequency so that it can keep the laser cool accurately. As you can see in the circuit below, the component says TPS54331, this is because for this circuit the TPS5432 variant of that chip did not want to load, this is a TI power designer malfunction and the component selected will work.

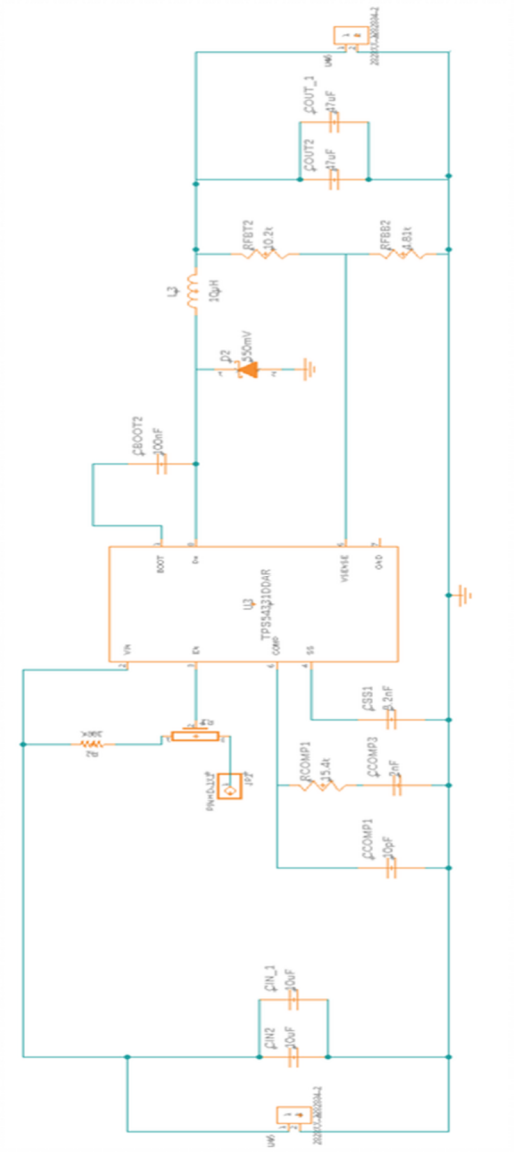


**Figure 21:** TEC Final Design

As we can see in the figure there is added pins to the final design so that interfacing with the physical components is much easier. The battery will be supplied at the

bottom of the wiring diagram and the top will be the out put to the TEC. If you look near the module itself you can see a variable resistor and this will help control the operating temperature of the Laser TEC. This is controlled by changing the voltage input into the module therefore reaching its cut off and cut on voltages. This will be described more later.

# 3.3.4 Photo Detector Power Supply

In the following section we will explore the power supply for the op amp and the photoreactor circuit. This circuit provides a reference voltage for the detector in order to operate properly. There is only one entry in this section as it was a straightforward design. Final PCB circuits will explained more later in the paper.

# 3.3.4.1 Electrical Final Photodetector OP-Amp

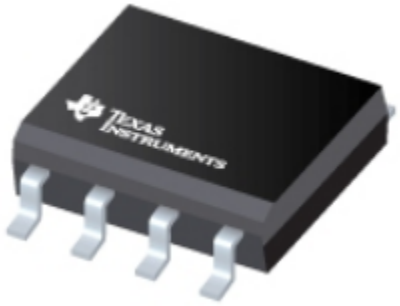


**Figure 22:** DC/DC Step-Down Regulator LMR23610ADDAR

This circuit was a little different than the others, first I will explain the power supply circuit and then how this component interfaces with the op-amp and the photodetector. The selected DC/DC voltage converter was selected for the availability and low output current. For this design the component selected was the DC/DC step down regulator LMR23610ADDAR from Texas Instruments. The BOM cost came to be $1.99, and the overall efficiency came to be 73.164%. The footprint of this circuit was a decent size at 195.00mm$^2$ taking space constraints into consideration. EN pin on this device can be controlled through a high and low voltage signal from a microcontroller or the main power supply. The Vin source will be from the drain battery and the left Iout will be the reference voltage for the photodetector. This circuit will then be integrated with the a transimpedance amplification circuit. This will take the signal from the photodetector and amplify the output voltage to the required 1.1V for a 1 bit and 0.9V for a 0 bit. This will then be ran into the serializer. This op-amp allows us to take the input signal of the photodetector and translate it to a usable input for the serializer to use. This op-amp utilizes a power input from another source, most likely will be controlled by the microcontroller. With switching speeds of 1.1GHz it is plenty enough in our 1Gbps application.

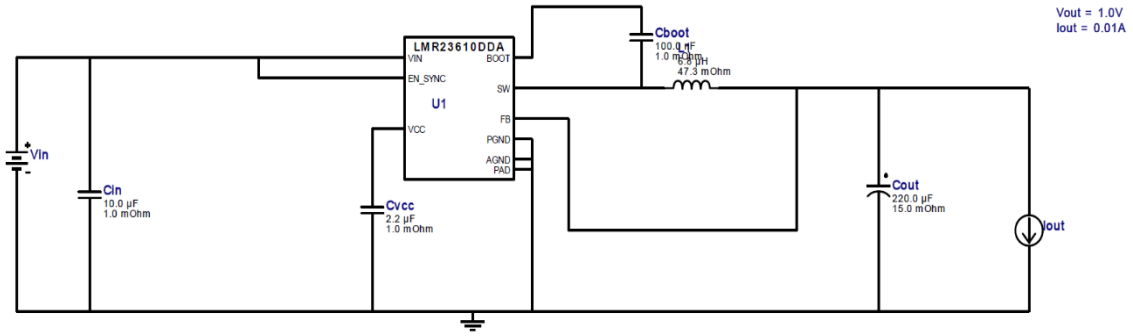



**Figure 23:** Photodetector Power Supply Design

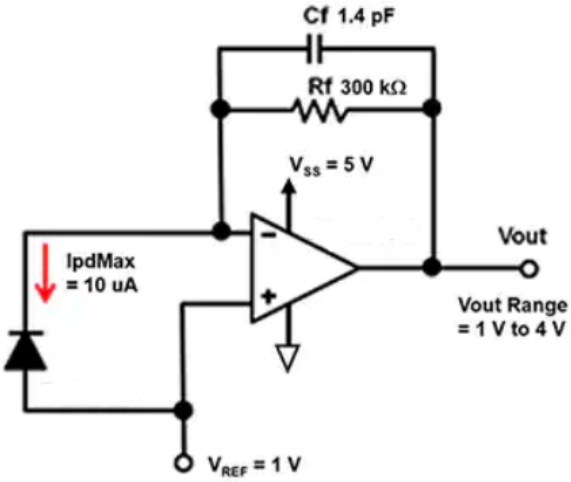



**Figure 24:** Transimpedance Amplification Circuit.

**Figure 25:** 1.1 GHz unity-gain bandwidth, 0.9nV/√Hz, bipolar input amplifier OPA856

# 3.3.5 System Controller

The S.T.E.A.L.T.H system will have two processing units, one on the transmitting side of the system and one on the receiving side. The unit in charge of transmission is attached to, and controls the operation of, the laser. It will be fed information that needs to be transmitted through the laser, which will then be received by the other processing unit. The receiving end is attached to the lens.

To keep the system simple, both the transmitting and receiving ends will be using the same component. It will be easier to design the entire system this way, since only one type of unit is required to be studied and designed around. One big focus of this system is transmission speeds. A transmission of 1 GHz is desirable, so the transmitting unit but be able to process and output data at that speed and the receiving end must be able to handle the incoming transmissions. Power specifications must also be taken into account when selecting the controller, since

the providing power to the laser is a priority, so the controller's power consumption must be low.

# 3.3.5.1 Controller Options

The primary consideration taken when choosing a processing unit was the processor speed. It was important that the unit is able to handle data at 1+ GHz, so that was the constraint used when searching for a suitable product. Three options were found and are detailed in the rest of this section. The first technology researched for this project was the Raspberry Pi development board, due to its popularity and availability. The Texas Instruments (TI) line of microcontrollers was also considered, due to past experiences using TI's embedded systems through courses taken at UCF. Field programmable gate arrays (FPGA) were also researched since FPGA architectures offer more flexibility in terms of processing ability and speeds. Specifically, Xilinx's line of FPGAs was considered, due to previous experiences using the company's products, as well as Intel's family of FPGAs, the Altera Cyclone, based on the brand's popularity in the defense industry.

# 3.3.5.1.1 Raspberry Pi

The Raspberry Pi 4 Model B, the latest edition of this line of products, is a microcontroller that includes the Broadcom BCM2711 processor, which boasts processing speeds of up to 1.5 GHz. It is very popular in the world of electronics and has a lot of resources that the team can use during development as well as troubleshooting, including official documentation and a community forum. The Raspberry Pi runs on a Linux operating system called Raspbian and can be programmed using Python or C++ programming languages. Applications of the Raspberry Pi include media processing and data logging, which could be useful in future iterations of this project. The Raspberry Pi 4 offers multiple interfaces to transfer data at high speeds, including Ethernet, USB Type C, and PCIE ports. Any of these interfaces can be used to control the laser and lenses, by using a board that adapts the connections to useable pins.

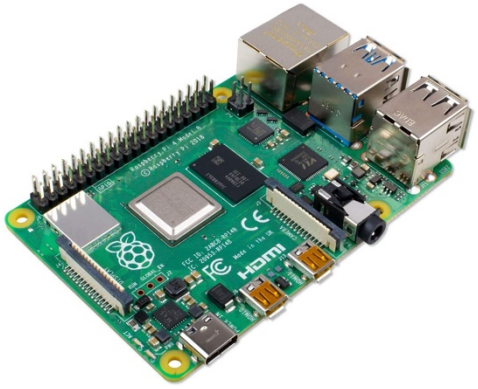


**Figure 26:** Raspberry Pi 4 Model B board and all its peripherals

# 3.3.5.1.2 TI AM5746 Microprocessor

TI offers a series of Arm-based microprocessors. Its processor can run at maximum speeds of 1.5 GHz. This microprocessor can be programmed using TI's Code Composer Studio Integrated Development Environment, which is a tool that has been used by team members in previous UCF courses. One disadvantage of using this microprocessor is that it is sold as a stand-alone chip; the team would need to design a PCB to use this microprocessor. A development board using this microprocessor is available for purchase on the TI website. However, the price tag for the development board is out of the budget range for this project, so a PCB design is a must. The datasheet, however, provides specifications to consider when design such PCB. It offers communication interfaces such as PCIE and Ethernet for fast transmission speeds.

# 3.3.5.1.3 Digilent Nexys-4 DDR Board

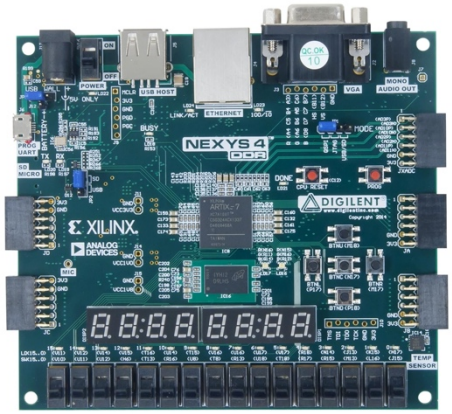



**Figure 27:** Digilent Nexys-4 DDR board

The advantages of using an FPGA over a microprocessor are that an FPGA is very flexible in terms of usability and what tasks it can perform. The Nexys-4 DDR development board from Digilent includes Xilinx's Artix FPGA XC7A100T-1CSG324C. This FPGA was selected for research because one team member owned one from a previous course, and because FPGAs are popular devices in the defense industry and in military applications, therefore designing a system around one would provide invaluable experience in such careers. The Digilent's development board contains many peripherals, and its processor runs at speeds of up to 1 GHz. It has USB and Ethernet interfaces to provide fast transmission speeds. It can be programmed using VHDL inside Xilinx's ISE Design Suite.

# 3.3.5.1.4 Digilent Cmod S7: Spartan-7 FPGA Module

Digilent's Carrier Module, or Cmod is a family of products designed to offer simple and flexible integration of FPGAs for circuit design and prototyping. The Cmod S7 is a 36-pin board built around Xilinx's Spartan-7 FPGA. The board includes 32 Input/Output pins. Xilinx's Spartan-7 FPGA runs on processor speeds exceeding 450 MHz. This FPGA was selected for research based on documentation from Texas Instruments that used this FPGA on a project for the serializer/de-serializer

component described in later sections of this report. This board can be programmed using VHDL or Verilog in Xilinx's ISE Design Suite.

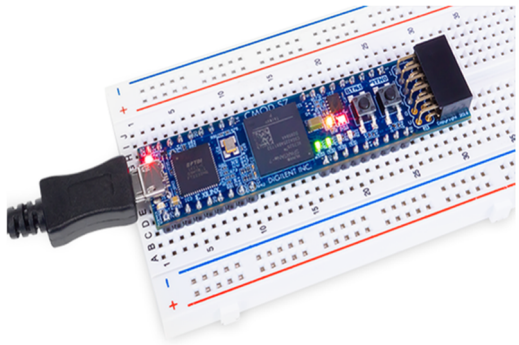


**Figure 28:** Digilent Cmod S7 component attached to a breadboard.

# 3.3.5.1.5 Intel Altera Cyclone IV FPGA Development Board

**Figure 29:** Intel Altera Cyclone IV FPGA

This Intel Altera FPGA was researched because, along with Xilinx's Spartan-7 FPGA mentioned previously, it was mentioned in a project by Texas Instruments describing the functionality of a serializer/de-serializer. This development board includes 70 input/output pins. This FPGA has a maximum processing speed of 500 MHz. The Cyclone IV can be programmed using Altera's Quartus II Web Edition Software Suite using Verilog Hardware Description Language.

# 3.3.6 Controller Comparisons

Three different system controllers were initially chosen for research. These components were the Raspberry Pi 4 Model B, TI AM5746 microprocessor, and Xilinx's Artix FPGA XC7A100T-1CSG324C attached to a Digilent Nexys-4 Board. After the team researched other components included in the computer sub-system, additional research was done on other components to ensure that there will be guaranteed functionality when the system is built as Senior Design II progresses. The research was done on Xilinx's Spartan-7 FPGA Development Board and Intel Altera's Cyclone IV FPGA.

The same controller unit will be in charge of the transmitting and receiving sides of S.T.E.A.L.T.H., one on each end of the system. Specifications that were taken into consideration included processor performance, communication interfaces and the

interfaces' transmission speeds, cost, power consumption, and memory size. The following sections provide a breakdown of such comparisons.

# 3.3.6.1 Comparison Breakdown

The following table, Table 2, shows the comparisons between the components that were researched. Each specification is further discussed in later subsections.

**Table 2:** Controller Processor Frequency Comparison

| | Raspberry Pi 4 Model B | TI AM5746 | Digilent Nexys-4 | Xilinx Spartan-7 | Intel Altera Cyclone IV |
|---|---|---|---|---|---|
| **Frequency (MHz)** | 1500 | 1500 | 1000 | 500 | 500 |
| **GPIO Pin Count** | 40 | 247 | 50 | 36 | 70 |
| **GPIO Voltage Levels** | 3.3 | 3.3 | 3.3 | 3.3 | 3.3 |
| **General-Purpose Clock Pins** | 3 | 1 | 1 | 1 | 1 |
| **Clock Source Frequency (MHz)** | 216-1000 | 192 | 1000 | 450 MHz | 400 MHz |
| **Highest Operating Voltage (V)** | 5 | 3.3 | 5 | 3.3 | 5 |
| **Highest Operating Current (A)** | 3 | 2.7 | 2.5 | 1.2 | 0.5 |
| **Operating Power (W)** | 15 | 8.91 | 12.5 | 3.96 | 2.5 |
| **Unit Price** | $93.99 | $82.95 | $265.00 | $69.00 | $59.99 |
| **Total Price** | $187.98 | $165.90 | $265.00 | $138.00 | $119.98 |

# 3.3.6.1.1 Processing Speeds

Processor performance is proportional to clock speed. Power current is also proportional to clock speed. Processor clocks are necessary because they connect to external peripherals, such as pulse-width modulators (PWM), digital-to-analog and analog-to digital converters (DAC and ADC), sensors, etc., which may not have dedicated clock of their own. The system clock drives them. The sampling of an ADC or the baud rate of UART, for example, as well as other critical functions are directly tied to system clock frequency. Table 2 above indicates the frequency of the processors for each component researched.

Table 2 shows that the Raspberry Pi and the TI AM5746 are equivalent in terms of processor frequency. The Digilent FPGA board with XC7A100T-1CSG324C has lower processing power. This means that while the Raspberry Pi and TI AM5746 can process 1.5 billion instructions per second, the FPGA can only process 1 billion.

One thing to note is that the Raspberry Pi has considerable overhead in that it is essentially a small computer, so it may be running other processes in the background while overseeing the system as well. That is an advantage that the TI AM5746 has over the Raspberry Pi, the team would be able to design and include only what is essential for the system.

Xilinx's Spartan-7 and Altera's Cyclone IV were researched further along the design process, when the team realized that there may be better compatibility among these two components and other components of the computing subsystem. Their processing capabilities are much slower than the other three alternatives. However, the processing frequency of the system was overestimated in its importance, meaning that the frequency will not need to be as high as previously discussed and these two components are sufficient in its processing power. Therefore, the Spartan-7 and Cyclone IV are still in consideration for system controllers.

# 3.3.6.1.2 General-Purpose Inputs & Outputs

The general-purpose input & output (GPIO) header is a grouping of pins that can be connected to peripherals outside of the controller board. The pins within this header can be programmed at the software level to accept an input signal or send an output signal. The resolution of the data being transmitted will be 16 bits. These 16 bits will be sent in parallel to a serializer, so the transmitting controller must have enough pins to transmit this data, and the receiving controller, which will be connected to a de-serializer, must also have a sufficient pin count to accept incoming data. The serializer requires an input signal voltage between -0.3 V and 3.6 V, so the GPIO pins must be able to provide data signals between these

voltage levels. The same voltage levels apply to the output signals coming from the de-serializer, so the GPIO pins of the receiver must accept these voltage levels. Table 3 shows the GPIO pin count and voltage levels comparisons between the three candidates.

The TI AM5746 has the highest count of GPIO pins and offers a wide range of functionality to use them. However, the Raspberry Pi and the XC7A100T-1CSG324C offer more than enough pins as well. All three components meet the requirements of the serializer/de-serializer voltage levels as well. Moreover, the Raspberry Pi and XC7A100T-1CSG324C are development boards, so the GPIO pins already have headers connected to their respective chips, so it allows for easy implementation to the project without having to design a PCB.

Switching speeds of the input and output pins are a consideration that were not previously taken. In electronics, the slew rate of a signal is defined as the change of voltage during a period of time. Figure 23 shows an example of a square input wave and how the slew rate affects the output signal. It is desired that output waveform resembles the square input wave as much as possible, therefore reducing the effects of slew rate. The slew rate determines the rise and fall times of the signals being tested.

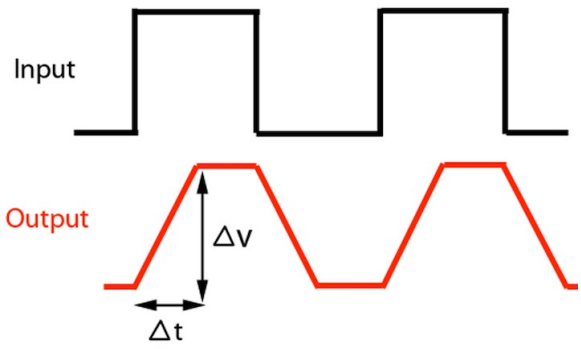



**Figure 30:** A square input wave form and the output, showing the effects of slew rate.

After researching further into the GPIO and the rise and fall times of the signals coming out of these pins, the Raspberry Pi 4, TI AM5746, and XC7A100T-1CSG324C would not be able to meet the demand of having a switching rate greater than 50 MHz without extensive programming. After studying TI's project on the serializer and de-serializer, feeding an external clock on an FPGA such as the Spartan-7 and Cyclone IV will allow such FPGAs to reach the desired frequencies and output valid signals that can be read by the DS92LV96.

# 3.3.6.1.3 General-Purpose Clock

One of the main requirements of this system is achieving transmission speeds of at least 1 GHz. Relying on the controller to output signals at this speed is not viable, since it would require many more parallel pins than what is available or even feasible, taking up a lot of space and power to implement such a design. The team will, therefore, use a serializer to capture the 16 bits of data in parallel and reduce them to a serial stream. The exact serializer and its functionality is discussed in a later section of this report. The serializer, however, requires a clock signal in the range of 25 MHz and 80 MHz, which will be provided by the controller. The following table shows a comparison of general-purpose clocks available to use for each of the three candidates.

The Raspberry Pi includes three GPIO pins that can be configured as general-purpose clocks, with different pins providing a different maximum clock frequency. Only two pins, however, can be chosen from for the purpose of this project, since the third pin is listed a HDMI auxiliary. From documentation, the GPIO clock pins can be configured to a fixed frequency without the need of ongoing software control. Moreover, the clock frequencies can be divided further down to any desired frequency with a simple line of code to achieve the required 25-80 MHz of the serializer and de-serializer.

One consideration not taken is that GPIO pins of the Raspberry Pi may not be able to reach the switching speeds necessary to have valid data at the pins of the serializer. The processing speed of the Cyclone IV and Spartan-7 FPGAs may be sufficient to propagate a switching speed of at least 50 MHz at the pins, so for this reason, they are being considered. These two FPGAs will also be able to provide the necessary frequency to the TCLK pin of the serializer and REFCLK pin of the de-serializer.

# 3.3.6.1.4 Power Consumption

The power consumption of the controller is another major consideration. The system prototype is being designed with the idea that future iterations will mount the design on a drone, so the battery employed on the system will be a typical drone battery. For this system, the battery will also have to prioritize powering the laser, which is the most power-consuming aspect of the entire setup. The following table shows the maximum voltage and current ratings of the units being discussed.

Power consumption was calculated by multiplying the operating voltage and operating current columns for each component. As shown in Table 3, the Raspberry Pi is the most power-consuming component of the three, consuming 68% more power than the TI AM5746 and 20% more power than the XC7A100T-1CSG324C.

After new research was performed on the two FPGAs, the Cyclone IV and the Spartan-7 FPGA development boards are the two least power-consuming components, with maximum ratings of 2.5 and 3.96 watts.

# 3.3.6.1.5 Cost

The cost comparison between the three devices is shown in Table 2.

The total price takes into account that two components will be needed for the entire system. The team would have to procure only one additional Digilent board containing the XC7A100T-1CSG324C since a team member already possess one board. As it can be seen in Table 2, the Raspberry Pi is the cheapest component to obtain. The TI AM5746's price only includes the chip itself, the cost does not include the price for PCB manufacturing and all that that entails, so the expenses of using this processor are higher than what is listed in the table.

The Spartan-7 and Cyclone IV FPGAs provide sufficient power at a reasonable price and no additional costs are required, such as the development of a PCB board.

# 3.3.6.2 Controller Choice

Following the comparisons of all five components in previous, the Raspberry Pi was thought to be the microcontroller that would provide the best fit for the S.T.E.A.L.T.H. system. The cost of this component was the lowest when there were only three options being considered, and it was believed to be the easiest to implement. In performance, it matches the TI AM5746, with both outperforming the XC7A100T-1CSG324C. At 1.5 GHz processor speeds, it was believed to be more than capable of meeting performance requirements, with sufficient GPIO pins and clocking capabilities. It meets GPIO requirements and will be able to drive the clock inputs of the serializer and de-serializer, with two available clock pins that the team can use. The Raspberry Pi will be easier to implement into the design since it is a development board that already has all the necessary peripherals attached to it. This is the biggest advantage that the Raspberry Pi has over the TI AM5746, its ease of use and implementation.

However, upon further research into the serializer and de-serializer components, the switching speed of the GPIO pins of whichever controller is ultimately selected must be able to match the TCLK and REFCLK frequencies. For example, if the clock pins are 50 MHz, the data pins must be able to have switching characteristics that match this frequency. After follow up research was done on the Raspberry Pi, no source of information indicated that its GPIO pins could satisfy this requirement. All signs pointed to the GPIO pins to have switching rates much lower than 50 MHz, meaning that the Raspberry Pi 4 would not be able to deliver reliable data to the serializer or read data from the

de-serializer. In essence, the serializer would read data at a much higher frequency than the data was being updated. For this reason, the Raspberry Pi will not be considered further.

The team reassessed how to achieve a transmission speed of at least 1 gigabit per second. The Serializer and De-serializer, discussed in later sections, would be able to create a serial stream from a parallel input bank. The main issue faced was that the data from the GPIO pins would not be updated at the same frequency as the input clocks. A project was searched for and the team was able to find a paper published by Texas Instruments that employed the serializer and de-serializer chosen. The serializer and de-serializers in this project were used to reduce simultaneous switching output noise in FPGAs. The paper further showed how an FPGA with no dedicated serialization or deserialization circuitry for high-speed communications could benefit from working alongside an external serializer and de-serializer. The FPGAs considered in the project were Xilinx's Spartan family and Intel Altera's Cyclone families of FPGAs. The paper further claimed that the serializer and de-serializer can be used with any FPGA density and architecture.

The Digilent Cmod S7 was considered because it was relatively inexpensive and able to be attached to a breadboard easily. The Intel Altera Cyclone IV development board was similarly chosen because of its high amount of GPIO pins as well as its price. Between these two options, the Altera Cyclone IV development board has the most amount of pins and consumes the least amount of power. One interesting aspect of the Cyclone IV involves its switching characteristics at the GPIO. The datasheet for this FPGA says "I/Os using general-purpose I/O standards such as 3.3-, 3.0-, 2.5-, 1.8-, or 1.5-LVTTL/LVCMOS are capable of a typical 200 MHz interfacing frequency with a 10 pF load." This is exactly the type of documentation that the team was searching for. No such claim is made on the Spartan-7 FPGA from Xilinx.

For the reasons stated in previous paragraphs, the team will continue the design process with Intel Altera's Cyclone IV FPGA development board.

# 3.3.7 Serializer & De-Serializer

As mentioned before, the system will require to transmit information at very high speeds. One GHz transmission speeds is the goal for a system like this. However, such transmissions would only be achievable if the team uses many GPIO pins in parallel, which is unrealistic due to power and spacing constraints. The way that such transmissions will be achieved is by incorporating a serializer and de-serializer into the design.

# 3.3.7.1 TI DS92LV16 Serializer and De-Serializer

The DS92LV16 is a serializer and de-serializer that translates a 16-bit parallel bus into a serial stream and vice-versa. The DS92LV16 contains independent one transmitter block and one receiver block that are independent from each other, meaning that it can be used as a serializer only on the transmitting end and a de-serializer on the receiving end. Figure 4 shows the block diagram of the DS92LV16. It takes 16 bits of data at the serializer block (DIN[0:15]) and outputs it into a serial differential signal (DO+/-), reducing 16 pins down to 2 pins. It takes as input a system clock (TCLK) which is provided by the source of data, in this case the Raspberry Pi. TCLK requires an input frequency between 25 and 80 MHz to perform properly.

The DS92LV16 combines a serializer and a de-serializer into a single chip that sends 16 bits of parallel TTL data over a serial Bus LVDS link up to 1.28 Gbps. Serialization of the input data is accomplished using an onboard PLL at the Serializer which embeds two clock bits with the data. The de-serializer uses a separate reference clock (REFCLK) and an onboard PLL to extract the clock information from the incoming data stream and deserialize the data. According to the functional description provided in the datasheet of the DS92LV16, the serializer and de-serializer blocks each has three operating states, Initialization, Data Transfer, and Resynchronization.

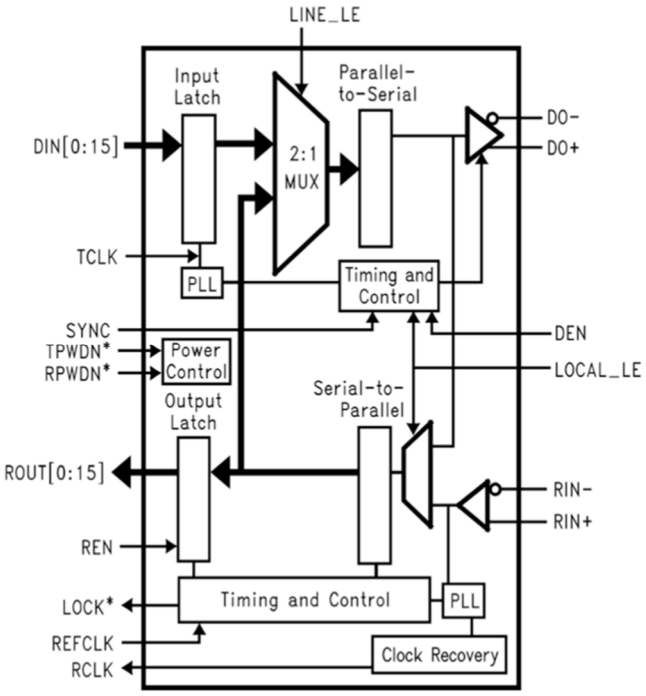



**Figure 31**: Block Diagram of DS92LV16

## 3.3.8 Analog-to-Digital Converter

The analog-to-digital converter (ADC) is in charge of capturing the waveform transmitted by the laser into digital logic to be interpreted by the microcontroller. Since high data rate is a requirement for this system, the ADC must be able to process the incoming transmission at rates of at least 1 giga-samples per second. The following ADCs were researched by the team as potential solutions to be used by the S.T.E.A.L.T.H. system.

Upon further understanding of the system the team decided that an ADC was not required for this system, since the photodetector will be able to output the required voltage levels to the de-serializer. Since the ADCs that were considered had a price range of $600 and above per unit, this is the desired outcome.

### 3.3.8.1 TI ADC16V130

The ADC16V130 is a high-performance CMOS analog-to-digital converter capable of converting analog input signals into digital words at rates up to 1000 mega samples per second (Msps). This converter uses a differential architecture with digital error correction and an on-chip sample-and-hold circuit to minimize power consumption and external component count while providing dynamic performance. A unique sample-and-hold stage yields a full-power bandwidth of 1.4 GHz. The digital data is provided via full data rate LVDS outputs.

### 3.3.8.2 TI ADS54J60

The ADS54J60 is a low-power, wide-bandwidth, 16-bit, 1.0-GSPS, dual-channel, analog-to-digital converter (ADC). Designed for high signal-to-noise ratio (SNR), the device supports the JESD204B serial interface with data rates up to 10 Gbps, supporting two or four lanes per ADC. The JESD204B interface reduces the number of interface lines, allowing high system integration density. An internal phase-locked loop (PLL) multiplies the ADC sampling clock to derive the bit clock that is used to serialize the 16-bit data from each channel.

## 3.3.9 Receiving Lens

At the start of the receiving module, a problem must be solved as to how you collect the light from which your optical communication signal is deduced. This involves selecting a lens that gives you ideal transmittance at 1550 nm, focusing capability over a short range to assist in pointing, and has a large enough aperture to collect a sufficient amount of irradiance from the beam’s diverged cross section at receiving range. Lastly, availability of parts must be considered as well. Despite desire to put as much design into the system optics as possible, the scope of this

project is constrained to what are available as “off the shelf” lenses in order to meet necessary project budget and deadline goals.

To begin this selection process, we first had to ponder what size of lens are we okay with having. On one hand, maximizing the size of the lens allows us to collect as much optical power from the beam’s intensity as possible, but on the other as size and collection capability increases, minimum form factor size and shape decreases. In addition to one side needing to be larger as a function of actual lens size, larger lenses generally have smaller minimum focal distances, meaning that the depth of the system may have to increase as well. With these factors in mind, we decided on 50 mm (~2 inches) as an ideal starting point for lens diameter as we believe with that diameter, we can collect enough light to witness a discernable signal at 1 km range while suffering the minimum penalty to form factor. Based on the minimum case size needed to house other components, at this time we are not even sure if a 2-inch lens causes any disruptions to desired form factor at all which was a big pro for choosing this size. Another consideration in lens size is cost. The smallest lens we can use to achieve our necessary light collection objectives is going to likely be the least expensive viable option as well when controlling for other parameters.

Next we also had to consider the material selection of the lens. During our selection process, we started with what was readily available and narrowed it down to two primary choices: N-BK7 and N-SF11. Some of their properties are listed below in Table 3.

**Table 3:** Comparison of lens glass material properties with lens choice highlighted

| Glass | Refractive Index ($n_d$) | Abbe Number ($v_d$) | Density ($g/cm^3$) | Coefficient of Thermal Expansion | Max Operating Temp (°C) |
|---|---|---|---|---|---|
| N-BK7 | 1.517 | 64.2 | 2.46 | 7.1 | 557 |
| N-SF11 | 1.785 | 25.8 | 5.41 | 6.2 | 503 |

While N-BK7’s higher Abbe Number and generally wider availability were both positive qualities, we ultimately plan to use an N-SF11 lens as our receiving aperture for 2 primary reasons. The first being that its higher refractive index allows it to focus light down to a focal spot more strongly/quickly, resulting in shorter focal distances as a function of lens thickness. The second motivation for this choice was a more ideal antireflective coating option from Edmund Optics referred to as 1550 nm v-coat, which is less than 0.25% reflective at our wavelength. Because we wish to conserve as much of the collected power as possible due to the small irradiance caused by our large beam area, having the highest transmittance at every component possible throughout the design process was a strong motivating factor.

Once our lens size and material was selected, it was just a matter of sourcing the shortest focal length that would be available the soonest, and as previously mentioned that ended up being an offering by Edmund Optics, with a focal length of only 50 mm, yielding an F/# of 1.0, we think this is the right lens for our collecting aperture.

# 3.3.10 Collimating Lens

As of the time of this draft, this is the last optical component yet to be selected, however we figured it would be of value to still discuss the ongoing selection process for this component. The collimating lens is the lens that forms the exit aperture of the transmitting end of the system. Because we already have to have one side of our device be at least two inches tall to accommodate for our collecting lens, the size of the transmitting lens is less impactful but similarly to in the case of the collecting aperture, we still want to optimize size versus performance needs. Also important to us is the transmittance of a collimating lens being similarly close to 1 for 1550 nm light. A factor that did not need to be considered in the case of the collecting lens that must be weighed here is the divergence of the beam after the lens. In a world where pointing a beam the width of our 2 inch collecting lens and perfectly hitting our target at a 1 km range was an easy task, we would want a divergence as close to 0 radians as possible. However, because we want to design a real-world system capable of solving real world problems, we have to set realistic constraints. This limiting requirement to have some minimum beam divergence informs what we want angular direction we want light to exit our transmitting aperture at. Figure 25 depicts the trigonometry at play in order to find the required divergence to have a 2 meter diameter cross section at our desired maximum communication range.

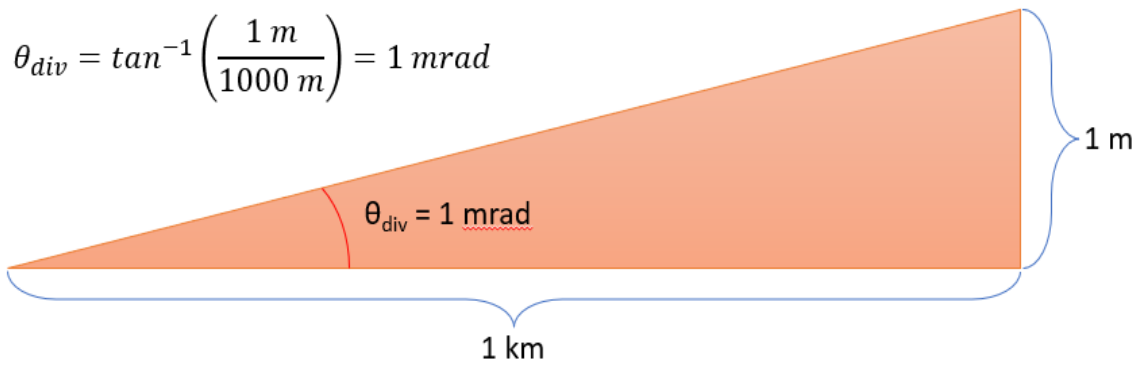



**Figure 32:** Desired beam divergence scenario

While we are still working on the design process of this lens, a solution that has shown great promise in our technology investigation is an adjustable fiber collimator. This component leverages our already fiber coupled laser and allows us to adjust the beam divergence dynamically. We think this may end up being the most ideal solution for a project like ours because although we are designing the

system to be able to communicate at a 1 km range, we may only be able to test at short ranges. At very short ranges, there is some risk associated with driving our laser to a high power because the upper limit of optical power that can safely be detected by our photodiode is half of what our laser is capable of outputting. Additionally, this adjustable fiber collimator leverages the fact that we are using a fiber coupled laser, and some of them are specifically created with fiber-to-air applications like ours in mind. This alleviates the need for creating our own adjustable lens assembly within an already tight fit form factor case while still providing us the flexibility of variable focal distances and beam divergences.

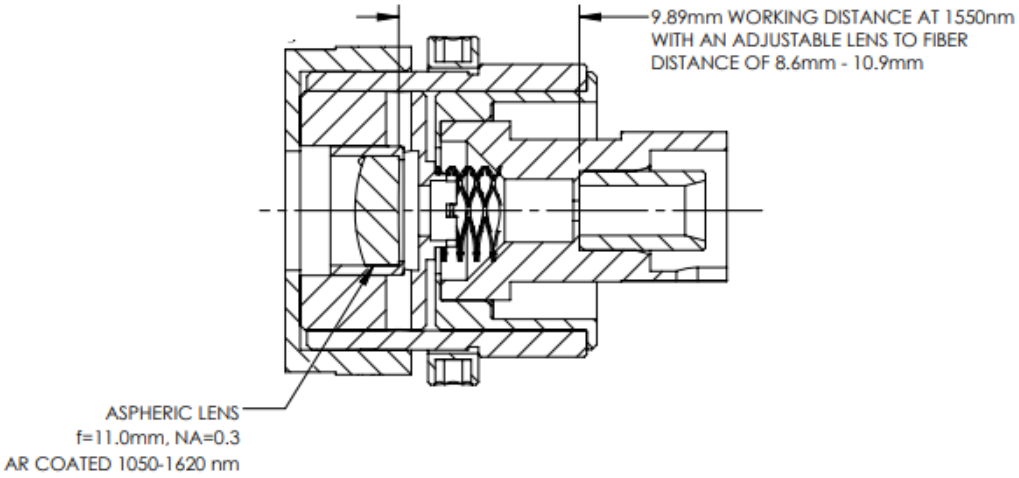



**Figure 33:** Schematic of a general adjustable fiber collimator layout

Looking at Figure 26 above it can be seen that the working principle of these adjustable collimators is that rotation of the outer face where the lens is located results in a non-rotational translation along the optical axis, which in turn adjusts the distance between the fiber end face and the lens's front principle plane, and as a result the distance at which light comes to a focus is changed. The closer that this location nears the front focal plane of the fiber, the closer the angular direction of light exiting the collimator approaches 0 and therefore light goes towards infinity. However, we actually desire a slightly more divergent path than a perfect paraxial collimation. Instead, as mentioned prior we want a 1 mrad beam divergence to assist in the expected to be difficult task of system pointing at range. Furthermore, the adjustable collimator already contains an aspheric lens, the type of lens ideal for producing an axially uniform beam distribution from a semiconductor laser, which is the type of laser source coupled into our fiber laser. These sources do not typically have a perfectly Gaussian intensity pattern without some sort of optical beam shaping and the aspheric lens shape helps towards that goal. The inclusion of this in the adjustable collimator saves us some work in additional procurement and high precision mounting (relative to the fiber laser end facet) that would be required in the case of trying to make an off the shelf aspheric lens work in free space as compared to at the fiber termination.

Lastly, from a Senior Design demonstration perspective, it is important that not only our product is flexible for testing methods we have available to us, but perhaps most importantly is clearly demonstratable. While we intend to design a system capable of communicating at a 1 km range, we should be able to demonstrate the viability of the product at 3-5 meters. Thinking about the geometry at this range, given the 1 mrad divergence the system is designed for at range, two problems may arise. The first problem being that pointing and aligning the system with such a small beam cross section at a 5-meter range could be difficult, and lengthy alignment and troubleshooting could obfuscate thorough exemplification of what the system is capable of. Second, given a 1 mrad fixed divergence at those ranges the beam cross section is smaller than the collecting aperture, meaning all of the laser power can be collected by the receiving end system. This actually creates an unintended problem, as there is a limit on optical power that the photodiode can be reasonably exposed to at a focal spot without receiving damage. Furthermore, the data side of the project requires that the amplitude of the signal produced by the photodiode be within a certain threshold to make correct bit decisions, however at this close of range even the intended laser power level for a 0 bit would saturate the photodiode, producing a constant erroneous bit stream of 1s. This second problem can and will in part be mitigated by the introduction of a neutral density filter for demonstration purposes, as will be detailed in a later section of this report.

# 3.3.11 Optical Bandpass Filter

The optical band pass filter component ended up being a more critical component choice than we initially thought at the onset of the project. Due to Planck's Radiation Law, which determines the amount of ambient solar flux we can expect to be incident on the photodiode. The total amount of flux is a function of the band size, so the more we can reduce that band via an optical bandpass filter, the less ambient solar power our optical laser signal needs to compete with in terms of signal/bit interpretation. In our research it seemed that as spectrally filtered bandwidth got smaller, so did the minimum transmission within the desired band. This created a tension where in order to optimize the maximum amount of power over noise at the photodiode, we had to make the best compromise between filter transmission at 1550 nm and the smallest filtered bandwidth. Our choice was a 1550 nm 12.5 mm diameter Hard Coated OD 4.0 10 nm bandpass filter, with a FWHM band accuracy of ± 2.0, meaning that the overall band size is as large as 12. For this reason, we estimated in all calculations that the size of the band passed through the receiver system would be from 1544 nm to 1556 nm (1550 nm ± 6 nm). This optical filter has a minimum transmission of 85%. While it is unfortunate to lose as much as 15% of our received optical power, the silver lining is that the unwanted solar flux that makes it through the filter within this band also experiences this loss.

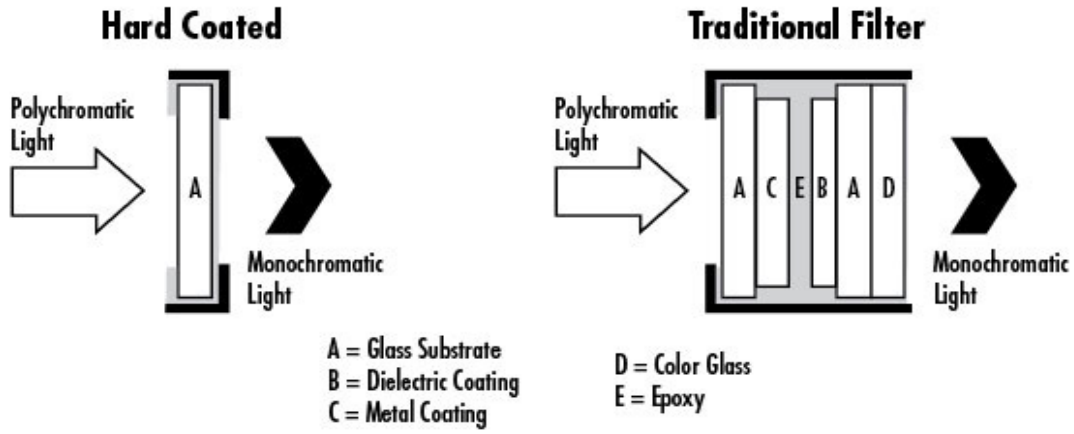



**Figure 34:** Comparison of Hard Coated optical filters to Traditional Filter variations

In particular, a high performance hard coated optical filter was selected for its increased transmission (given that we already lose so much laser light due to divergence) and robustness in comparison to more traditional optical filter types due to the desire for the final S.T.E.A.L.T.H. product form factor to be semi-ruggedized such that it will hold up to outdoor operation.

# 3.3.12 Optical Neutral Density Filter

When considering the viability of demonstrating this project to scale at smaller link distances than the design intended 1 km, it we must consider the difference in optical power of a small portion of a large beam cross section at range to the entire beam being collected at short enough ranges. In order to demonstrate our system which will be designed to receive on the order of microwatts of optical power at range close up using a laser that has a peak optical power output of 10s of milliwatts, rather than significantly change transmitter or receiver functionality, we can physically intervene and adjust the relative power seen by the sensor via the introduction of a neutral density filter.

Neutral density filters reduce the amount of light that is allowed to enter an aperture by way of reduced transmission. Neutral density filters will have some intentionally low transmission within their design band. This transmissivity is a function of a metric known as optical density (OD). The optical density is a factor of the attenuation caused by the filter and is given by the following:

$$OD = \log_{10}\left(\frac{1}{T}\right)$$

**Equation 1:** Optical density as a function of transmission

In order to use this equation, we can think of the scale factor which we want to apply to our beam in order to simulate the amount of power collected from a portion of the diverged cross section at range by thinking about how much that power is in

relation to the maximum output of the laser. This ratio is proportional to the amount of transmission we would desire for our filter, and thus will allow us to find OD as a function of transmission as such:

$$P_{laser,max} = 20\ mW = 0.02\ W$$

$$P_{received,1km} = 12\ \mu W = 0.000012\ W$$

$$T_{OD} = \frac{0.000012\ W}{0.02\ W} = 0.0006$$

$$OD = \log_{10}\left(\frac{1}{0.0006}\right) = 3.22185$$

**Equation 2:** Consideration of desirable optical density for neutral density filter component selection

We can see the for proving this product at short ranges with a system designed for long ranges, that an OD value near 3.22 would be ideal for our use case. It should be noted that due to availability and lead time constraints, it is likely that we will have to use an available off the shelf filter whose OD is not exactly 3.22. While we shouldn't need that exact value for it to work, in the case that we want as precise of a comparison between our short-range demonstration and long range design case we can approach this accuracy with an ND filter with lesser OD. Through use of the adjustable fiber collimating aperture discussed previously, an OD of less than 3.22 can be used and the 1 km analogous power into the aperture of approximately 12 μW can be achieved at any range by adjustment to the beam divergence and thus irradiance at range

Many neutral density filters that have been looked at with our desired spectral and OD parameters, for instance the Thorlabs NENIR30A-C, are available already within a thread mounted holder. For this reason it may be wise that we leverage this by lending design considerations to our 3d printed outer casing design to have matching threads or ability to add a threaded adapter to the physical aperture where the receiver collecting lens will collect light from for easy installation and removal of an ND filter or even various ND filters of the same size and threads for various test cases in order to maximize our flexibility in Senior Design 2.

# 3.3.13 Photodiode

There are a wide range of different photodiodes to choose from. The key features our project depends on are low capacitance, responsivity, and dark current. Capacitance determines response time or "speed" of the photodiode. The lower the response time, the faster the photodiode will respond to an optical input. An incoming photon is absorbed by the semiconductor material, which in turn

generates an electron-hole pair. This pair then begins to move in the material from the effect of the electric field, when then creates a current. A response time known as the RC time constant:

$$\tau = RC$$

**Equation 3:** RC time constant that contributes to photodiode response time

The combination of R and C combines the photoresponse over time, which in turn lengthens the impulse of the response time of the photodiode. Responsivity is the ratio of photocurrent generated from incident light to the power of that incident light. This is usually expressed in units of amps per watt (A/W). Responsivity is a function of wavelength; meaning is it dependent on the wavelength. This can also be stated as the quantum efficiency, which is the ratio of number of photogenerated carriers to incident photons and is a unitless number. For our project, we want the peak responsivity of the photodiode we choose to be at 1550 nm. Dark current is the current through the photodiode when there is no direct optical input. This is usually caused by background radiation that can come from sources like the sun or another external light source as well as the saturation current of the semiconductor junction. Dark current needs to be accommodated for through calibration in order to get an accurate optical power measurement. A good place to start though is trying to acquire a photodiode with a low dark current, but response time and responsivity should be placed ahead in importance.

# 3.3.14 Photodiode Options

There are very wide range of companies that make various photodiodes. We decided to go with Thorlabs' selection because we have used them in our class labs for two years and they have always been reliable.

# 3.3.14.1 Thorlabs FGA01 Photodiode

This model is ideal for measuring both pulsed and continuous wave (CW) fiber light sources. This is a standard three pin device. It has a responsivity of 1.003 A/W at 1550 nm. The active area diameter is 0.12 mm. The rise/fall time is 0.3 ns / 0.3 ns. The dark current is 0.05 nA. The capacitance is 2 pF. Thorlabs sells this product for $62.76. The major drawback of this model is that it has a ball shaped lens, which is better suited for signal coupling between fibers, for that reason this photodiode will not be considered.

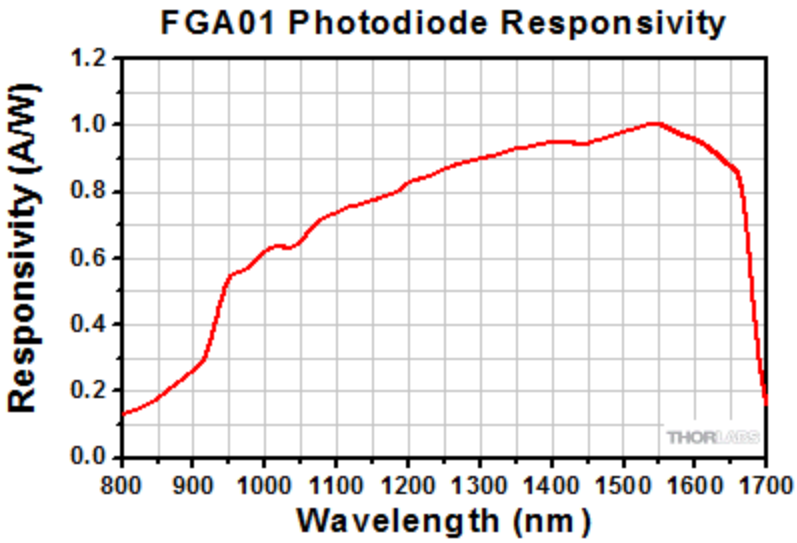



**Figure 35:** Photodiode Responsivity of FGA01

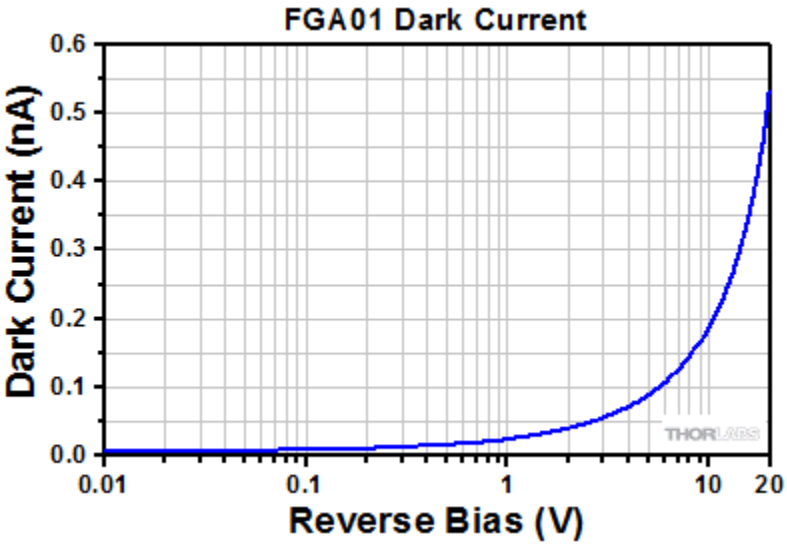



**Figure 36:** Dark Current of FGA01

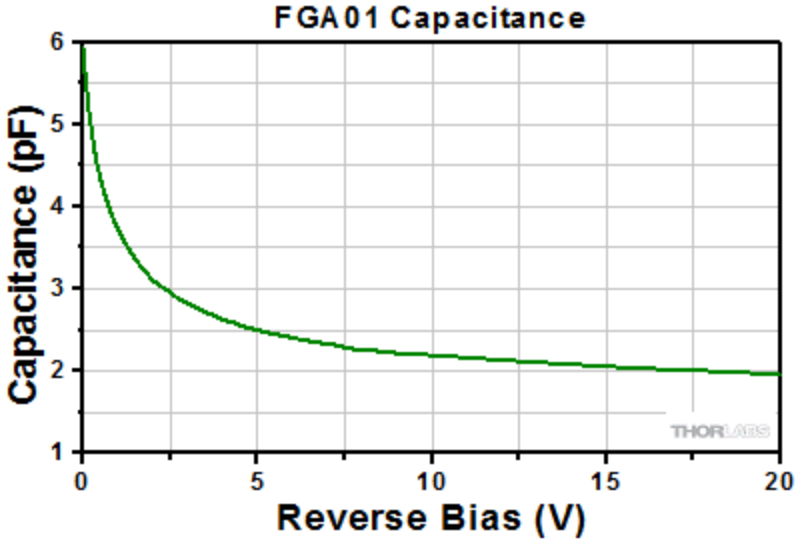



**Figure 37:** Capacitance of FGA01

# 3.3.14.2 Thorlabs FGA01FC Photodiode

This model can measure both pulsed and CW fiber light sources. This is a standard three pin device. It has responsivity of 1.003 A/W with a peak wavelength of 1550 nm. The active area diameter is 0.12 mm. The rise/fall time is 0.3 ns / 0.3 ns. The dark current is 0.05 nA. The capacitance is 2 pF. Thorlabs sells this product for $159.07. This diode is equipped with a bulkhead, which is for coupling directly to a fiber. Our system will not be coupled directly to a fiber, and therefore this product will not be considered.

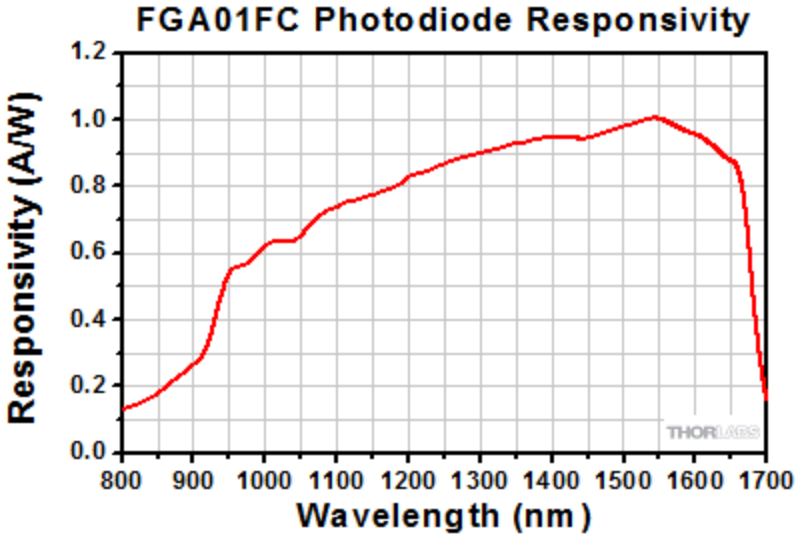



**Figure 38:** Photodiode Responsivity of FGA01FC

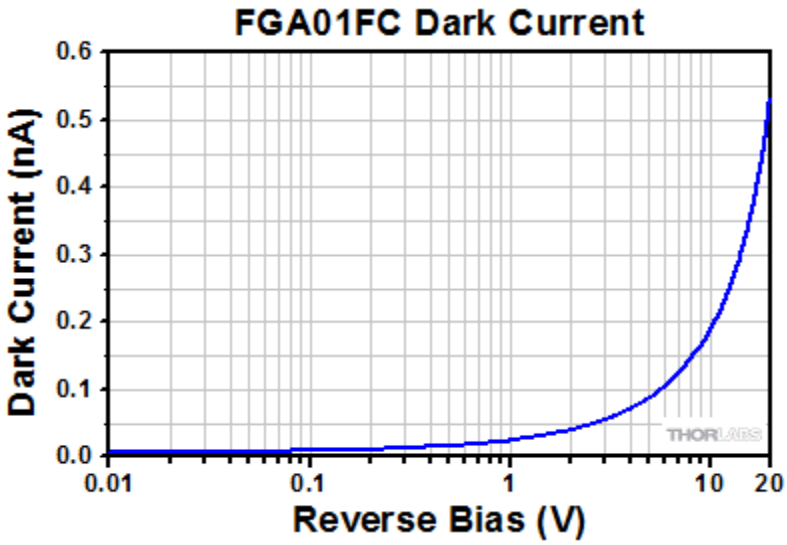



**Figure 39:** Dark Current of FGA01FC

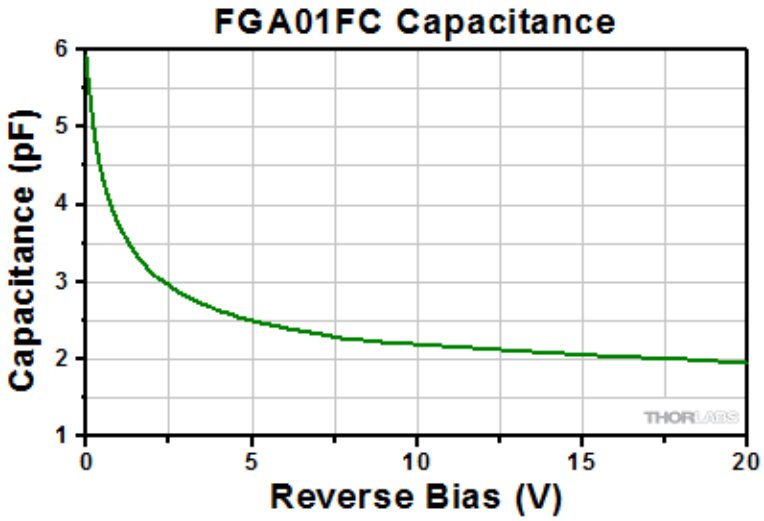



**Figure 40:** Capacitance of FGA01FC

# 3.3.14.3 Thorlabs FGA015 Photodiode

This model can measure both pulsed and CW fiber light sources. This is a standard three pin device. The photodiode features a flat window with a broadband AR coating centered at 1550 nm., which is ideal for our project. It has responsivity of 0.95 A/W with a peak wavelength of 1550 nm. The active area diameter is 150 µm. The rise/fall time is 300 ps / 300 ps. The dark current is 0.5 nA. The capacitance is 1.5 pF. Thorlabs sells this product for $58.35, which is the cheapest out of all the options. They advertise this model as “high speed and low capacitance” which exactly what we are looking for in the photodiode selection. This model also has

the lowest capacitance out of all the photodiode options. As a result of the lowest cost and lowest capacitance, our group selected this photodiode for our project.

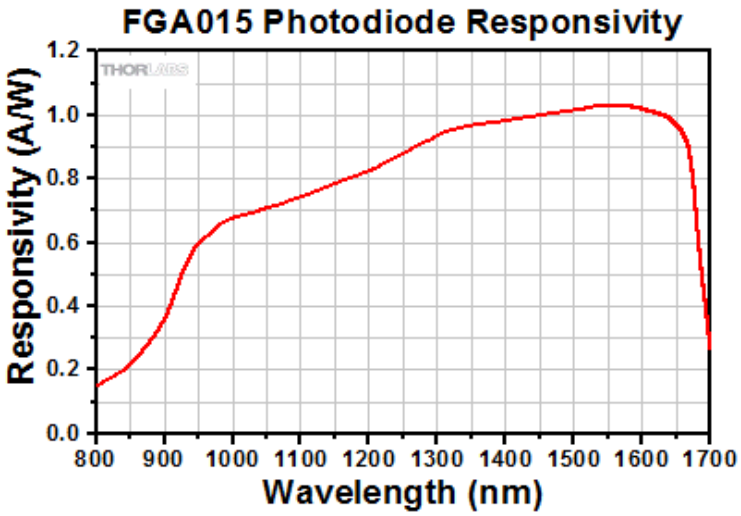



**Figure 41:** Photodiode Responsivity of FGA015

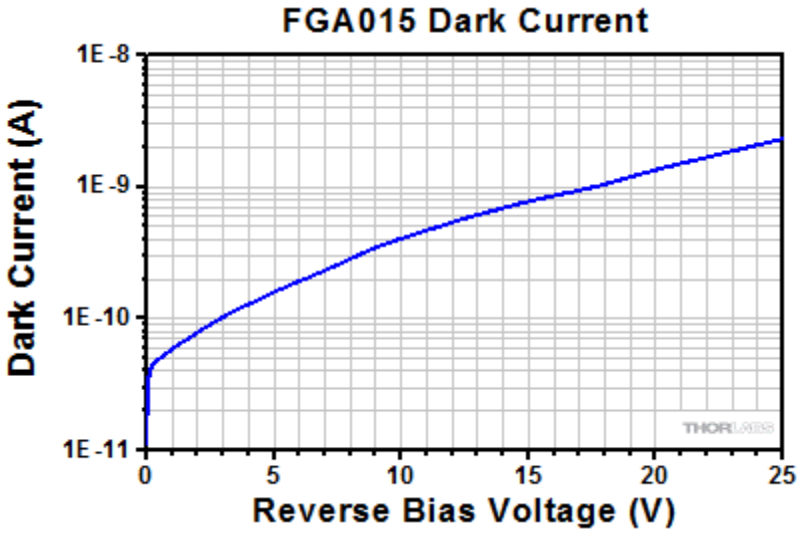



**Figure 42:** Dark Current of FGA015

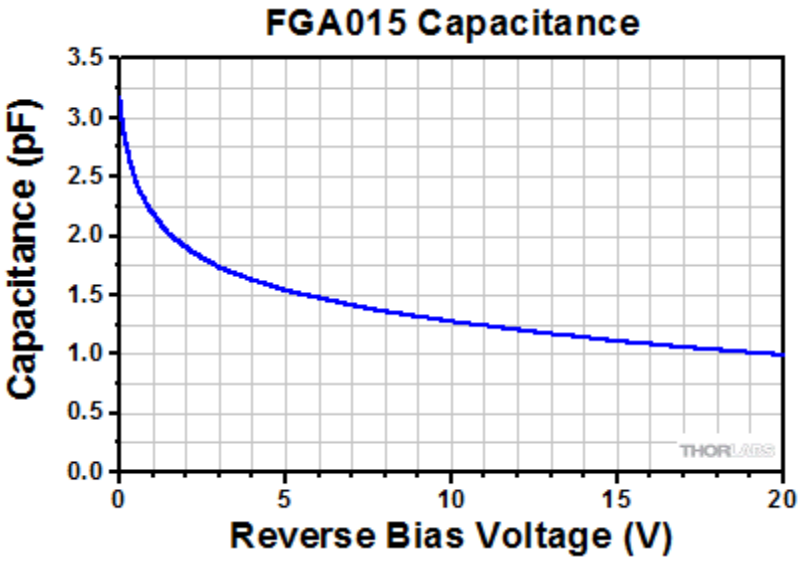



**Figure 43:** Capacitance of FGA015

# 3.3.14.4 Thorlabs FDGA05 Photodiode

This model can measure both pulsed and CW fiber light sources. This is a standard three pin device. It has responsivity of 0.95 A/W with a peak wavelength of 1550 nm. The active area diameter is 0.12 mm. The rise/fall time is 2.5 ns / 2.5 ns. The dark current is 6 nA. The capacitance is 10 pF. Thorlabs sells this product for $148.25. This photodiode has relatively high dark current and capacitance, so it will not be considered.

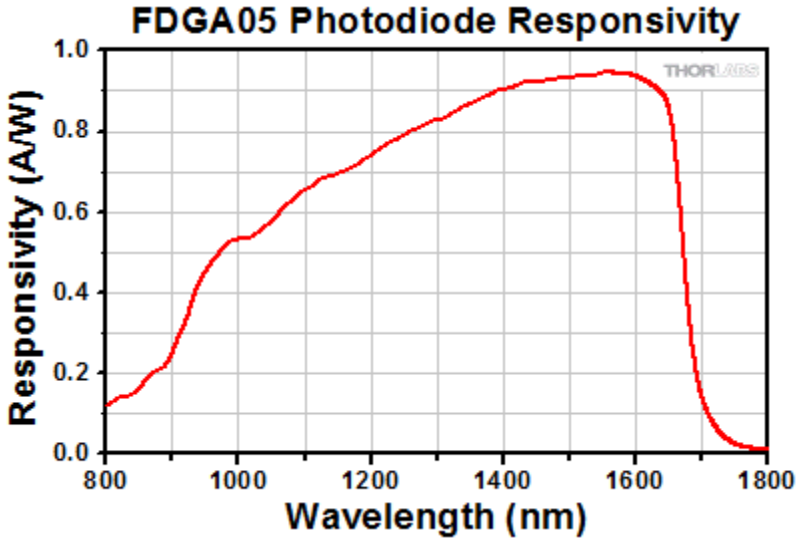



**Figure 44:** Photodiode Responsivity of FDGA05

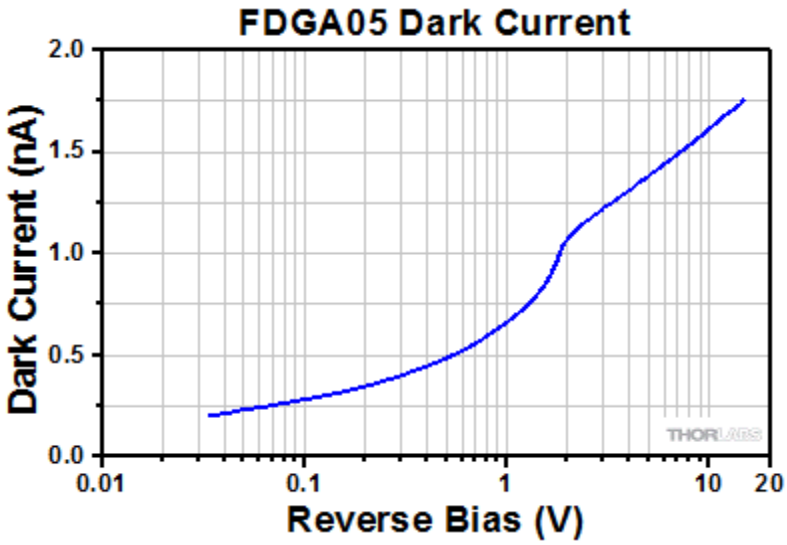



**Figure 45:** Dark Current of FDGA05

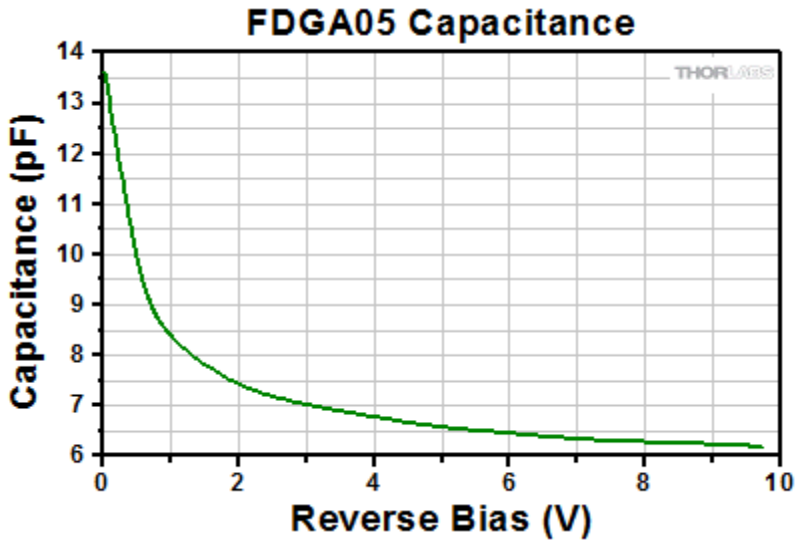



**Figure 46:** Capacitance of FDGA05

# 3.3.14.5 Thorlabs FGA21 Photodiode

This model can measure both pulsed and CW fiber light sources. This is a standard three pin device. It has responsivity of 1.04 A/W with a peak wavelength of 1590 nm. The active area diameter is 3.1 $mm^2$. The rise/fall time is 25 ns / 25 ns. The dark current is 50 nA. The capacitance is 100 pF. Thorlabs sells this product for $241.31. The biggest advantage of this photodiode is the largest active area out of all of the other photodiodes. However, every other feature of this product is not advantageous for our project, specifically that the peak wavelength of responsivity is at 1590 nm and not 1550 nm. This automatically eliminates this product as a real option for our project.

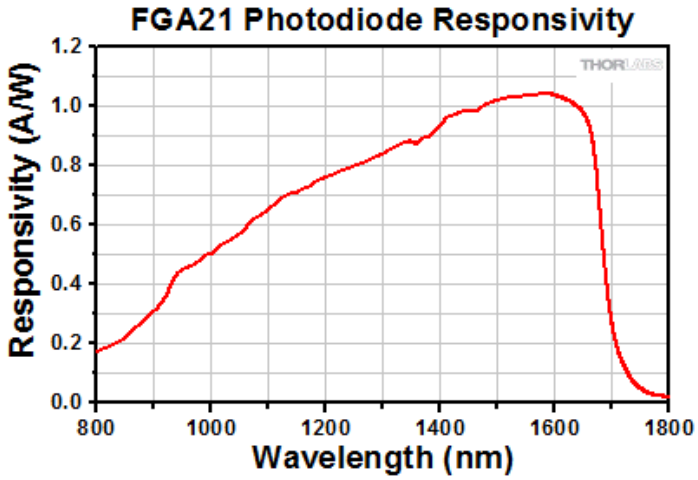



**Figure 47:** Photodiode Responsivity of FGA21

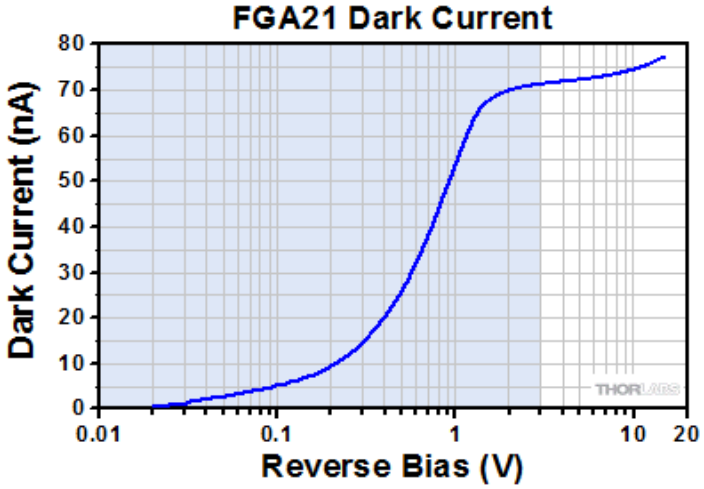



**Figure 48:** Dark Current of FGA21

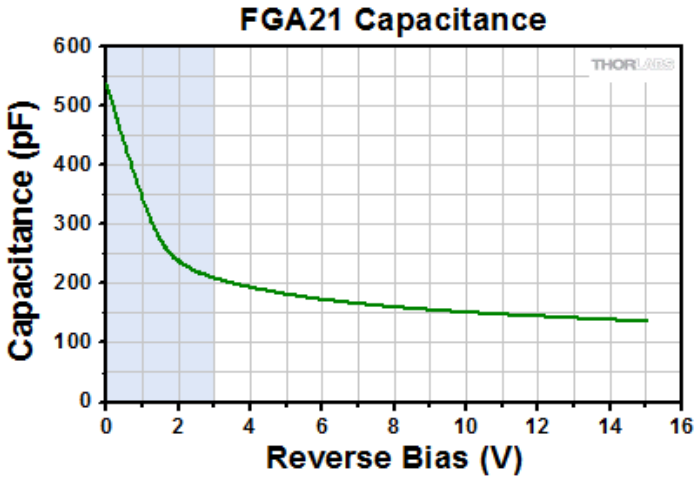



**Figure 49:** Capacitance of FGA21

# 3.3.15 Lasers

The S.T.E.A.L.T.H system will be using lasers to transmit data back and forth. These are key components of the system. The system requires two lasers because both ends of the system need to be able to send and receive data.

This project is using Distributed Feedback (DFB) lasers because they are designed to emit light within the telecom band (1310-1550 nm). A major part of DFB laser selection was choosing between externally modulated and directly modulated lasers. The fundamental difference between these two designs is the directly modulated laser is modulated by using an input drive current, whereas external modulation uses an integrated optical modulator.

There are different kinds of external modulation such as electro-absorption, electro-optic, magneto-optic, and acousto-optic. Electro-absorption modulation uses an electro-absorption modulator (EAM) in a single chip. A simple circuit controls the EAM to generate on/off signals for the laser beam. For electro-optic modulation, light from the laser passes through a material whose refractive index can be altered through an applied electric field. Changing the refractive index of a material allows two light waves to be out of phase by half a wavelength. This in turn makes the light waves cancel out and the laser beam will not propagate to the receiver. For magneto-optic modulation, the laser beam passes through a medium that is magnetically sensitive. This medium's refractive index is manually controlled by changing the magnetic field around the medium to change its polarization by angle (θ). Changing the polarization can then change the phase of the medium. If the phase of the medium is different than the phase of the beam, the beam will not propagate through the medium. Then switching the polarization back-and-forth can act as an on/off switch. For acousto-optic modulation, the laser beam again enters a medium, but this medium also has acoustic waves passing through it. These waves create areas of compression and refraction within the crystal high structure. As a result, the medium has periodic changes in refractive index. This in turn allows input light to the acousto-optic device to be diffracted into a number of orders at the output. The device also has an absorber for the waves to prevent secondary diffractions due to reflections. External modulation allows for faster processing and can be used with higher power lasers. However, these systems are more expensive and are usually more complex than a directly modulated system.

Directly modulating a laser is done by controlling the driving current going to the laser diode chip. This means that sending a higher current through the laser will causes it to emit light which represents a "1" in binary, whereas running a lower current through the laser does not emit light, this in turn represents a "0" in binary. This form of modulation is advantageous because it only requires a simple circuit and is not a complex as external modulation. The biggest advantage of only needing a simple circuit is huge savings on weight and size, which is one of the goals got this project.

There are so many different laser wavelengths to choose from, why is 1550 nm the best? One of the biggest advantages is there is lower attenuation at longer wavelengths, which means less fiber loss. The average attenuation for this wavelength is around 0.2 dB/km. 1550 nm is within the C-band (1525-1565 nm), and this range is commonly known as the “zero loss window”.

# 3.3.16 Laser Options

The best options for directly modulated DFB lasers were on OEQuest. The important characteristics needed for our project are operating wavelength, data rate, and output power. Coincidentally, all the lasers are made by Optilab.

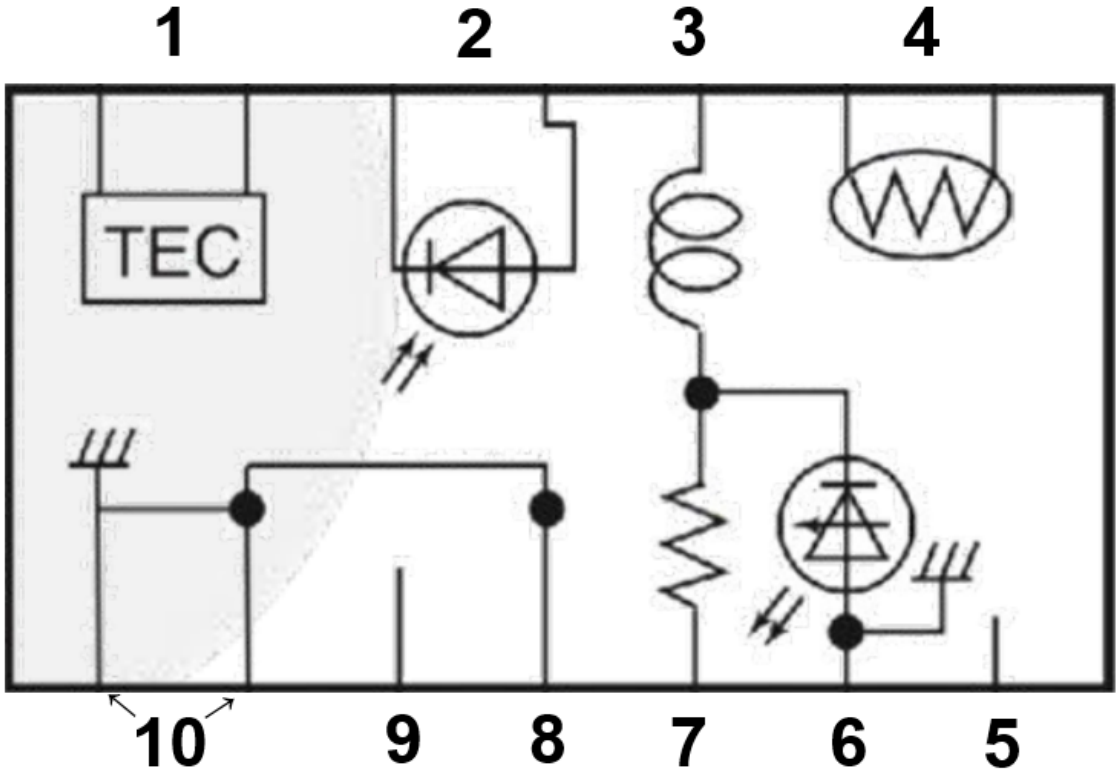



**Figure 50:** Optilab DFB Functional Diagram

**Table 4:** Optilab DFB Functional Diagram Legend

| Pin | Parameter | Pin | Parameter |
|---|---|---|---|
| 1 | TEC(+ and -) | 6 | Case Ground |
| 2 | Monitor (Anode and Cathode) | 7 | Laser Modulation (-) |
| 3 | Laser DC Bias (-) | 8 | Laser Ground |
| 4 | Thermistor | 9 | Not Connected |
| 5 | Not Connected | 10 | Case Ground |

A thermistor is a type of resistor whose resistance is directly related to temperature. The word itself is a combination of thermal and resistor. These resistors used as inrush temperature sensors (negative temperature coefficient or NTC type typically), current limiters, self-regulating heating elements (positive temperature coefficient or PTC type typically), and self-resetting overcurrent protectors. This relationship between resistance and temperature is highly dependent upon the materials from which the thermistor is composed. Thermistors are a type of semiconductor, meaning they display traits of both conductors and insulators. The two types of thermistors are Negative Temperature Coefficients (NTC thermistors) and those with Positive Temperature Coefficients (PTC thermistors). Resistance of NTC thermistors decreases as their temperature increases, while the resistance of PTC thermistors increases as their temperature increases. The relationship between resistance and temperature is linear and is given by:

$$\Delta R = k\Delta T$$

**Equation 4:** Linear Approximation Model Equation

Where ∆R is the change in resistance with units of ohms(Ω), ∆T is the change in temperature with units of Kelvin (K), and k is the first-order temperature coefficient of resistance. k can be positive or negative depending on the type of thermistor. Resistance increases with increasing temperature if k is positive. However, the resistance decreases with increasing temperature when k is negative. With resistors that are not thermistors, they are designed so that their k is as close to 0 as possible. This will allow the resistance to remain relatively constant over a wide range of temperatures. Using the linear approximation model above is only accurate over a limited temperature range. If a larger temperature range is needed, then a more complex approach is needed. Using a resistance–temperature transfer function provides a more reliable characterization of the performance of the thermistor. The function of choice is the Steinhart–Hart equation, as seen below:

$$\frac{1}{T} = a + b\ln(R) + c[\ln(R)]^3$$

**Equation 5:** Steinhart–Hart Equation

Where a, b, and c are called the Steinhart–Hart parameters and are specific for each device. R is resistance (Ω) and T is temperature (K). The above cubic equation in  can be solved to give resistance as a function of temperature. the real root of this equation is shown as:

$$\ln(R) = \frac{b}{3cx^{\frac{1}{3}}} - x^{\frac{1}{3}}$$

**Equation 6:** Real root of cubic equation

Where:

$$y = \frac{1}{2c}\left(a - \frac{1}{T}\right) \quad \text{and} \quad x = y + \sqrt{\left(\frac{b}{3c}\right)^3 + y^3}$$

**Equations 7 and 8:** Coefficients for cubic equation

Over a 200 °C range, the error in the Steinhart–Hart equation is generally less than 0.02 °C. Another form of the Steinhart–Hart equation for NTC thermistors that uses a B or β parameter can be expressed by:

$$\frac{1}{T} = \frac{1}{T_0} + \frac{1}{B}\ln\left(\frac{R}{R_0}\right)$$

**Equation 9:** Stein-Hart Equation with parameter B or β

Where:

$$a = \frac{1}{T_0} + \frac{1}{B}\ln(R_0) \quad , \quad b = \frac{1}{B} \quad , \quad c = 0$$

**Equations 10, 11, and 12:** B parameter conversion for Steinhart–Hart parameters

All temperatures are in K, is the resistance at a specified temperature . Solving for R gives:

$$R = R_0 e^{B\left(\frac{1}{T} - \frac{1}{T_0}\right)}$$

**Equation 13:** B parameter equation solved for R

Thermistors are used in lasers as an inexpensive and accurate temperature monitor. A large aspect of this project is trying to keep the system as cheap as possible. However, we should always try to maintain quality while still cutting costs; that is why devices like NTC thermistors are important.

The general purpose of a thermoelectric cooler (TEC) is to control the temperature (usually to cool) of an element within an electronic system. Thermoelectric cooling utilizes what is known as the Peltier Effect or the thermoelectric effect. An electric current is first passed through a thermocouple, which is an electrical junction consisting of two dissimilar conductors. This special junction allows for heat to be evolved at one junction and absorbed at the other. This “heat” is called Peltier heat and can be quantified by:

$$Q = (\Pi_A - \Pi_B)I$$

**Equation 14:** Peltier heat equation

Where $\Pi_A$ and $\Pi_B$ are the Peltier coefficients of the two conductors and they represent how much heat is carried per unit charge.  is the electric current going from A to B. Now the Peltier heat isn't the total heat generated, but rather a portion of it. This temperature difference is what gives TECs the ability to heat and cool electrical elements. TECs allow the operating temperature of a laser to be carefully monitored, which is important for precise laser applications medical procedures and 3D printing.

A monitor photodiode is used to monitor the main laser diode's optical power by using the photodiode's current as feedback. A control system will use this feed back to try to keep the optical power constant.

# 3.3.16.1 Optilab DFB-1547-DM-4

This laser has an operating wavelength of 1547 nm, data rate of 5 Gbps, and an output power of 20 mW. It has a built-in TEC, thermistor & monitor PD. The only problem with this laser is the operating wavelength; our project is based around using a laser that has an operating wavelength of 1550 nm. Therefore, this laser will not be considered.

# 3.3.16.2 Optilab DFB-1548-DM-4

1548 nm is the operating wavelength of this laser, the data rate of 5 Gbps, and an output power of 20 mW. The TEC, thermistor, and monitor PD are built in. This laser will not work for our project because the operating wavelength is too short; 1550 nm is the operating wavelength for our project. As a result, this laser was not considered any further.

# 3.3.16.3 Optilab DFB-1549-DM-4

The operating wavelength of this laser is 1549 nm, with a data rate of 5 Gbps, and an output power of 20 mW. It has a built-in thermistor, TEC, and monitor PD. However, this laser will not be considered because the operating wavelength is too short for our project, which is designed around a laser with an operating wavelength of 1550 nm.

# 3.3.16.4 Optilab DFB-1550-DM-4

This laser has an operating wavelength of 1550 nm, data rate of 5 Gbps, and an output power of 20 mW. It has a built-in TEC, thermistor & monitor PD. This is the most ideal laser for our project as it has an operating wavelength of 1550 nm. As a result. This is the laser our group will be using.

**Table 5:** Important laser specs.

| Laser Specifications | Values |
|---|---|
| Center Wavelength Range | 1547-1550 nm typ. |
| Optical Output Power | 20 mW typ., 17 mW min. |
| Threshold Current | 20 mA max. @ CW |
| Operating Current | 150 mA typ. @ CW |
| Laser Set Temperature | 10°C min., 40°C max. |
| Slope Efficiency | 0.16 mW/mA typ. |
| Monitor Current | 0.10 mA min., 1.0 mA max. |
| Laser Linewidth | 5 MHz typ. |
| Rise/Fall Time (10%-90%) | 100 ps typ. |
| Optical Fiber Type | SMF-28 |

Although this laser is designed to operate at 1550 nm, if it not operating in ideal conditions there could be some wavelength fluctuation within the center wavelength range. Optical output power and center wavelength range are the two most important values to look at. The output power of 20 mW will give us enough signal at the receiver end to successfully transmit data. Threshold current is the minimum current required for any lasing to occur. This comes into play when calculating what the low bit optical power and current will be. The operating current is what the laser will typically run at under normal operating conditions. The laser set temperature is a range of temperatures the laser can run at. The optimal operating temperature will have to be found experimentally. This value can heavily affect our data because of how sensitive semiconductor lasers are to temperature. SMF-28 is a type of optical fiber and is what comes with our Optilab laser. This is a non-dispersion-shifted fiber (NDSF), which means NDSF exhibits zero chromatic dispersion at a wavelength of 1550 nm.

# 3.4 Possible Architectures and Related Diagrams

This section will contain figures and diagrams of the proposed system. It will give visual aid to further understand the system from each discipline perspective with an explanation of design ideas and applied technologies.

## 3.4.1 System Electrical Diagram

The below figure is a basic overview of the component architecture and there interfaces, this visual aid provides connection details and structure for layout planning. Starting at the drone battery, this will be our power source. From the battery it will plug into a custom designed PCB with multiple integral power conversion circuits utilizing the aforementioned buck DC/DC voltage converters. The first circuit will then supply the power to the microcontroller, this connection will require thicker gauge wire than the others to deliver the estimated 15W at 5V.

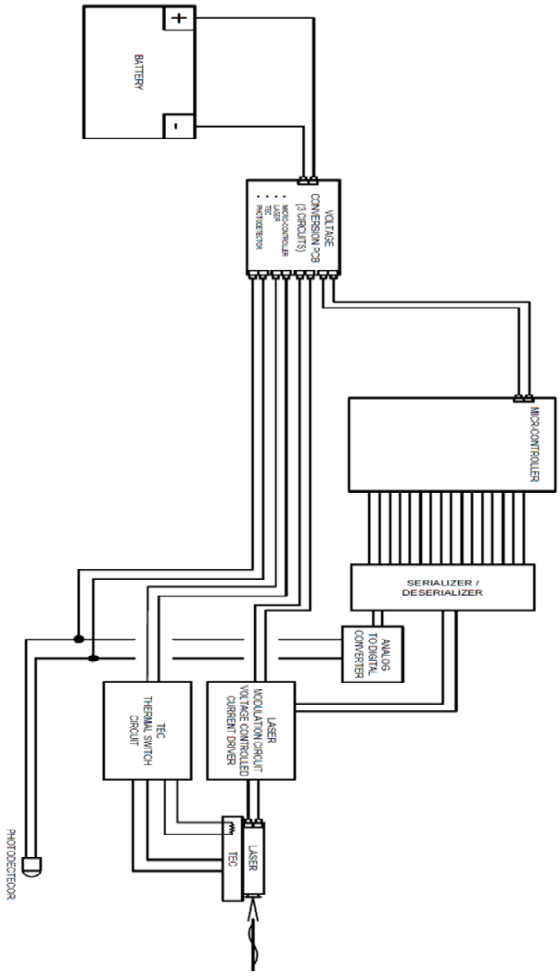



**Figure 51:** Overall Electrical Power Architecture

## 3.4.2 Computer Sub-system Diagram

The computer sub-system will act as the brains of the operation. This system will contain some type of controller that will be in charge of interpreting data provided by the team and transmitting it using the optical system to be received at another controller. This section provides an overview of the team's initial block diagram of the computer sub-system's design. Later sections will provide more details and more accurate depictions of the computer sub-system. For now, these block diagrams helped the team narrow their design process by identifying components that need to be researched, to find the specific component that will be used in the final design. Figure 40 shows the initial block diagram of the computer sub-system.

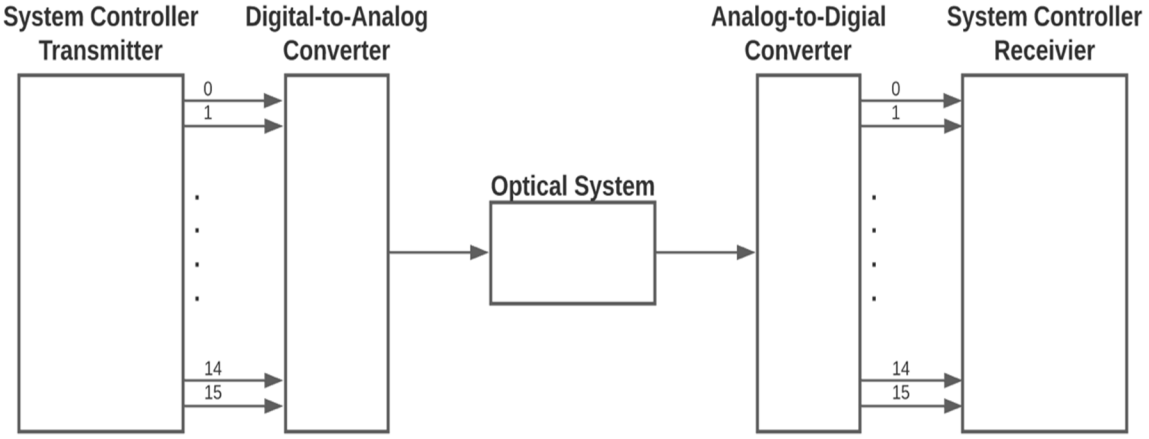



**Figure 52:** Initial block diagram of the computer sub-system

# 3.5 Parts Selection Summary

In the process of designing the initial system and selecting the correct parts it became apparently clear that we would be affected by global events. The electronics shortage and shipping crisis is a double whammy as the USA currently is only importing these parts. During the parts selection a great bit of knowledge was obtained that would have been useful before the process began. Such as the voltage converters have associated switching frequencies instead of an always on configuration. For the laser power supply specifically, the design might have to be changed in finding a component that can switch at a frequency between 900Mhz – 1.5GHz.

# 4.0 Related Standards and Realistic Design Constraints

This section will divulge into our design constraints and related standards for this project. Standards are important to keep manufacturing and public safety to a consistent measure.

# 4.1 Related Standards

https://www.ansi.org/education/standards-education-training

This section deals with the impact that realistic design constraints and industry standards will have on the S.T.E.A.L.T.H. system. Standards exist for nearly every type of project out there. Standards can come from multiple sources, but the most common and respected are The Institute of Electrical and Electronics Engineers Standards Association (IEEE SA), the Institute of Printed Circuits (IPC), and the America National Standards Institute (ANSI). IEEE SA and IPC are more for electrical engineering side of standards.

ANSI puts out a multitude of systems and electronic components, including laser standards. Laser standards fall under the Z136.1 Safe Use of Laser Standard section of ANSI. The United States government also puts out their own laser standards through the Center for Devices and Radiological Health (CDRH) which is a part of the Food and Drug Administration (FDA).

Standards play a huge role when projects involve international teams or involve multiple systems communicating with each other. They allow everyone on earth to follow the same set of requirements and specifications, which keeps everyone involved with a project “on the same page”. People also know that anything that is “built to standards” will be built to be safe and dependable.

Anytime a discussion involving technical standardization is had, it is unavoidable to not mention both the International Organization for Standardization (ISO) and International Electrotechnical Commission (IEC) which, together, make up the ISO/IEC Information Centre. There are multiple levels of standards that are used during the design process of the of a product. This includes, but is not limited to, international standards, national standards, and company level standards. This large range of standards established by these organizations help to lay the guidelines for a lot of unique and different applications.

As mentioned before, there are there are also multiple organizations that put out standards needed for building products. What about standards for finished products for the consumers? There are multiple companies that put out standards for things like this. For finished products that include circuitry like computers and

gaming consoles for example, high standards need to be set for safety purposes. This is especially true for products that children use. If a product starts causing injuries to its users, people will stop buying it. This in turn will cause profits to come down. There are various international Certification Bodies (CB), as shown below in Fig. X


**Figure 53:** Symbols and logos of Certification Bodies worldwide

# 4.1.1 Related Optics Standards

There are many standards that apply to the S.T.E.A.L.T.H. system. These range from optical standards to interface standards, as well as standards that contain recommendations for best practices when working with electrical equipment. The following sections outline the standards that the team found relevant to this project.

# 4.1.1.1 ISO 10110 Drawing Standard

The international standard for optics drawings was published in 1966. It is based loosely on the German DIN 3140 standard for optics drawings, which is a pictographic/symbolic notation system intended to reduce the language ambiguity associated with translation of notes. This can actually cause a problem for engineers and opticians trained in the United States, because most US drawings are notes-based, structured loosely on MIL-STD-34 optical drawings notation.
As of 2020, the US will implement WITHOUT MODIFICATION the ISO 10110 drawing standard. The changeover to use the ISO 10110 as an international standard is a huge step in making international standards the normal. The new series of American National Standards shall be called ANSI/OEOSC ISO 10110 and will be identical to the international version.

# 4.1.1.2 Surface Imperfections

MIL-PRF-13830B has various forms, but has been used as the standard for surface imperfections specification and measurement throughout the world since 1945. As time goes, however, as technology progresses, new demanding applications and technical savvy customers have been making this standard obsolete. The optics and photonics industry now has a choice of which standard to use, but the problem is, there is no clear choice for which comes next.
There is now ANSI/OEOSC OP1.002-2009, which is the newest offering for surface imperfections, based on the original MIL specifications, and the original MIL standards. ANSI/OEOSC OP1.002-2009 is recommended for anyone who needs a cosmetic specification for new optics. They have a minimum of conversion cost from the MIL methods. In turn offers the simplest path forward, as along as you can accept the "relative brightness" metric.

ISO 10110-7is the third option. This method is based mostly on the German DIN 3140 standard and is becoming increasingly popular in Europe and around the world. The difference with this standard is how surface scratches are noted. Most scratch standards are based on line width. However, this standard does allow for visual comparison, using chrome-on-glass comparison standards. Since chrome on glass has a very different "relative brightness" from "real" scratches on an optic, microscopes are often required to validate the smaller scratch widths. ISO 10110-7 is recommended for applications where actual scratch width, rather than brightness, is what matters in the application.

A new version of ISO 10110-7 and its sister metrology standard, ISO 14997 were published in 2017. Based on the MIL standard, the new version of the ISO surface imperfection standard includes a visibility notation. The new version sticks to the basic approach of a visual inspection of parts and a comparison standard for gauging scratches and digs but is more streamlined and simplified. The MIL and ANSI standards have virtually the same accumulation and concentration rules.

# 4.1.1.3 Mid-Spatial Frequency Ripple (Waviness)

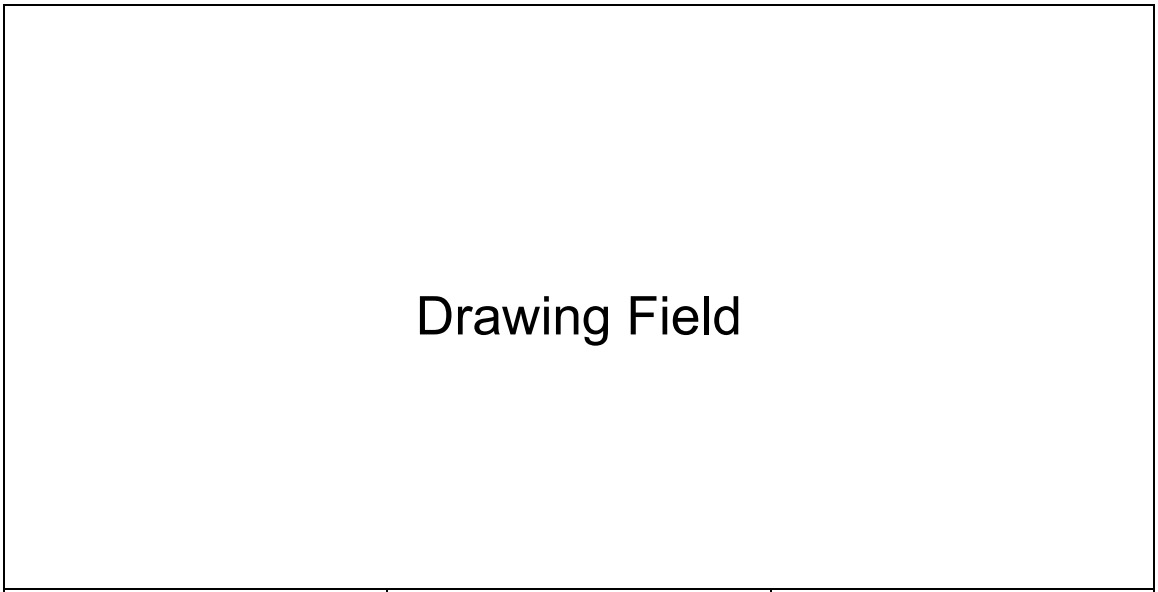
Ever-since the majority of the world converted to deterministic polishing methods for the manufacture of precision aspheres and even spherical optics, an entirely new type of form error has emerged. This error stems from the relative obscurity of X-ray optics and high-powered lasers becoming more and more mainstream. These modern deterministic polishing methods such as MRF or STP leave a

signature "ripple" in the surface form. This “ripple” is related to the tool size, the step size, and other polishing parameters.

Called "ripple" or "waviness," mid-spatial frequency (MSF) errors are typically defined as surface form errors. These errors are beyond the practical reach of Zernike specifications, which are around 5 or 6 cycles per diameter, but still too long a scale length to be practically evaluated using roughness measurement instruments. For example, on a typical 50 mm diameter optic, this would be the 5 mm to 0.1 mm spatial periods.

Surprisingly, for mid-spatial frequency ripple on optics, there is no clear best standards to use. Within the automotive industry, there is an excellent notation standard, ISO 10110-8. This standard allows the use of RMS surface texture over discrete wavebands. This allows for the use of the best analytic tool for MSF ripple, the power spectral density (PSD) of the surface profile. The PSD is a Fourier domain technique, which results in many manufacturers not being able to comfortably sign up to a PSD without some significant help. The most common methods to specify MSF ripple by are Judicious use of notes for RMS slope specifications or RMS surface errors versus spatial frequency bands are, but each has its weakness.

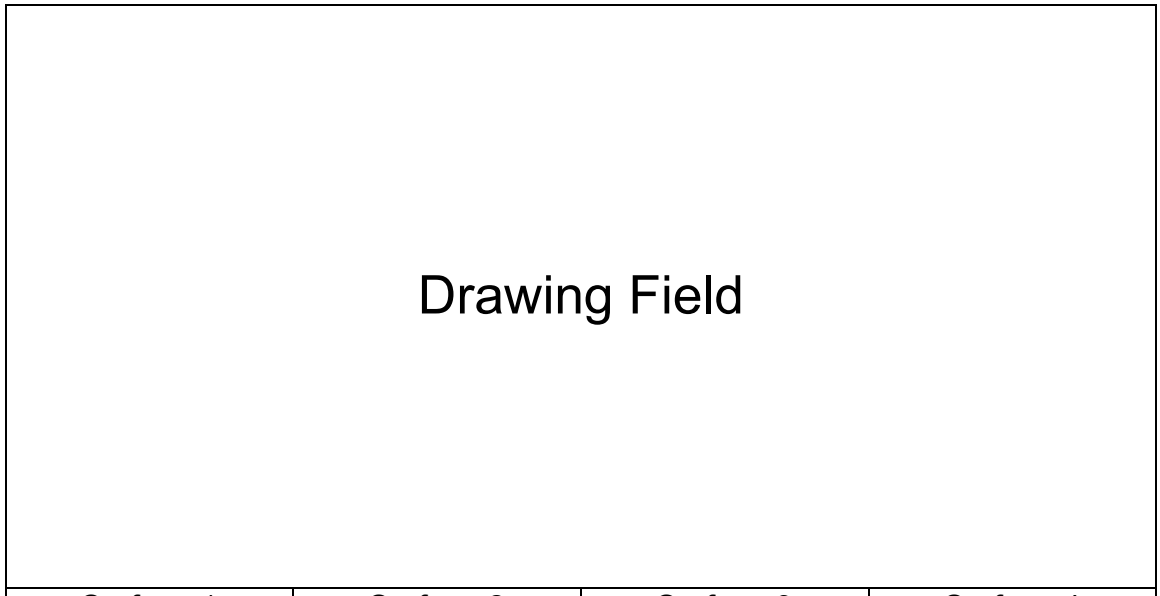
# 4.1.1.4 Drawing Presentation




| Surface 1 | Material Specifactions | Surface 2 |
|---|---|---|
| $R$ or surface type<br>$\emptyset_e$<br>Protective chamber | <br><br>$n$<br>$v$ | $R$ or surface type<br>$\emptyset_e$<br>Protective chamber |

| | | |
|---|---|---|
| $\lambda$<br>3/<br>4/<br>5/<br>$\sqrt{}$<br>6/ | 0/<br>1/<br>2/ | $\lambda$<br>3/<br>4/<br>5/<br>$\sqrt{}$<br>6/ |
| Indications in accordance with ISO 10110 | | $\lambda = 1550\ nm$ |

**Figure 54:** Tabular indication of data for a single optical element




| Surface 1 | Surface 2 | Surface 3 | Surface 4 |
|---|---|---|---|
| $\emptyset_e$<br>$\lambda$<br>4/<br>6/ | $\emptyset_e$<br>$\lambda$<br>4/<br>6/<br>Cement: | $\emptyset_e$<br>$\lambda$<br>4/<br>6/<br>Cement: | $\emptyset_e$<br>$\lambda$<br>4/<br>6/ |
| Indications in accordance with ISO 10110 | | | $\lambda = 1550\ nm$ |

**Figure 55:** Tabular indication of data for a cemented optical assembly (triplet)

# 4.1.1.5 U.S.C. Title 18 Chapter 2 Section 39A

Under Section 39A of Title 18 Chapter 2 of the US Code for aircraft and motor vehicles, it is considered an offense to knowingly aim the beam of a “laser pointer” at an aircraft or its flight path within the jurisdiction of the United States. In this section, a “laser pointer” is defined by any device that emits a laser light beam used to point to or designate an object or position. Violation of this law can result in up to 5 years of prison time and/or being subjected to a fine of up to $250,000. Our final product is intended to only be tested horizontally at or near ground level, so we do not expect to encounter any problems presented by this law, however, even in a future use case for S.T.E.A.L.T.H., the intended functionality of the

device as a communication system, combined with the lack of intentionality to point it at a manned aircraft should alleviate any potential violations of US Code. That being said, we still do not wish to be responsible for any undue harm to any airmen. This was an additional motivation for selecting an operating wavelength band that is eye safe, as discussed further in the safety considerations section of this report.

# 4.1.1.6 FAA 14 CFR 91.11

The Federal Aviation Administration (FAA) governs a similar piece of legislation under Title 14 of the Code of Federal Regulations (CFR), Part 91.11 which prohibits interference with any aircraft crewmember. This provision subjects anyone knowingly interfering with the duties of aircraft crewmembers to a fine up to $25,000 as of a 2016 increase via the FAA Extension, Safety, and Security Act. Interference under this bill in the case of a laser pointer incident the bill under Subtitle A of Title II (Aviation Safety Critical Reforms) shares the definition of a laser pointer offense under U.S.C. Title 18. Due to this interpretation, we do not expect to encounter any conflicts with FAA law even in the case of pointing these lasers across the sky at altitude.

# 4.1.1.7 Laser Classes

There are four classes of lasers: 1, 2, 3R, 3B, 4. Eye injury hazard increases as you go up in class number. Lasers must be in accordance with the accessible emission limit (AEL). This is the maximum possible laser radiation allowed within a specific classification. There are different safety thresholds that are measured in maximum permissible exposure (MPE). There are two organizations involved with laser hazard classification; they are The American National Standards Institute (ANSI) Z136.1 Safe Use of Laser Standard and The Center for Devices and Radiological Health (CDRH) which is a part of the Food and Drug Administration (FDA). Below is the FDA's description of laser classification.

**Table 6:** FDA laser classification

| Class FDA | Class IEC | Laser Product Hazard | Product Examples |
|---|---|---|---|
| I | 1, 1M | Considered non-hazardous. Hazard increases if viewed with optical aids, including magnifiers, binoculars, or telescopes. | laser printers, CD players, and DVD players |
| IIa, II | 2, 2M | Hazard increases when viewed directly for long periods of time. Hazard | bar code scanners |

| | | | |
|---|---|---|---|
| | | increases if viewed with optical aids. | |
| IIIa | 3R | Depending on power and beam area, can be momentarily hazardous when directly viewed or when staring directly at the beam with an unaided eye. Risk of injury increases when viewed with optical aids. | laser pointers |
| IIIb | 3B | Immediate skin hazard from direct beam and immediate eye hazard when viewed directly. | laser light show projectors, industrial lasers, and research lasers |
| I4 | 4 | Immediate skin hazard and eye hazard from exposure to either the direct or reflected beam; may also present a fire hazard. | laser light show projectors, industrial lasers, research lasers, and medical device lasers for eye surgery or skin treatments |

As a comparison, below is The American National Standards Institute Z136.1 Safe Use of Laser Standard's table for laser classification. One can see that ANSI's table is more gauged towards safety in a professional environment rather than recreational and professional laser usage.

**Table 7:** ANSI requirements by laser class

| Class | Control Measures | Training | Laser Safety Officer (LSO) | Engineering Controls |
|---|---|---|---|---|
| 1 | Not Required | Not Required | Not Required | Not Required |
| 1M | Required | Application Dependent | Application Dependent | Application Dependent |
| 2 | Not Required | Not Required | Not Required | Not Required |
| 2M | Required | Application Dependent | Application Dependent | Application Dependent |
| 3R | Not Required | Not Required | Not Required | Not Required |
| 3B | Required | Required | Required | Required |

| | | | | |
|---|---|---|---|---|
| 4 | Required | Required | Required | Required |

Safety is of paramount importance when dealing with devices such as lasers. Therefore, we have compiled what we think are the most common laws and recommendations for laser safety requirements in the tables below.

**Table 8:** Compiled Class 1 laser safety requirements

| ANSI and IEC laser classification | Class 1 | |
|---|---|---|
| Sub-class | Class 1 | Class 1M |
| U.S. FDA laser classification | Class I | No special FDA class |
| Human-accessible laser power (for visible light) | Emitted beam must be below 0.39 mW and not accessible during laser operation. | |
| Warning indication | No warning indication. | |
| Label descriptive text | | DO NOT VIEW DIRECTLY WITH OPTICAL INSTRUMENTS |
| EYE AND SKIN HAZARDS | | |
| Eye hazard for intraocular exposure | Long-term intentional viewing is safe. | Safe for unassisted eye exposure. Can become hazardous if viewed through optical devices. |
| Maximum or typical Nominal Ocular Hazard Distance | NA | Probably safe but best to consult an LSO. |
| Eye hazard for diffuse reflection exposure | None | |
| Skin burn hazard | None | Talk to LSO |
| Materials burn hazard | None | Talk to LSO |
| | | Talk to LSO |

| | | |
|---|---|---|
| VISUAL INTERFERENCE DISTANCES | | Talk to LSO |
| Maximum or typical flashblindness distance | NA | |
| Maximum or typical glare distance | NA | Talk to LSO |
| Maximum or typical distraction distance | NA | Talk to LSO |
| Technical notes | A lot class 1 lasers are labeled as Class 2 | Class 1M lasers are not made for consumer use, but if you come across one, talk to an LSO |

**Table 9:** Compiled Class 2 laser safety requirements

| ANSI and IEC laser classification | Class 2 | |
|---|---|---|
| Sub-class | Class 2 | Class 2M |
| U.S. FDA laser classification | Class II | No special FDA class |
| Human-accessible laser power (for visible light) | Emitted beam must be less than 1 mW. | NA |
| Warning indication | No warning indication | NA |
| Label descriptive text | DO NOT STARE INTO BEAM | DO NOT STARE INTO BEAM OR EXPOSE USERS OF TELESCOPIC OPTICS |
| EYE AND SKIN HAZARDS | | |
| Eye hazard for intraocular exposure | Do not stare into laser. Accidental exposure under 0.25 s is okay. | Accidental unaided exposure under <0.25 s is okay. Do not stare into beam. |
| Maximum or typical Nominal Ocular Hazard Distance | NOHD of 0.99 mW beam: 7 m | Talk to LSO |
| Eye hazard for diffuse reflection exposure | None | Talk to LSO |
| | None | Talk to LSO |

| | | |
|---|---|---|
| Skin burn hazard<br>Materials burn hazard | None | Talk to LSO |
| VISUAL INTERFERENCE DISTANCES<br>Maximum or typical flashblindness distance<br>Maximum or typical glare distance<br>Maximum or typical distraction distance | For a 0.99 mW beam: 36m<br>159 m<br>1593 m (1.6 km) | Talk to LSO<br>Talk to LSO<br>Talk to LSO |
| Technical notes | Infrared and ultraviolet lasers cannot be under Class 2 or 2M and under, as those classes only apply to lasers that emit light in the visible range | Class 2M lasers are not made for consumer use, but if you come across one, talk to an LSO |

**Table 10:** Compiled Class 3 laser safety requirements

| ANSI and IEC laser classification | Class 3 | |
|---|---|---|
| Sub-class | Class 3R | Class 3B |
| U.S. FDA laser classification | Class IIIa | Class IIIb |
| Human-accessible laser power (for visible light) | Emitting beam must fall within the range of 1 mW and 4.99 mW for visible light. | Emitting beam must fall within the range of 5 mW and 499.9 mW for visible light. |
| Warning indication | CAUTION | WARNING |
| Label descriptive text | AVOID DIRECT EYE EXPOSURE | AVOID EXPOSURE TO THE BEAM |
| EYE AND SKIN HAZARDS<br>Eye hazard for intraocular exposure | Direct or reflected accidental exposure has a low risk. Avoid direct | Eye hazard, avoid direct or reflected beam exposure. |

| | | |
|---|---|---|
| Maximum or typical Nominal Ocular Hazard Distance | or reflected beam exposure.<br>NOHD of 4.99 mW beam: 16 m | NOHD of 499.9 mW beam: 160 m |
| Eye hazard for diffuse reflection exposure | None | Safe in general. Try not to stare at the laser spot for multiple seconds at close range. |
| Skin burn hazard | None | If beam is held on skin long enough at close range, the skin can start to heat up. |
| Materials burn hazard | None | If beam is held on material long enough at close range, the material can burn. |
| VISUAL INTERFERENCE DISTANCES | | |
| Maximum or typical flashblindness distance | For a 4.99 mW beam: 80m | For a 499 mW beam: 797 m |
| Maximum or typical glare distance | 356 m | 3563 m (3.5 km) |
| Maximum or typical distraction distance | 3563 m (3.5 km) | 35,628 m (35.6 km) |
| Technical notes | Class 3R is either: Five times the Class 2 limit of 2.5 mW/cm2, which works out to be 12.5 mW/cm2 or from 1 to 4.99 mW into a 7mm aperture (e.g., pupil of the eye) | NA |

**Table 11:** Compiled Class 4 laser safety requirements

| | |
|---|---|
| ANSI and IEC laser classification | Class 4 |
| Sub-class | Class 4 |
| U.S. FDA laser classification | Class IV |
| Human-accessible laser power (for visible light) | Emitting beam has an optical power of 500 mW or more for visible light. |
| Warning indication | DANGER |
| Label descriptive text | AVOID EYE OR SKIN EXPOSURE TO DIRECT OR SCATTERED RADIATION |
| EYE AND SKIN HAZARDS | |
| Eye hazard for intraocular exposure | Severe eye hazard, avoid direct or reflected beam exposure. |
| Maximum or typical Nominal Ocular Hazard Distance | NOHD of 1000 mW beam: 224 m<br>NOHD of 10 W beam: 710 m |
| Eye hazard for diffuse reflection exposure | If you stare at the laser spot for an extended period of time, you could see an afterimage that lasts up to 10 seconds. |
| Skin burn hazard | Can and will instantly burn skin. Avoid direct or reflected beam exposure. |
| Materials burn hazard | Can and will instantly burn material. Avoid direct or reflected beam exposure, especially when working with materials susceptible to burning. |
| VISUAL INTERFERENCE DISTANCES | |
| Maximum or typical flashblindness distance | For a 1 Watt beam: 1,127 m (1.1 km)<br>For a 10 W beam: 3,563 m (3.5 km) |
| Maximum or typical glare distance | For a 1 Watt beam: 5,039 m (5 km)<br>For a 10 W beam: 15,933 m (16 km)<br>For a 1 Watt beam: 50,386 m (50 km) |

| | |
|---|---|
| Maximum or typical distraction distance | For a 10 W beam: 159,333 m (160 km) |
| Technical notes | NA |

There are so many different laser wavelengths to choose from, why is 1550 nm the best? One of the biggest advantages is there is lower attenuation at longer wavelengths, which means less fiber loss. The average attenuation for this wavelength is around 0.2 dB/km. 1550 nm is within the C-band (1525-1565 nm), and this range is commonly known as the “zero loss window”.

# 4.1.2 Related Electrical Standards

Electrical standards are important for setting a widespread set of guidelines that will be followed to primarily keep people safe. These are important as it keeps quality of products generally consistent in minimum requirements to function. For example, in industrial electrical engineering consulting you have to abide by the NEC. The NEC lays out everything from wire and breaker sizing requirements, to grounding requirements. By doing this, they have also given everyone a useful tool to learn how to design systems in an efficient, functional way.

# 4.1.2.1 UL 1642 – Lithium Batteries

The Underwriters’ Laboratories (UL) developed this standard to outline different test standards and minimum requirements for products to gain the UL listed status. This standard includes sections, construction, to define materials and protocols. The performance section contains, standards on technician and user replaceable batteries, these outline tests that the technician must conduct before replacing a battery.

# 4.1.2.2 IPC-A-610G Acceptability of Electronic Assemblies

This standard is produced by IPC which is a trade association. They have developed this standard and it is widely used for quality control. This standard covers ESD prevention, hardware installation, wire routing and bundling and much more. This standard will provide the design team in the correct procedures and guidance for designing and assembling our custom PCBs. [ICB-A-610G]

#### 4.1.2.3 IPC-J-STD-001G Acceptability of Electronic Assemblies

This is another standard produced by IPC. This standard is a quality control document for soldering that includes materials and methods to produce functional quality products. Covering items such as different types of connections and how to install them, and cleaning procedures for proper adhesion of solder. [IPC-J-STD-001G]

### 4.1.3 Related Computer Standards

The standards discussed in the following subsections are relevant to the computer subsystem of the S.T.E.A.L.T.H. project. These standards are ways of transmitting information that are employed by the serializer and de-serializer, helping the team interface with the FPGA and achieving the transmission speed requirements set by the project.

#### 4.1.3.1 Low-Voltage Differential Signaling

With the increase in high-speed processor technology, data transmission at the physical layer has not been able to cope with the high bandwidth of applications such as high-resolution multi-media, like video and audio. Transmission standards like RS-422/485 have many limitations, including the number of pins required to use and lower speeds. The low-voltage differential signaling (LVDS) fixes many of the issues by being able to transmit data at much higher speeds. Two industry standards define LVDS, the more common of the two being ANSI/TIA/EIA-644. LVDS uses differential data transmission, meaning that it transmits information as the difference between two voltages on a pair of wires. TIA/EIA-644 defines the driver output and receiver input characteristics. The differential voltage is interpreted at the receiver end. Signal quality is an important aspect of LDVS I/O to consider in design. There are numerous ways of determining signal quality on the transmission media. Bit Error Rate (BER), jitter, eye pattern, ratio of rise time and unit interval are some of the different ways designers use to determine signal quality.

For S.T.E.A.L.T.H., LVDS will be employed at the output of the serializer. The serializer takes in an input of 16 bits in parallel and reduces it to a differential serial stream using only two pins. The LVDS standard has enabled engineers to design systems with speeds between 155 megabits per second (Mbps) and 1.5 gigabits per second (Gbps), which is relevant to this project since the system is aiming transmission speeds of 1 Gbps. The signal quality will also need to be considered at the serializer output to ensure that the data transmitted is valid and that the system is working correctly.

#### 4.1.3.2 Low-Voltage Complementary Metal Oxide Semiconductor

The low-voltage complementary metal oxide semiconductor (LVCMOS) I/O is a CMOS technology that enables the interface of digital integrated circuits at various low voltage levels. A subset of the low-voltage transistor-transistor logic (LVTTL), which uses 5-volt levels only, LVCMOS was introduced by the Joint Electron Device Engineering Council (JEDEC), to reduce the voltage levels of I/O below 5 volts. Many voltage levels were standardized by JEDEC, including 1.0, 1.8, and 3.3 volts, among others. LVCMOS I/O standard is also used to match the impedance of the input and output line, as well as the input port and the output port. LVCMOS I/O is also able to reach data rates of 200 Mbps.

The operation of LVCMOS states that, taking a 3.3 volts level, for example, a logic level of low will be 0 (or ground) and a logic level of high will 3.3 volts. This makes it easy for components to interpret digital logic. For S.T.E.A.L.T.H., LVCMOS will be used to interface the Raspberry Pi 4 Model B output pins to the serializer input pins, since that is the standard defined by the serializer's datasheet.

#### 4.1.3.3 ANSI/ESD S20

The ANSI/ESD S20 is an industry standard that outlines the development of electrostatic discharge (ESD) control programs to protect sensitive electronic components, assemblies, and equipment. Examples of ESD sensitive items include microcontrollers, integrated circuits, and printed circuit boards. Most commonly, this standard also requires a certification to allow engineers to work with ESD sensitive items. One source of electrostatic discharge is the human body. To work around this, the use wrist straps connected to a grounding system should be used, as well as using static matting placed on work areas to protect these sensitive equipment's and components. This standard is very relevant to the team's timing constraints. An ESD sensitive device must be protected to reduce the risk of damaging such device and having to waste time procuring new products.

## 4.2 Design Constraints

As engineers, it is our job to design real world solutions to real world problems. With real world problems, come realistic design constraints that must be met to ensure a successful end result. These design constraints come in various forms, they can be based on anything from economics, to ethics, to safety and many more niche rational in between. Each type of project will have unique constraints, but it is important to clearly identify them from the onset so as to not hit a speed bump or roadblock further into project development.

### 4.2.1 Economic Constraints and Time Constraints

The cost of designing this system is a major constraint. Some components are very expensive, such as a high-quality laser, or, surprisingly, analog-to-digital converters that are able to read at greater than one giga-sample per second. Some economic and time constraints that are affecting this project more than anticipated. With the global microchip shortage we are seeing cost of items increasing, as well as long lead times for shipping. This is affecting our project as premium components are not available anymore. This forces us to buy products that are less efficient. With some of the components not even being available forcing different designs.

Some economic and time constraints are affecting this project more than anticipated. This supply chain issue also places timing constraints on the team. Electronic components that may have taken a couple of weeks to procure in years prior are now listing their lead times at over a month. Given that Senior Design will end in May 2022, the team must be able to procure components at a fast speed. At the latest, the team must procure all components by the end of Senior Design 1 before the beginning of Senior Design 2. This will allow the team to have sufficient time for testing and redesign, with the tradeoff being that the components procured may not be the team's first choice.

### 4.2.2 Manufacturability and Sustainability Constraints

As mentioned before, procurement of parts will be a major limitation for the team. For this reason, it is important to decide to use components that will be available for a long time. At the controller side of the system, it is important that manufacturers mention support for their components for at least a year, meaning that for the duration of the design and building of the system, the team will have support when troubleshooting. Stock is also a major limitation. After some component research, many manufacturers and vendors only sell in quantities of 1000 units, way out of the range required by the team. It is also important to consider if stock is only available at less than 100 units, limiting the chances of the team actually obtaining said parts before they go out of stock.

When considering sustainability for this project, one major concern is transmission speeds. With related products on the marked already discussed in previous sections of this report, it is important that this product is able to compete with these already available products. Considering the product from a military standpoint, it is important that the product is able to transmit data quickly and reliably. Data speeds play a major role in determining if the product will remain on the market and future

iterations will build upon this design, or if the product won't survive in the market at all.

### 4.2.3 Environmental, Health, and Safety Constraints

There is a strong push for new technologies to be environmentally conscientious. The S.T.E.A.L.T.H. system will be run entirely off a battery that can be recharged. Moreover, at the controller side, the system will focus on using low-power consuming components. The Raspberry Pi is the most power-consuming component, requiring 30 watts to function. The serializer and de-serializer circuit DS92LV16, is a low-power chip, using technology like LVCMOS and LVDS, which are transmission standards that use low voltages at high speeds. This will allow the battery to focus on providing power to the optical side of the system, since that is the most demanding part of S.T.E.A.L.T.H., and reduce the amount of power consumed by the system as a whole from the battery.

In a system like S.T.E.A.L.T.H., safety is a very relevant constraint. Working with a laser, the team will have to consider what are safe levels of exposure, especially to human eyes. Moreover, the computer sub-system but be adequately taken care of. Electrostatic discharge, for example, is an issue that can affect the team's timing and economic constraints by damaging equipment and components. Great care must be taken when working with voltage polarity, because that may cause integrated circuits and PCBs to become damaged as well.

Environmental concerns reside in the beginning and end of electronic life cycles. Whether it be batteries or microchips or solar panels. All these products require either large machinery that pollute the environment as well as disturb the local fauna of which they are operating in. At the end of their life cycles many people throw things away as opposed to recycling. As well as recycling being very inefficient these components typically end up polluting a landfill. Safety standards allow for safe operation and handling of dangerous materials as well as protect people from electrocution.

### 4.2.4 Ethical, Social, and Political Constraints

An ethical positive is this system is capable of providing communications to undeveloped areas with a lower construction cost than installing physical cables. Socially and politically this system may be divisive, with the end goal being for a vehicular application, the security provided by this point-to-point communication system will be beneficial as it will be more difficult for information to be intercepted.

# 5.0 Project Hardware and Software Design Details

The design of the system is divided into four different sections. These sections are the initial optics design, initial electrical design, initial computer design, and initial software design.

# 5.1 Initial Optics Design

As a primarily optics driven project, there are many important initial optical design considerations that must be considered in order to prepare for a successful project. The needs optical elements of this project inform the requirements of the electrical project elements, meaning that flaws in the optical design trickle down throughout the entire project. For this reason, thorough attention has been paid to understanding and optimizing the optical design portion of this project.

# 5.1.1 Receiving Aperture Design

When approaching the problem of which lens we wanted to select for to collect light at our receiving end, we asked ourselves, what are the parameters of an optic that best suits our system? First and foremost, we had to select a lens material and/or coating combination that is as transmissive or antireflective as possible for the 1550 nm light that we wish to collect. AR coated N-BK7 and V-Coated N-SF11 were evaulated, but ultimated N-SF11 has been selected for its less than 0.25% reflectance at our operating wavelength of 1550 nm. Due to the desire to allow our beam to diverge to a point where it has expanded enough to alleviate pointing requirements for establishing a link, we knew that the amount of irradiance we would get at our goal range of 1 km would be relatively small compared to our output power. To mitigate this issue, we want to collect as much light as possible, requiring a large receiving aperture. This allows us to maximize the amount of power we are able to focus onto the sensor. We selected 2 inches (50.8 mm) as a receiving lens diameter in order to maximize the amount of light collected by the receiving system, while not distorting the envisioned form factor of our final product. In addition to the aperture diameter needs, our lens needs to have a relatively short focal length which increases the angular field of view and reduces the f/# of the lens. We selected a 50 mm focal length as it was the shortest focal length available for a readily available off the shelf 2 inch lens. Havinga shorter focal length also aids in alleviation of pointing requirements by allowing for a smaller focal spot which in the idealized case of a Gaussian beam is given by:

$$d = \frac{4 \cdot f}{\pi \cdot D} \cdot \lambda = \frac{4 \cdot 50\ mm}{\pi \cdot 50.8\ mm} \cdot 1550\ nm = 2\ \mu m$$

**Equation 15**: Focal Spot of a Gaussian Beam

Here *d* is the focal spot size, *f* is the focal length of the lens, $\lambda$ is the wavelength of our source, and *D* is the size of our collecting aperture. This small spot size is appreciated as in a mobile use case of this system, vibrational jitter could cause the focal spot to wander about the face of the photodetector, so it is valuable to have a focal spot that is comparatively small to the size of the face our photodiode as seen below in Figure 46.

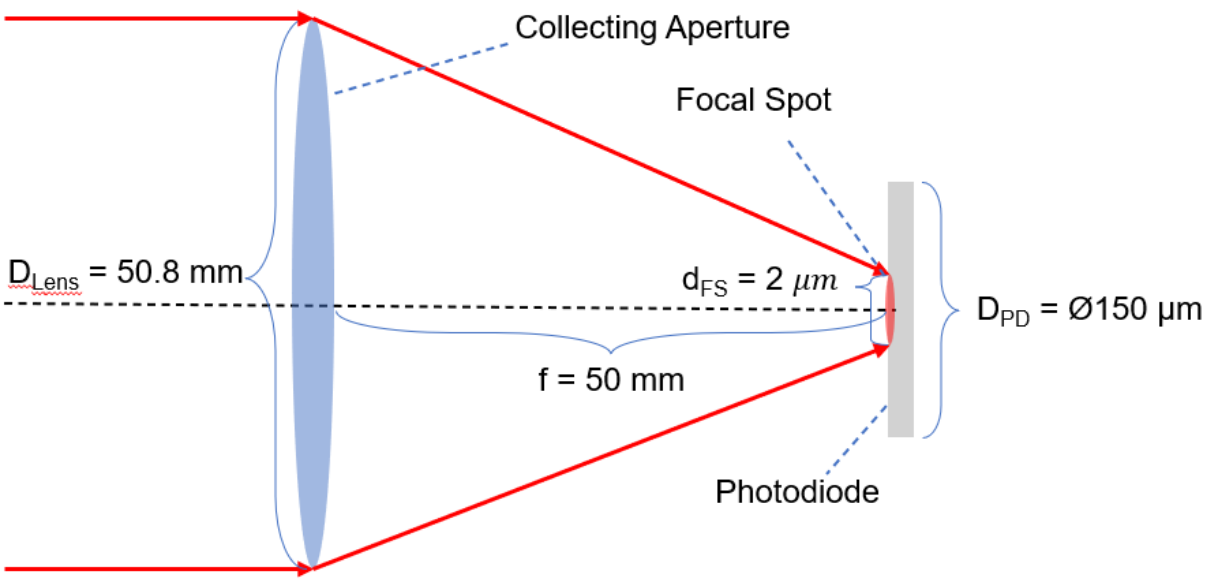



**Figure 56:** Light is collected by the receiving end and focused down to a focal spot of size $d_{FS} \approx 2$ μm at a distance $f = 50$ mm behind the lens

The maximum angle at which rays can enter the receiving side of the system is defined by the angular field of view. This field of view can be determined as a function of the sensor size and the size of the collecting aperture. The equation to determine the angular field of view for a fixed focal length lens is given by:

$$AFOV = 2 \cdot \tan^{-1}\left(\frac{H}{2} \cdot \frac{1}{f}\right) = 2 \cdot \tan^{-1}\left(\frac{150\ \mu m}{2 \cdot 43.28\ mm}\right) = 3.466\ mrad$$

**Equation 16:** Angular Field of View of the lens-photodiode system

In the above equation, H/2 is half of the diameter of the photodiode's active area onto which we are trying to focus our collected light, and f in this case is the back focal length of the lens, not the lenses effective focal length. This field of view can also be thought of as a solid angle by considering a cone whose half angle is half of the angular view of view such as:

$$\Omega = 2\pi\left(1 - \cos\left(\frac{AFOV}{2}\right)\right) = 2\pi(1 - \cos(0.001733)) = 9.43 \times 10^{-6}\ sr.$$

**Equation 17:** Solid angle of receiver as defined by the angular field of view

# 5.1.2 Optical communication considerations

When describing the speed at which one can transmit data with a digital optical communication system, the bit rate parameter is used. Bit rate can be thought of as the digital equivalent to system bandwidth in analog communication. It is the number of bits that can be communicated per unit time and is often described in units of bits per second. Digital communication signals resemble square waves in shape, and the frequency of these square wave-sequel signals is proportional to system bit rate. To achieve a high bit rate, all of the core components of the system must operate at a frequency equal to the desired bit rate. For instance, the response time of a photodiode used to receive a signal on the receiving end of an optical fiber must be small enough that it can respond to 1,000,000,000 distinct changes in power to enable a 1 Gbps bit rate in 1-bit digital communication. It is worth noting that there are advanced methods that enable higher speeds as a function of equivalent hardware limitations by communicating more than one bit at a time such as by employing more than 2 optical power levels, however these methods are not going to be used for S.T.E.A.L.T.H.

Bit error rate (BER) describes the number of incorrectly communicated bits, also referred to as bit errors, per second. BER is an important parameter to minimize to optimize an optical communication system. When measuring bit-error rate, it is not always obvious where in the system the sources of bit error occurrences are coming from. To identify these flaws, eye diagrams can be used to help characterize, understand, and improve the system. An eye diagram is essentially a single diagram that simultaneously displays all the signal waveform features in one figure. Although digital signals resemble square waves in terms of their waveform features, no real-world digital signal has perfectly square features, as physical hardware limitations will necessitate some finite minimum rise and fall times. Features of the eye diagram of a system correspond to different qualities affecting BER. For instance, the slope of the rising and falling diagonals of the eye correspond to system sensitivity to timing errors. The smaller this slope is, the less likelihood that a timing error. This is because the longer the period between a 1 and 0 in the bit stream, the more likelihood that a bit decision is erroneously made during the rise and fall, which is undesirable. The larger the middle opening of the eye, generally the better signal to noise ratio of the system. The smaller the eye opening, the more noise causing unwanted signal variation. The vertical size of the top and bottom horizontal lines of the eye diagram correspond to the signal distortion, as these show variance in the high and low (1 and 0) bit energy levels. All these factors can result in bit errors, which increase the BER. By examining the system output on an oscilloscope as you tune it, and checking against the changes

in the eye diagram, as these eye diagram features are improved, the BER is thus minimized.

## 5.1.3 Atmospheric Effect Considerations

Despite S.T.E.A.L.T.H. being a free space optical communication system, in the real world, free space propagation within Earth's atmosphere is not true free space. Due to atmospheric effects, such as atmospheric turbulence, even a free standing system not on a moving aerial platform will undergo some effects due to the atmosphere, and it is important to have a baseline understanding of what these effects are, how they might impact performance, and what can be done to mitigate negative externalities due to atmospheric conditions.

While this system is intended for future use on platforms such as drones that are not typically used in precipitous weather conditions, atmospheric aerosol matter such as dust, smoke, or fog can still impede signal transmission via beam attenuation. One mitigating step taken for our system was to select a wavelength with a high atmospheric transmission coefficient, as seen in the following link budget section. With a high atmospheric transmittance, atmospheric extinction is due to absorption is low enough to achieve successful signal transmission at long propagation distances without problematic levels of signal loss. Additionally, signal loss that does occur can be compensated for via pre and post transmission electrical signal gain. While these factors mitigate risks caused by attenuation over the propagation distance to successful signal recovery on the receiving end, they do not fully eliminate the potential sources of errors that can be induced by atmospheric effects.

Atmospheric turbulence in the optical transmission channel induces signal losses that similarly to attenuation, increase as a function of propagation distance. While longer wavelengths feel these effects less, meaning our 1550 nm signal should fare better than visible spectrum light, it is not immune to turbulence effects. When a beam travels through the atmosphere, it experiences many changes in effective refractive index of the air, which is why transmission within the atmosphere can not be treated as truly pure free space propagation like that in a volume. Even if the effective indices of the atmosphere that are changing are all near n = 1, the traveling through these changes cause the beam to incur small phase change effects in 3 dimensions, whose cumulative effects over the entire propagation distance can be significant in magnitude.

One of the chief causes of atmospheric refractive index variation is due to atmospheric density and temperature gradients, which within a small proximity are approximately equal in the horizontal direction but have much variation in the vertical direction. The strength of atmospheric turbulence effects on the optical channel are characterized using the refractive index structure parameter $C_n^2$, which is a typically measured value that helps us predict the degree of atmospheric effects on beam propagation. $C_n^2$ varies by location, as different locations

experience different atmospheric environments. There is a popular model which we may use in the future that provides a generalized clear weather $C_n^2$ profile for inland locations known as the Hufnagel-Valley. An example from the Hufnagel-Valley data set versus various local atmospheres can be seen below as HV 5/7 in Figure 57.

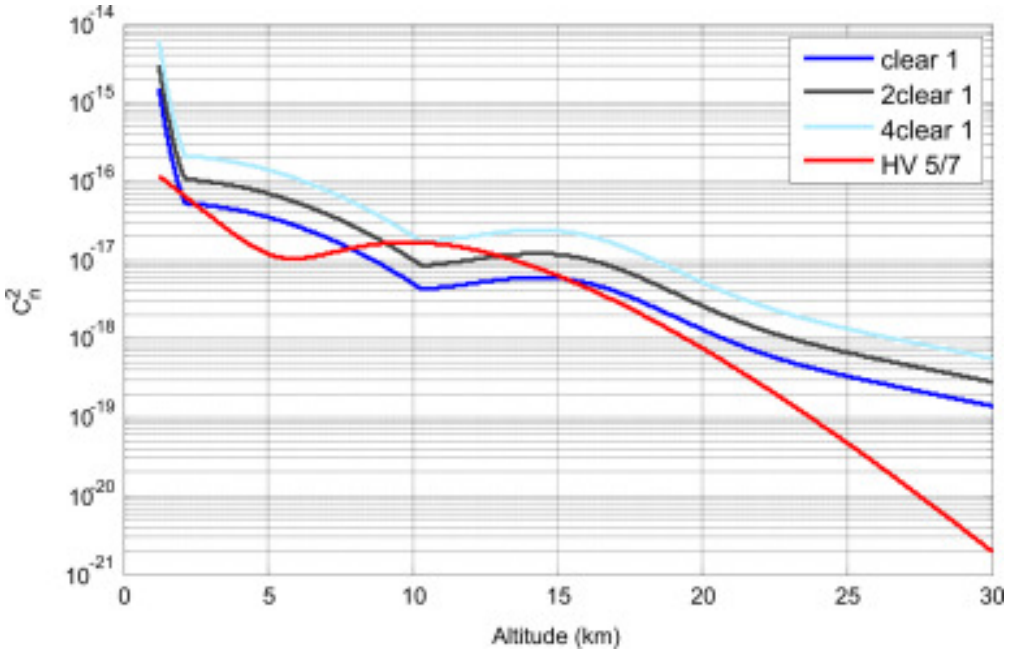



**Figure 57:** A collection of Cn2 datasets plotted against the Hufnagel Valley 5/7 model (standard generalized atmospheric turbulence model)

Some additional parameters to consider when thinking about the atmospheric effects on beam propagation include the Fried parameter $r_0$ and the Greenwood time constant $t_0$. The Fried parameter, or atmospheric coherence diameter describes the size of an average chunk of uniform air within a turbulent propagation path. The Greenwood time constant, the time-scale over which alterations in atmospheric turbulence become significant. As the beam propagates, the turbulence of the atmosphere, as described by $C_n^2$, induces changes to the phase information of a complex field. The distance that these changes occur at is estimated by $r_0$. Using these factors, we can analytically examine the wave optics effects incurred by the atmospheric turbulence using the following equation.

$$U(\mathbf{r}) = U_0(\mathbf{r}) \exp[\psi(\mathbf{r})]$$

**Equation 18:** Modified Wave equation including atmospheric turbulence phase factor

If we treat $U_0(r)$ as the solution of the wave equation in a vacuum, $\psi(r)$ is the remaining phase argument that need be accounted for in atmospheric propagation.

In practice when you consider all of this atmospheric wave optics theory, the primary concerns raised by signal transmission in the atmospheric optical channel is this: if cumulative phase changes over a long enough propagation distance sum to a large enough magnitude, the beam can spend some amount of time missing the target (i.e. receiver module), and thus some information in the bit stream is lost. This is because the phase changes in the beam can change the beams cross sectional intensity profile with propagation length, so an initially Gaussian beam at the transmit end will no longer appear Gaussian at the receive side and could warp in shape such that there is not enough intensity on axis (the portion of the beam cross section into the collecting aperture) to correctly receive the signal. There are error correction methods, such as forward error correction in the bit stream, that can be introduced to aid in mitigating this, but they come at the cost of bandwidth or bit rate. However, such sacrifices may be necessary to ensure a sufficiently low bit error rate that meets the standards when compared to other telecommunication protocols. When talking about optical fiber communication, typically a maximum BER of $10^{-9}$ or better is expected, meaning that the signal on average incurs no more than 1 error in every $10^9$ bits. Or in our case at our goal 1 gigabit speed, no more than one error per second on average. Future modeling of atmospheric propagation of our system will help inform the degree of steps needed to compensate adequately for atmospherically induced bit errors and create a system with an acceptable bit error rate.

# 5.1.4 Link Budget

The successful design and creation of any telecommunication system relies on the establishment of an accurate link budget, which accounts for the gains and losses experienced by the signal from the transmitter output, over the propagation distance, and into the receiver input. Within the realm of free space optical communication typical link budget parameters could include Transmitted power, transmission losses due to each interface encountered (Fresnel transmission coefficient of lenses), transmission losses across the free space propagation path (atmospheric transmission losses), losses due to beam divergence, and losses due to received power constraints (inability to focus all light from receiving end onto detector active area). The output of this link budget calculation must be weighed against the sum of the photodiode dark current and background power witnessed by the detector. In the case of an outdoor operated free space optical communication system, solar flux must be competed with within the band detectable by our photodiode. For this reason, we plan to spectrally filter down to a wavelength band of ± 6 nm surrounding our central wavelength of 1550 nm, which will greatly limit the amount of solar irradiance experienced by the photodiode. Within this band, Solar flux is much lower than that seen in the visible, which rewards our choice of 1550 nm with lower ambient background power to

compete with. Moreover, the atmospheric transmission is very high at this wavelength as seen below from MODTRAN in Figure 47.

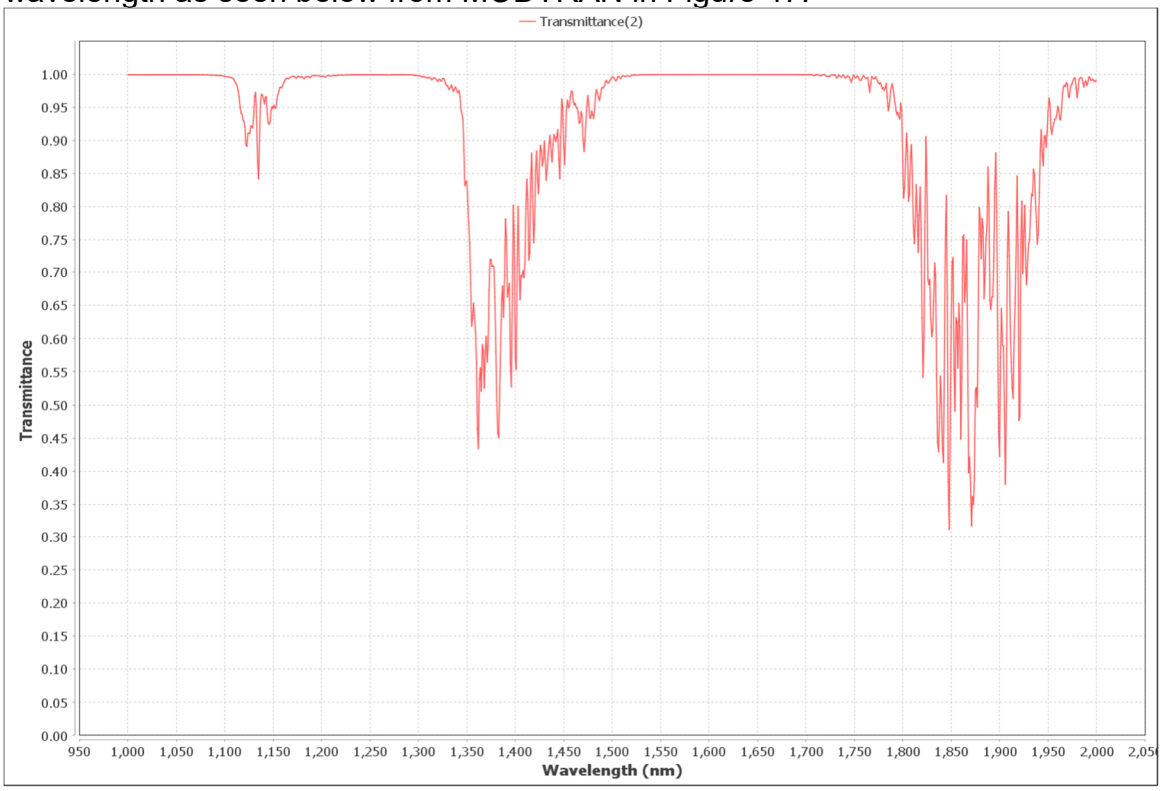



**Figure 58:** Transmittance over a 1km range as a function of wavelength for a Mid-Latitude Summer Atmosphere as modeled in MODTRAN

Based on the data seen in Figure 58, the transmittance in a clear sky scenario analogous to a clear day in Florida, the expected atmospheric transmittance for 1550 nm light is 99.9%. This transmittance value can be used to predict the amount of laser power that reaches the detector as well as the background light witnessed by the detector. First, we can calculate the amount of optical power that we could hope to collect at a 1km range by considering a few factors. In addition to the atmospheric transmittance as a function of distance, we also should consider the transmittance of our lenses, and most importantly the ratio of the amount of irradiance collected by our receiving lens aperture as a ratio of the total irradiance that is spread out by a diverged beam at range. This is given simply by a rearrangement of the conservation of irradiance:

$$I_{lens} = I_{beam} = \frac{P_{detector}}{A_{lens}} = \frac{P_{laser}}{A_{beam}} \Rightarrow P_{detector} = \frac{A_{lens}}{A_{beam}} \cdot P_{laser}$$

$$\frac{\pi(0.0245)^2}{\pi(1)^2} \cdot 20\ mW = \ \sim 12\ \mu W$$

**Equation 19:** Laser power collected from a diverged beam with a cross sectional area of 2 m, not accounting for atmospheric transmission ratio

It should be noted that in the above equation the 49 mm clear aperture (CA) of the lens is used as the basis for calculating its area, not it's full diameter, as that is the measurement, we are more concerned with when estimating the light collecting ability of the lens. While transmission is not accounted, for the clear day conditions which we are assuming as a base scenario for this system's motivational use case, atmospheric transmission is at or above 99.9%, so we assume nearly all of that optical power is focused down to the focal spot at the lens's back focal point.

The transmission coefficient we obtained from MODTRAN can also be used to help estimate the solar flux that we must compete with from the sun with the power of our optical signal. Across the sun's entire emission spectrum, a large amount of unwanted sunlight could enter our lens. This is where spectrally filtering for a thin band centered on 1550 nm comes in via the use of an optical filter. This severely limits the amount of solar flux that makes it to our detector. Luckily for us, within the band we intend to filter for, solar irradiance is comparatively low to in the visible and shorter wavelength IR bands as compared to at or around 1550 nm. Additionally, we can assume that any background solar flux can be defined as irradiance incident on the collecting lens via scattered rays across the sun's broad emission band that are collected by the lenses angular field of view as illustrated below in Figure 59.

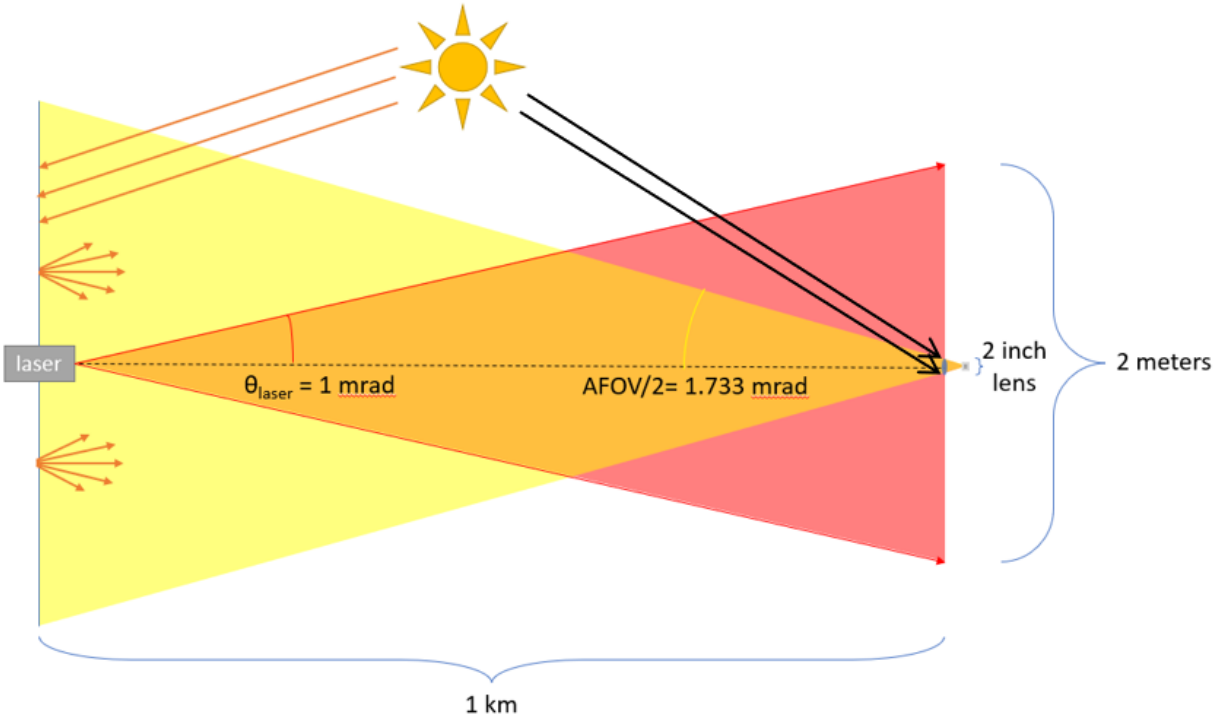


**Figure 59:** The total amount of light from the sun entering the receiver is the sum of the direct sunlight rays and the atmospherically scattered solar flux accepted by the receiver in a cone defined by the solid angle of the detector's angular field of view

Using this model of direct solar flux within the solid angle from the sun to the lens of the collecting aperture, we can integrate Planck's radiation law with respect to wavelength to get the spectral radiance, or in other words irradiance per units of steradians. The product of the spectral radiance and the solid angle created by treating the sun as a point source gives us the solar irradiance experienced by the lens in the direct sunlight scenario. Furthermore, we can set our bounds of integration to the wavelength band which we intend to filter for so that we can instead calculate specifically the irradiance of solar flux that will be experienced by the photodiode.

$$Band\ Radiance = \int_{1544\ nm}^{1556\ nm} \frac{2hc}{\lambda^5} \cdot \frac{1}{e^{\frac{hc}{\lambda k_B T}} - 1}\ d\lambda \left(\frac{W}{m^2 \cdot sr}\right)$$

$$Band\ Radiance = 40085.9\ \frac{W}{m^2 \cdot sr}$$

**Equation 20:** Planck's Radiation Law integrated with respect to spectrally filtered band of receiver

This compares closely to the value that can be found for the sun using a blackbody radiation calculator for the 1544 nm to 1556 nm band. Seen here:

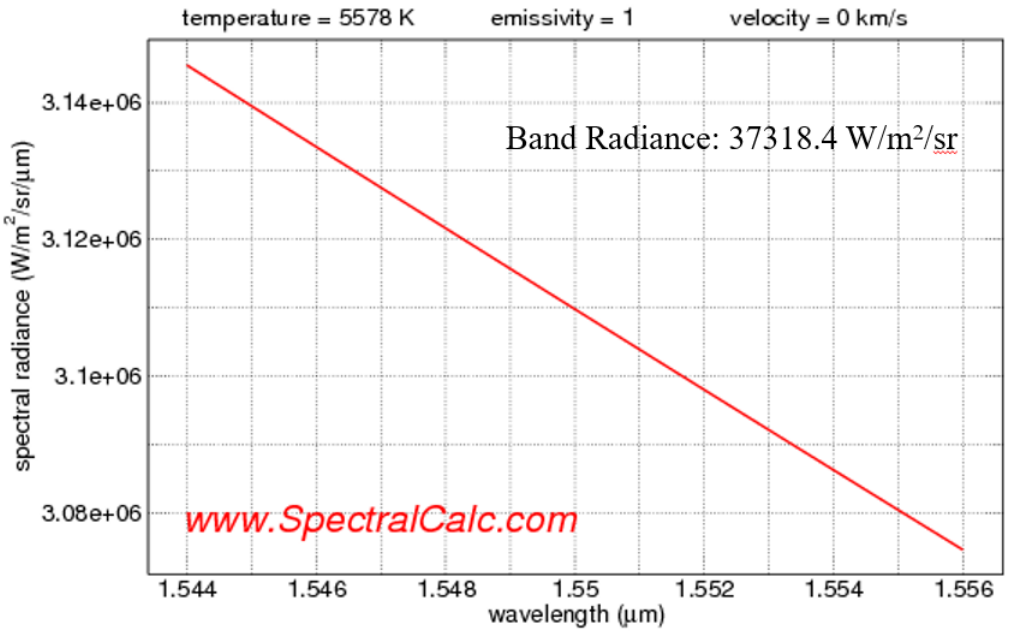


**Figure 60:** Solar flux emitted by the sun in our 12 nm spectral band found by treating the sun as a blackbody source

These values are used in figuring out the spectral irradiance generated by the sun as seen from earth which we can calculate the irradiance we can expect to be seen by our lens over our spectral band due to sunlight. A graph of expected spectral solar irradiance values can be seen below in Figures 60 and 61.

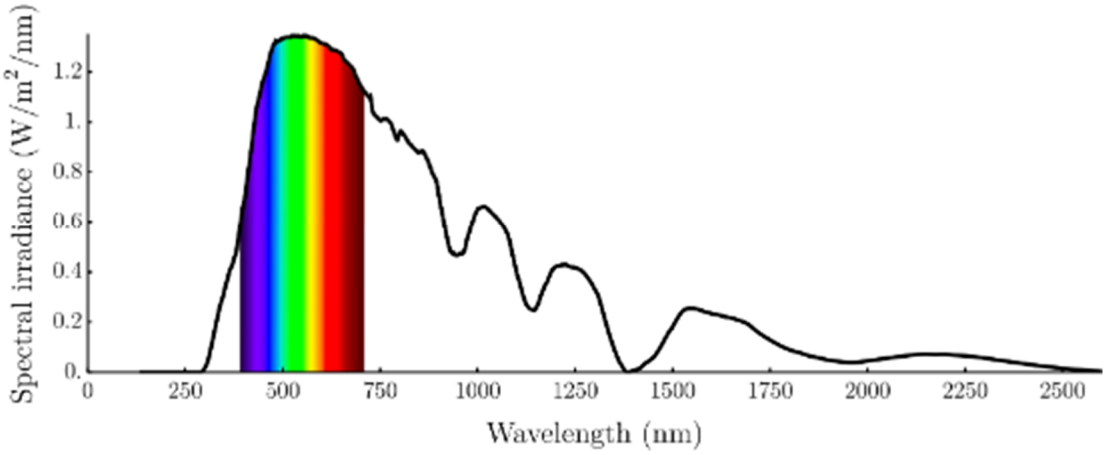



**Figure 61:** Full spectrum irradiance profile of direct sunlight showing the comparative benefit of our wavelength band versus competitive solar flux in the visible and nearer-visible IR (sub 1400) regimes

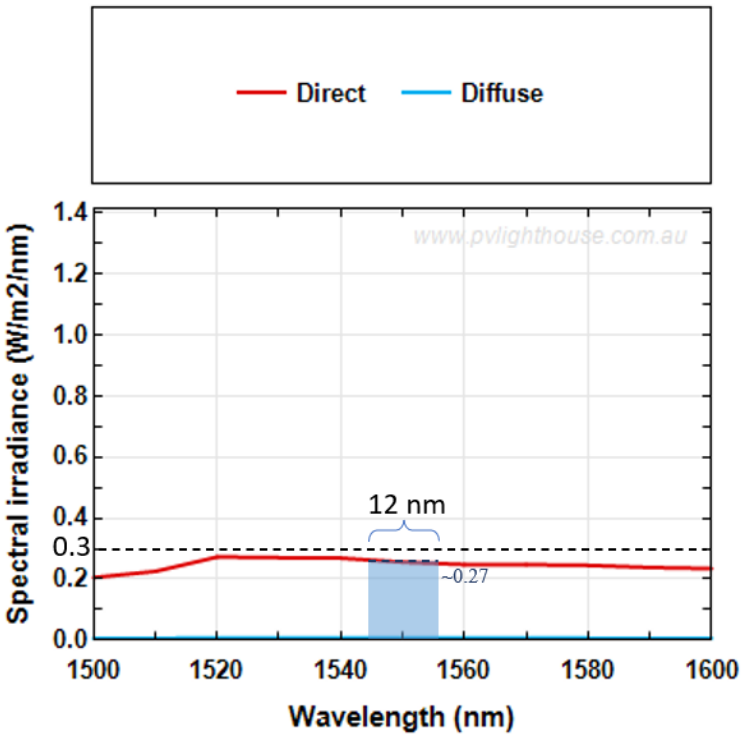



**Figure 62:** Spectral irradiance from 1.5 to 1.6 μm calculated for a clear day in Orlando, Florida via solar spectrum calculator in both the direct sunlight and diffusely scattered skylight cases

Looking more closely at the spectral irradiance within our target band above in Figure 62, we can see that the direct sunlight irradiance is far greater than that from diffuse scattering. From this figure we can assume the average Spectral irradiance within our band to be approximately 0.27 W/m$^2$. By graphically integrating over 1544 nm to 1556 nm we can find the approximate upper limit of direct sunlight irradiance that could be expected to be collected by the receiving aperture and thus the power collected due to direct solar flux:

$$Spectral\ Irradiance = \ 0.27\ \frac{W}{m^2 \cdot nm} \cdot 12\ nm = 3.24\ \frac{W}{m^2}$$

$$P_{Direct} = 3.24\ \frac{W}{m^2} \cdot \pi(0.0245)^2\ m^2 = 0.00611\ W$$

**Equation 21:** Solar Flux predicted to be collected by receiving aperture when collecting direct rays from the sun

Based on the value calculated by Equation 21, the unviability of overcoming direct sunlight exposure with our laser signal becomes clear. The amount of power we expect to receive at a 1km range from our laser is at least a few orders of magnitude lower than the solar flux collected by direct sunlight (~0.0001 W as compared to ~0.006 W). With this in mind, rather than fighting the uphill battle of

how to compete with direct sun rays, we have decided to try to communicate at nominally horizontal angles between the send and receive sides. This requires we design and implement features to optimally block direct rays coming from the sun without blocking direct communication rays around the horizontal. Plans for such controls will be detailed later in the physical system case design.

As seen above in Figure 51, it should be significantly easier to compete with the band irradiance of diffusely scattered rays. While at a glance it looks like an insignificant enough power, because our incident laser power is also low, it is important that we still quantify the solar noise that our laser will have to compete with. Unfortunately, despite best efforts to physically block ray paths from the sun, there will be some approximately on axis ambient skylight scattered through the atmosphere that will be collected by our lens. So, the next question is how does one model the amount and power of diffusely scattered background light along the entire scene seen by the collecting aperture potentially out to infinity. Because of the infinite points in space thinking about every point within the view of the aperture from which scattered rays could originate is not only impractical, but analytically impossible. Luckily, there do exist close approximations that simplify thinking about this problem.

In filtering for our ~12 nm band centered on 1550 nm, we must introduce an optical filter that comes with it, its own transmission coefficient, which at minimum for 1550 nm is 85%. To be conservative, we will assume that 15% of light is always lost due to this transmission ratio when doing calculations. This leaves us with ~ 10.2 μW of optical power from the laser reaching our photodiode.
We originally intended to use the atmospheric scattering equation to roughly model how much total power is reaching our detector as well as the ambient background that must be overcome by our signal. If we assume that 99.9% of light is transmitted as we propagate, we can also assume that 99.9% of rays from the sun within this band continue their path towards the ground, or in other words, are not scattered. This allows us to only concern ourselves with that remaining 0.1% of solar flux that we can consider as diffusely scattered skylight that may be incident on our collecting aperture. This scattered light as a function of solar transmission is accounted for in the following atmospheric scattering equation:

$$P_{detector} = t_{atm} t_{filter} P_{laser} + (1 - t_{atm}) t_{filter} P_{sun}$$

$$P_{detector} = t_{atm} t_{filter} P_{laser} + (1 - t_{atm}) t_{filter} I_{sun} A_{lens}$$

$$P_{detector} = 0.999 \cdot 0.85 \cdot 12\ \mu W + (1 - 0.999) \cdot 0.85 \cdot\ 3.24 \frac{W}{m^2} \cdot \pi (0.0245)^2\ m^2$$

$$P_{detector} = 10.19\ \mu W +\ 5.19\ \mu W = 15.99\ \mu W$$

**Equation 22:** Rough incomplete model of ambient skylight using the atmospheric scattering equation assuming 99.9% transmission of light near λ = 1550 nm

This still yields a very unfavorable optical signal to noise ratio (OSNR), however this model is very rough and suffers from a critical flaw: all light that does not follow its ray path to the ground is assumed to be scattered directly into the collecting aperture. To our benefit, scattering occurs in all directions, so still only a fraction of this solar flux makes it to our sensor.

We can more correctly model the light scattered within the sensor's field of view as light coming from the sun, hitting a diffuse surface, and scattering in all directions. This is still complicated to think about, as there are rays from each spot on the surface that will not make it into the acceptance cone of the collecting lens. The problem can further be reduced by concentrating the sum of scattered ambient solar rays as coming from a single on axis point on the surface. We assume that for our diffusely reflective surface, scattered rays originating from it follow an ideal three-dimensional Lambertian reflectance profile whose peak irradiance is normal to the surface. For convenience when thinking about the problem, we will have this diffuse surface subtend the solid angle of the sensor at a familiar distance: the location of the laser transmitter source. The two-dimensional projection of this scenario can be seen illustrated below.

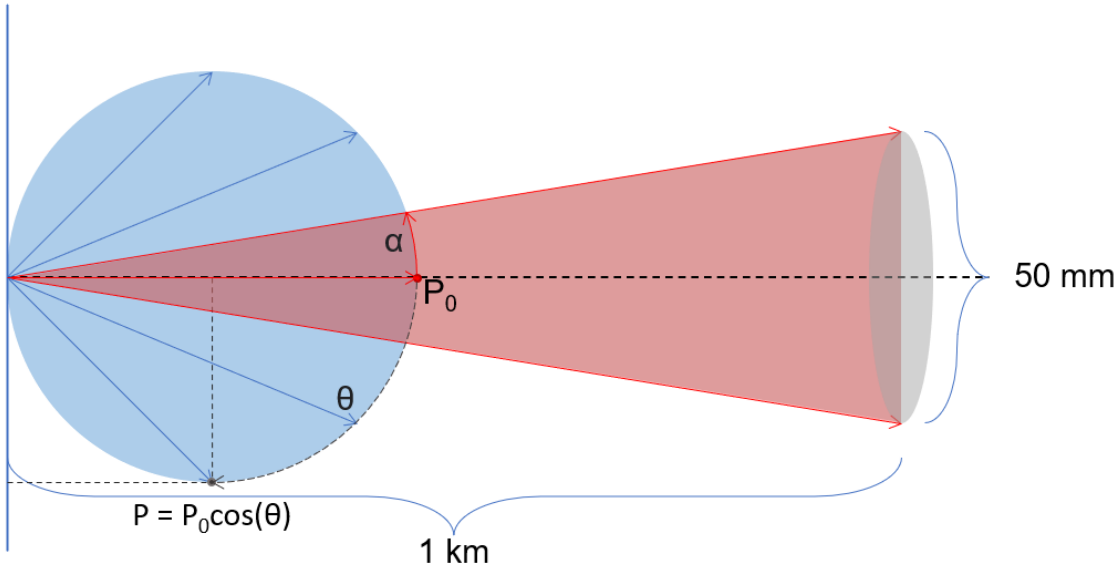



**Figure 63:** Two-dimensional view of Lambertian reflection of scattered sunlight coming from a diffuse surface at range

In two dimensions, this problem is simply a function of the angle, α, defined by the direction of the marginal (outermost) ray to the edge of the aperture with respect to the optical axis. Extending this problem into three dimensions demands we additionally consider the solid angle created by the source that makes it into the lens in comparison to the solid angle of the entire hemisphere coming off the surface which has a value of $2\pi$ Steradians. The coefficient that defines the ratio

of collected scattered light versus total scattered light can be thought of as an optical efficiency, $\eta_{opt}$, and is given by integration as described by:

$$\eta_{opt} = \frac{\int_0^{\alpha}\int_0^{2\pi} g(\theta,\phi)\sin(\theta)\mathrm{d}\phi\mathrm{d}\theta}{\int_0^{\pi/2}\int_0^{2\pi} g(\theta,\phi)\sin(\theta)\mathrm{d}\phi\mathrm{d}\theta}$$

**Equation 23:** $\eta_{opt}$ for a given Lambertian reflected cone as a function of θ and the solid angle ϕ as derived by Nabavi et al. where g(θ, ϕ) is the radiant intensity of the source in W/sr. [16]

This three-dimensional perspective is analogous to the azimuth-elevation angle notation seen commonly when dealing with celestial bodies, where θ is our effective elevation angle and ϕ is our azimuth (axial rotation) angle. The work referenced above in Equation 23 goes on to explain that for a rotationally symmetric Lambertian source (such as our model for diffusely reflected skylight), the equation is Equation 23 reduces to:

$$\eta_{opt} = P_0 \sin^2(\alpha)$$

**Equation 24**: Reduction of Lambertian reflected ambient solar flux model
Now finally with the above equation we can use the previously found irradiance from the direct sunlight case of 3.24 W/m$^2$ as our $I_0$ value corresponding to the irradiance responsible for $P_0$ to more correctly predict the irradiance seen by the receiving aperture as a result of ambient skylight.

$$P_{ambient} = I_0 \cdot A_{Lens} \cdot \eta_{opt} = I_0 \cdot A_{Lens} \cdot \sin^2(\alpha)$$

$$\alpha = \tan^{-1}\left(\frac{0.0245\ m}{1000\ m}\right) = 0.024\ mrad$$

$$\eta_{opt} = \sin^2(0.024\ mrad) = 6.0025 \times 10^{-10}$$

$$P_{ambient} = 3.24\ \frac{W}{m^2} \cdot \pi(0.0245)^2\ m^2 \cdot 6.0025 \times 10^{-10} = 3.667\ pW$$

**Equation 25:** Accurate calculation of the ambient solar flux collected by our receiving aperture

From this point we can proceed to establishing how much current would be produced by our photodiode that must be overcome by the laser given the current produced by ambient optical power in addition to the dark current. The typical responsivity of our photodiode at 1550 nm is 0.95 A/W. The typical dark current for our chosen photodiode is 0.5 nA, but in an attempt to be conservative on calculations, we will use the stated maximum dark current of 3 nA. With these photodiode parameters in mind, we can calculate the total current produced due to laser light in addition to the current that that laser light must overcome.

$$I_{laser,max} = 10.19\ \mu W \cdot 0.95 \frac{A}{W} = 9.6805\ \mu A$$
$$I_{noise} = 3.667\ pW \cdot 0.85 \cdot 0.95 \frac{A}{W} + 3\ nA = 3.00296\ \mu A$$

**Equation 26:** Current produced by photodiode responsivity

We can see that after more carefully considering the scattered background light and estimating the current generated by the photodiode, that the total electrical noise is comparatively small to our expected signal noise, even at a link range of 1 km.

# 5.2 Initial Electrical Design

The following circuit will be the TEC power supply, the required voltage will be outputted from the power PCB and then to the TEC control circuit. This will be comprised of a small size comparator that will then signal to a voltage-controlled transistor that will allow current to be supplied to the transistor to maintain optimal operating temperature.

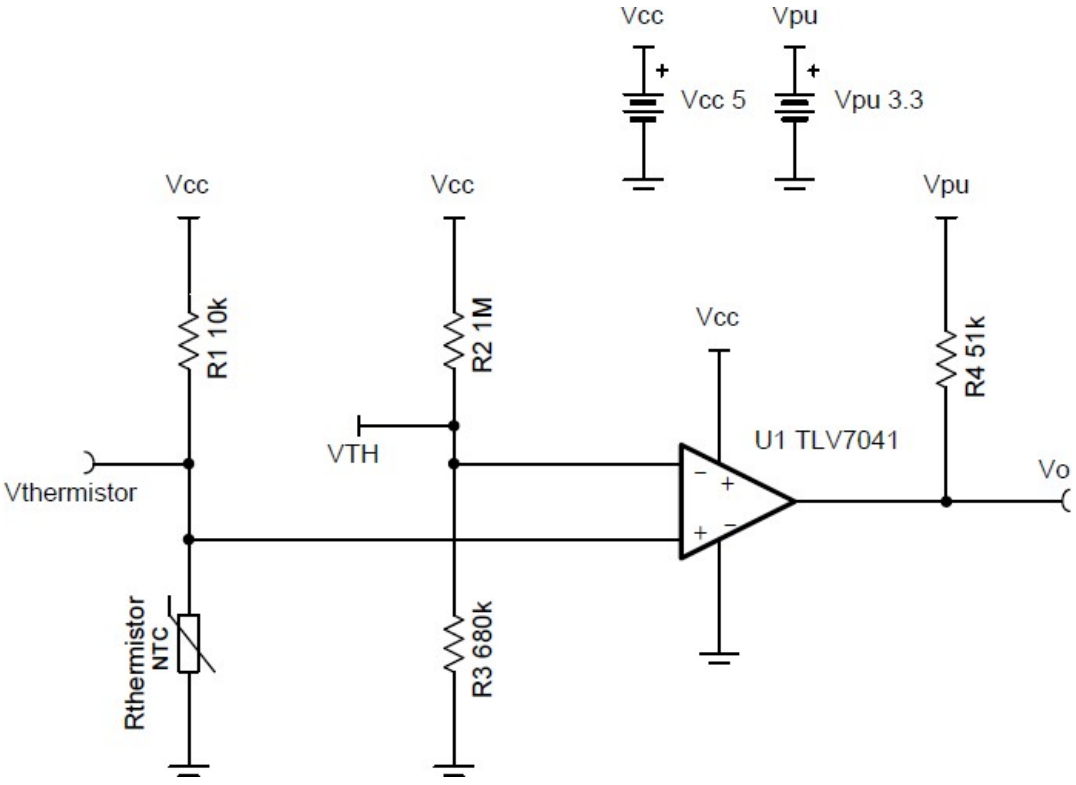



**Figure 64:** TEC Thermal Regulation Control Circuit

The next circuit will then be the supply power to the laser modulation circuit, that contains a high switching frequency transistor. The signal voltage from the serializer will be utilized as the voltage control, with high voltage being a 1-bit and the low voltage will be a 0-bit. These high and low voltages will act as the transistor switch and as the high voltage signal is sensed it will allow the full current to go to the laser. The laser will modulate slower if it is completely off so a constant low current supply will be configured as a bypass to this control circuit to keep the laser on a low power mode. The final power circuit will supply the operating voltage for the photodetector. This is required so that when the laser is on, the output current of the receptor diode will be easier to read as an analog signal. This signal then will go to an analog to digital converter then the de-serializer, then the microcontroller.

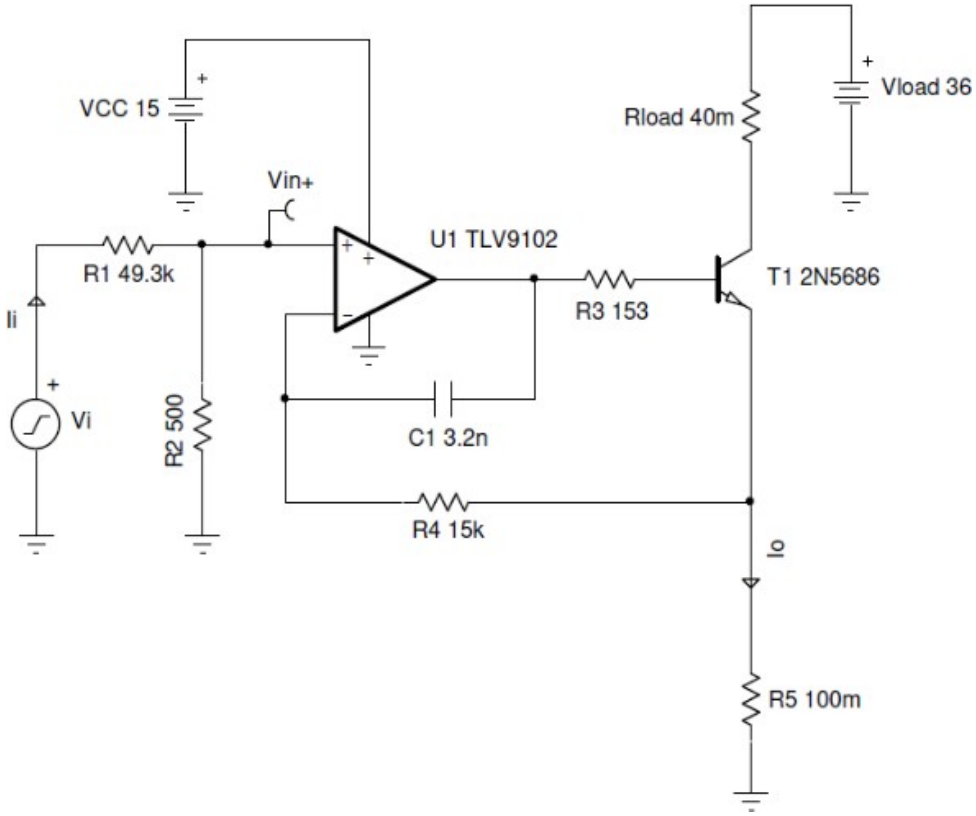



**Figure 65:** Laser Modulation Control Circuit

Under further investigation the proposed laser modulation circuit above will not be sufficient. Due to the nature of our project requiring high switching speeds I could not find any transistors that would switch fast enough at 1GHz.

# 5.3 Electrical Design

The following section is the final electrical designs. Through trial and error and going more in depth to the functionality of the systems we have encountered some issues. As for the laser current modulation circuit that was, there were no transistors available with sufficient modulating speeds. The team is waiting for a response from the laser vendor to further understand what is required in making a functional system.

This section will also show our final control circuits to each component. Such as the laser current modulation, TEC control, as well as the photodetector transimpedance amplification circuit.

## 5.3.1 Electrical Final Power Supply Constraints

The following section will also show the final designs for the power supply circuits, what components were selected, why they were selected, and circuit information. We also show preliminary PCB designs in this section. In the table below you will find the component at the top row, and various data about each component on the left. This table outlines each of the power supply circuits and the load of each system.

**Table 12:** Power Components Information

| | **Microcontroller** | **Laser** | **TEC** | **Photodetector** |
|---|---|---|---|---|
| Part Manufacturer | Intel | OptiLab | OptiLab | ThorLabs |
| Part Number | Cyclone IV FPGA | DFB-1550-DM-4 | Integrated to laser | FGA015 |
| DC/DC Buck Converter Part Manufacturer | Texas Instruments | Texas Instruments | Texas Instruments | Texas Instruments |
| DC/DC Buck Converter Part Number | tps54332 | lm43600 | tps54332 | lm43600 |
| Buck Converter Voltage Input | Vin MAX = 24.5V Vin MIN = 16.0V | Vin MAX = 24.5V Vin MIN = 16.0V | Vin MAX = 24.5V Vin MIN = 16.0V | Vin MAX = 24.5V Vin MIN = 16.0V |
| Buck Converter Output | Vout = 5V Iout = 3.5A | Vout = 1.5V Iout = 0.2A | Vout = 2.5V Iout = 1.4A | Vout = 1V Iout = 0.5nA |
| Load (Watts) | Pout = 17.5W | Pout = 0.3W | Pout = 3.5W | Pout = 0.5nW |

### 5.3.1.1 Final PCB Design

In the following section the final PCB images will be shown and I will give an explanation in detail on how each system will operate. Desigin the PCB was a challenge as it was a big increase in knowledge to gain from junior design. In order to properly design the PCB I downloaded Fusion 360 from Autodesk to obtain the ability to design multiple circuits on one board. Fusion 360 is an excellent product with the ability to integrate parts for three-dimensional design. This will also be used to design the final housing of the equipment into a 3D printed box.

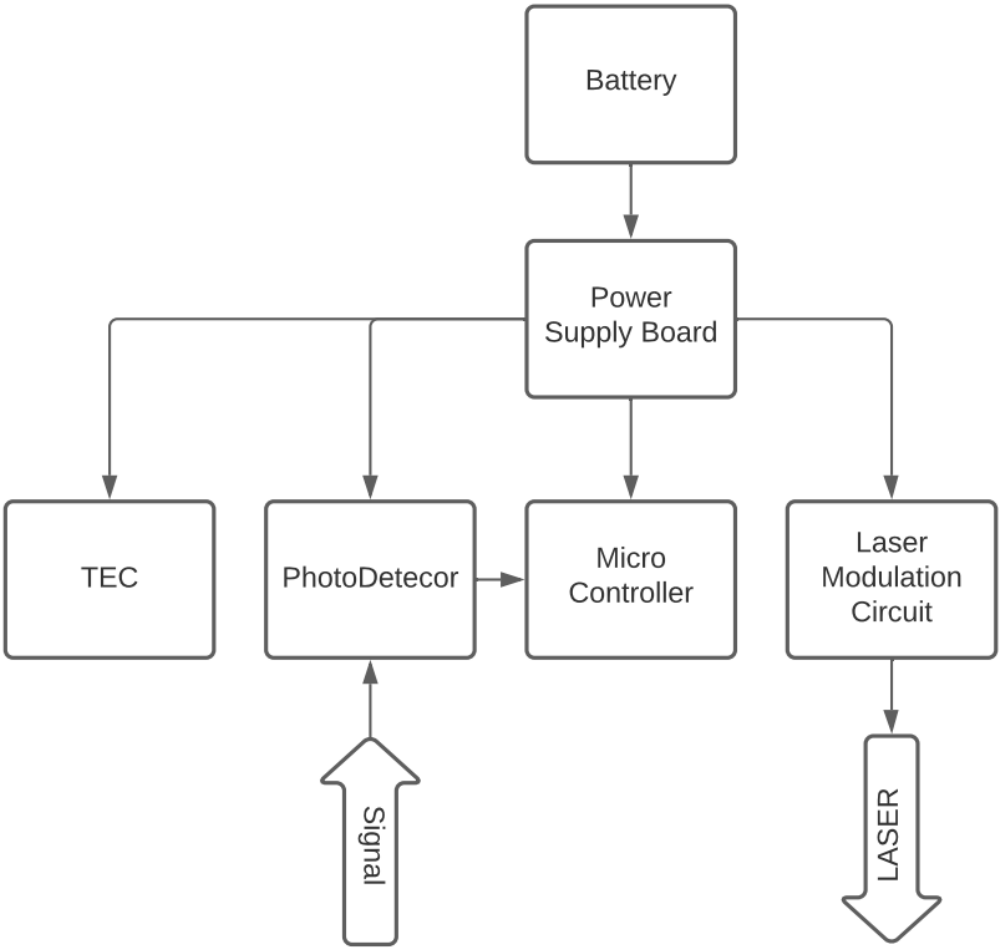



**Figure 66:** Block Diagram

To begin creating my PCB I started off with a simple block diagram for overall functionality of the system. Each block represented a stand-alone system that needed to be connected to each other. Each arrow is representation of wires. I did this to keep track of keeping the systems that I can combine into one board and the systems I am forced to separate into separate boards. The battery will supply

power to the PCB I create to supply each component correct voltage and current requirements.

In the image below you will see the PCB wiring view. I combined all of the power supply circuits excluding the photo detector module circuit. In the circuits below you will the addition of pins to be able to interface with the board. I selected screw pins as they are the most reliable. The large R1 at the top is the variable resistor for the TEC control. The JP1 next to the variable resistor is for the connection the thermistor resistor from the TEC itself. This will be used to regulate temperature explained further in a following section.

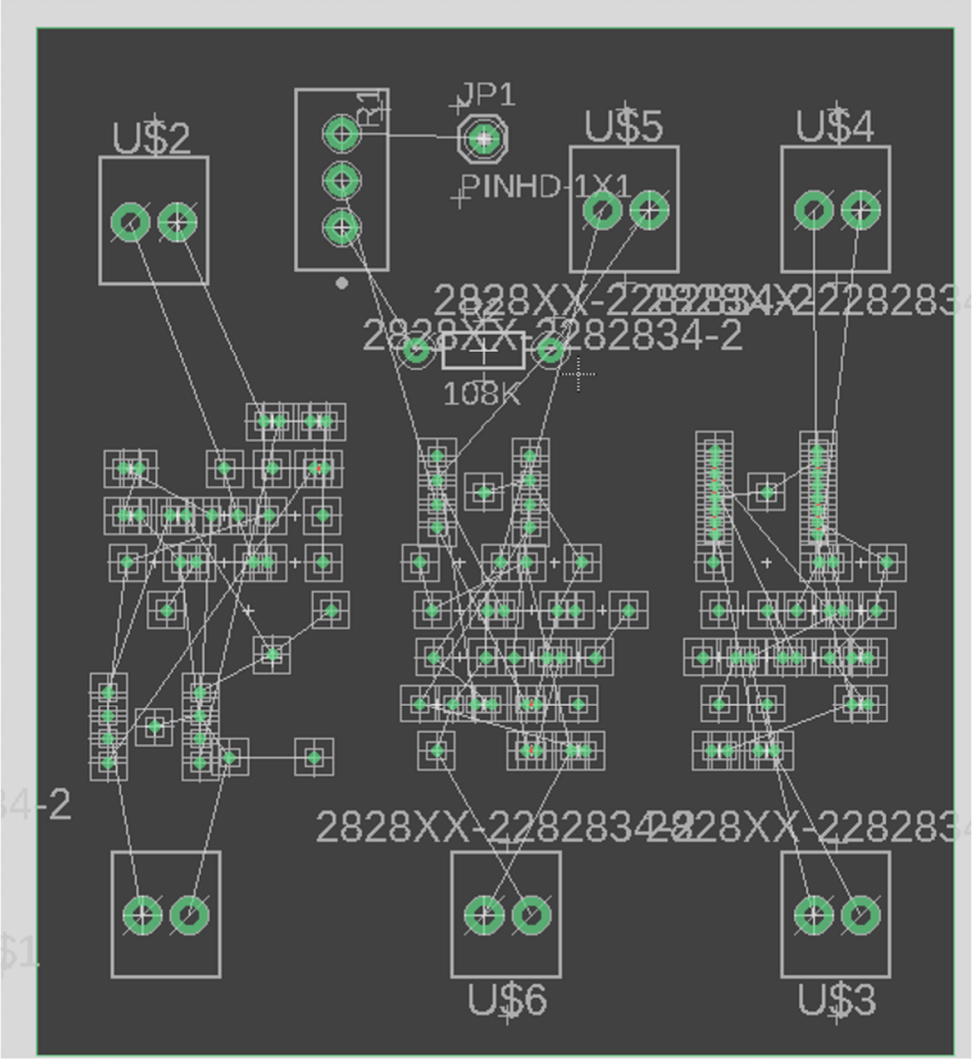



**Figure 67:** PCB Schematic View

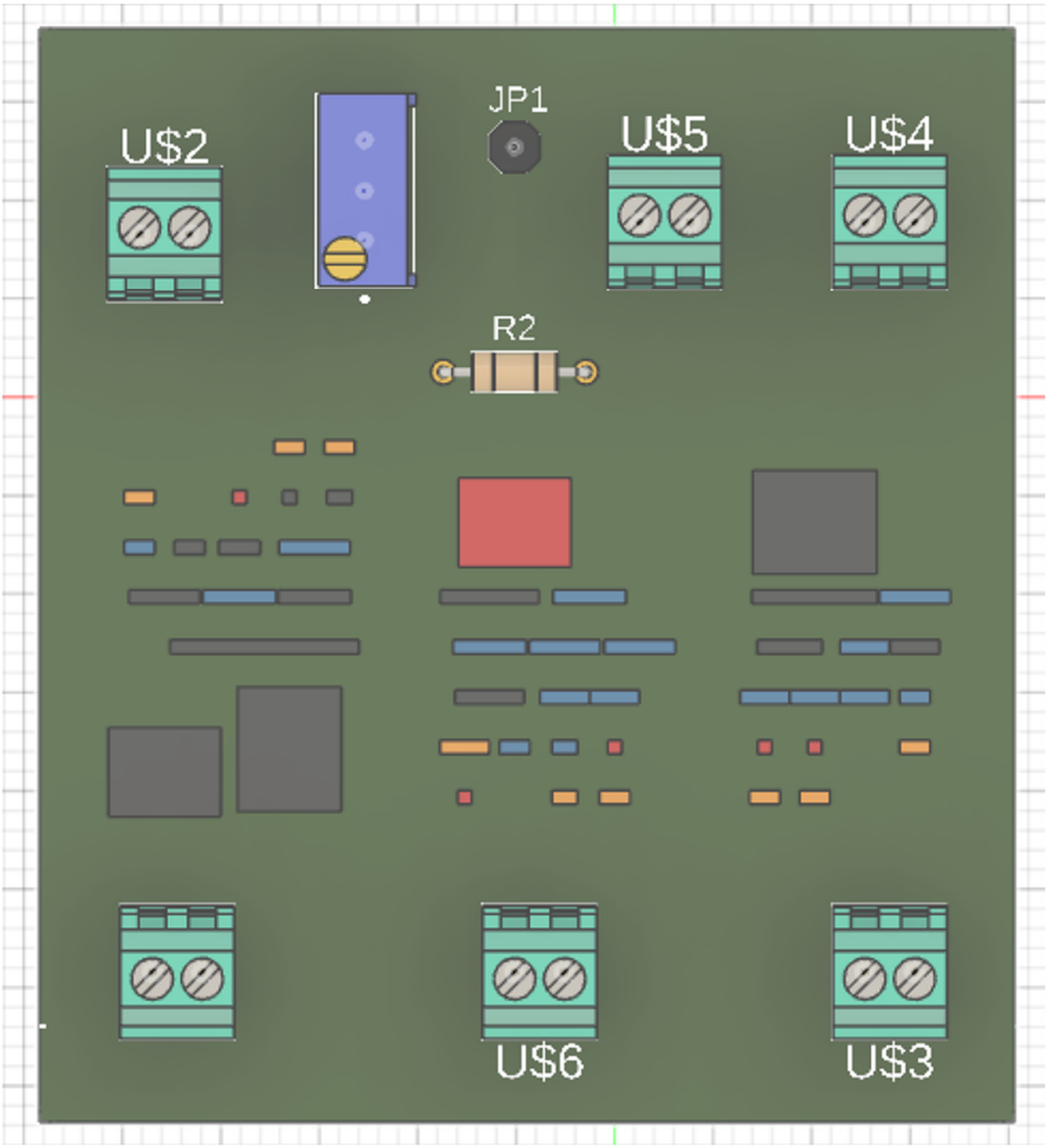



**Figure 68:** PCB Plan View

In the view above it shows a three-dimensional representation of what the board will look like. As mentioned before the pin connections can be seen clearly here and will be used for interfacing with the board.

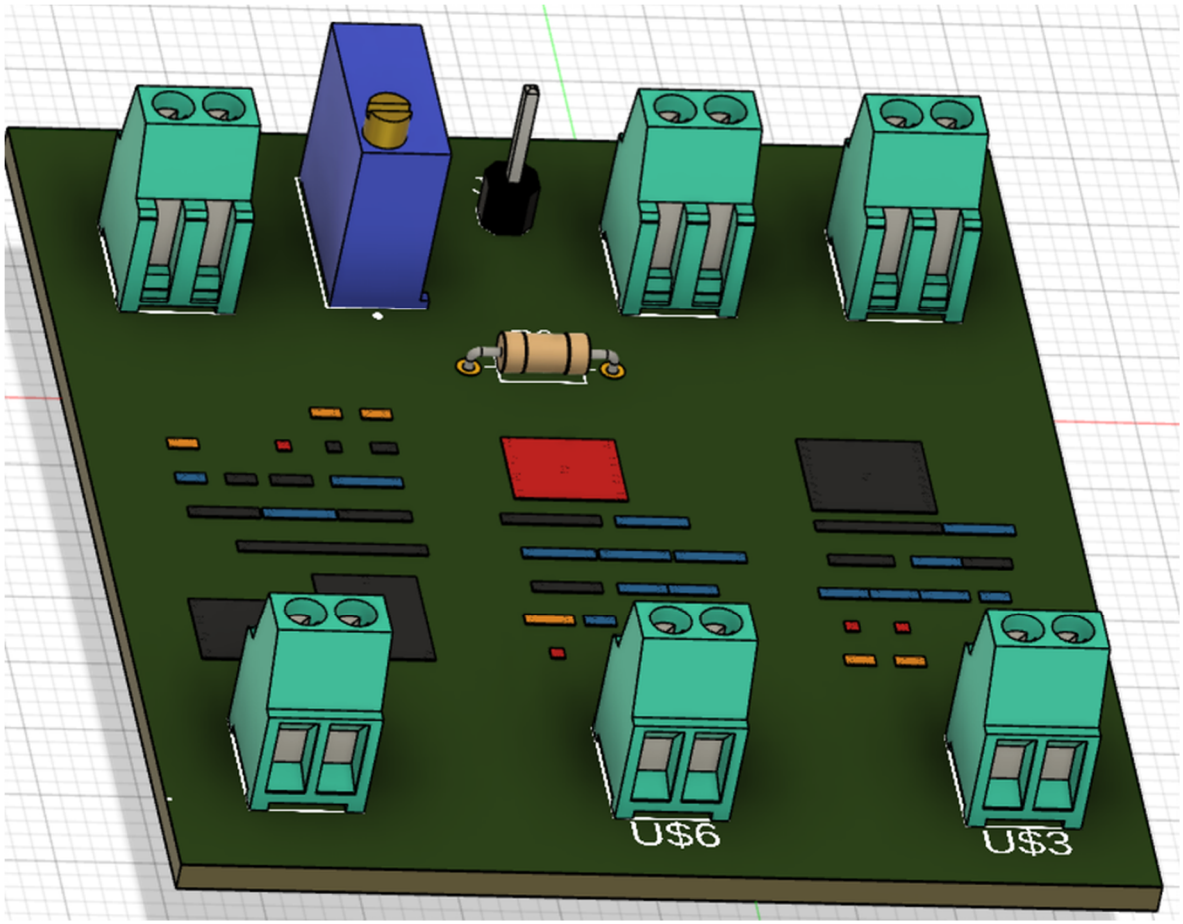



**Figure 69:** PCB Three-Dimensional View

In the view above it shows a three-dimensional representation of what the board will look like. This view gives a better representation of what the board will physically look like. The design of this board was with the intent of being able to package it into a 3D printed housing. This is a prototype and will need to be refined in a final iteration for better space management. The pins will be converted into a plug style connection in hopes of a more user-friendly system. The bare pin standing between the variable resistor will be for the thermistor connection and will be used to control the power module for the TEC. Fusion 360 was instrumental in being able to design a board of this nature.

# 5.3.1.2 Final Laser Power Supply Design

In the following section we will discuss the power circuit to the laser directly, this will be a current modulation circuit. This circuit will be a combination from the laser power circuit and an output from the microcontroller and serializer. The laser has 14 pins as seen in the following image and description in the table.

| | | | |
|---|---|---|---|
| **1** | Thermistor | **8** | Case Ground |
| **2** | Thermistor | **9** | Case Ground |
| **3** | Laser DC Bias (-) | **10** | Not Connected |
| **4** | Monitor Anode | **11** | Laser Ground |
| **5** | Monitor Cathode | **12** | Laser Modulation (-) |
| **6** | TEC (+) | **13** | Case Ground |
| **7** | TEC (-) | **14** | Not Connected |

**Table 13:** Laser PINs

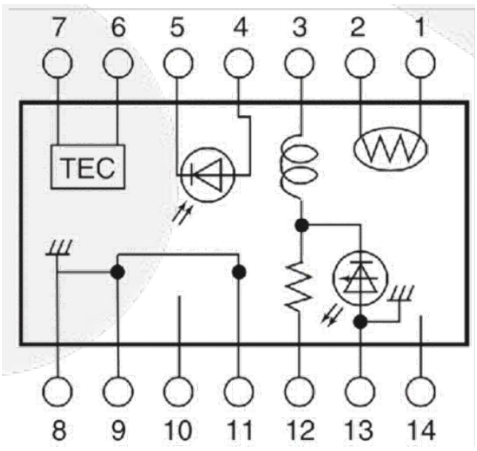



**Figure 70:** Laser PINs

For the laser power supply the power circuit from the PCB will be connected to pins 3 and the laser ground. Then the data signal from the serializer will be connected to the laser modulation pin 12. This output from the serializer will need to be tested in conjunction with the laser power circuit for me to finish this circuit. The end circuit will be the data signal with some combination of resistors and diodes so that when the data signal reads high, the voltage at pin 12 will be a low voltage allowing a higher opposing voltage from the supply to operate the laser at a high out put power. For a low signal or '0' bit the circuit will allow a higher threshold voltage through to create an opposing voltage at the pin 12 to allow a smaller voltage from the power supply through the laser diode. Unfortunately shipping lead times with the laser have forced us not to be able to do any sufficient testing of these components.

# 5.3.2 Electrical Final TEC Control Circuits

In this section the TEC control circuit will be described in depth. The TPS54331DDAR has a switch pin labeled as EN. This switch pin will be utilized in combination with the TEC thermistor. The thermistor operating ranges are in the below table.

**Table 14:** TEC Parameters

| | TEC Current | TEC Voltage | Cooler Power | TEC Resistance | Thermistor Resistance | Thermistor B Constant | Operating Temperature |
|---|---|---|---|---|---|---|---|
| Min. | 0A | 0V | 0W | 2.0 Ohms | 7.7k Ohms | 3270K | 10°C |
| Max | 1.0A | 2.4V | 2.4W | 3.2 Ohms | 12.6k Ohms | 3630K | 40°C |
| Typical | N/A | N/A | N/A | 2.4 Ohms | N/A | 3450K | N/A |

These values are the design constraints for the control circuit design. The main values considered were the thermistor min and max resistances. These are the values of the resistance that the thermistor will read at the described operating temperatures. The potentiometer seen in figure 71 below will give us control of the TEC temperature by adjusting the resistance therefore adjusting the input voltage to the EN pin. These are the equations used to calculate the range in the potentiometer resistances required. Ren1 is the resistor value that is used to calculate the adjustable input parameter for the potentiometer. Ren2 will be the min and max resistances of the thermistor. Vstart is the input voltage from the battery at 24V. Ven is the enable voltage of 1.25V, Vstop should always be greater than 3.5V so I solved using that value. This voltage is dependent of Ren1 so the potentiometer will be able to account for adjusting the circuit to optimal TEC temperature.

$$\boldsymbol{Ren1} = \frac{\mathbf{Vstart} - \mathbf{Vstop}}{\mathbf{3\mu A}}$$

$$\boldsymbol{Ren2} = \frac{\boldsymbol{Ven}}{\frac{\boldsymbol{Vstart} - \boldsymbol{Ven}}{\boldsymbol{Ren1}} + \mathbf{1\mu A}}$$

**Equation 27:** Ren1 and Ren 2 Equations

Using the above equations, we can rearrange to solve for Ren1. Which will give us the following equation, we can use this by inserting the min and max resistances of Ren2, the thermistor resistance.

$$\boldsymbol{Ren1} = \frac{\boldsymbol{Vstart} - \boldsymbol{Vstop}}{\frac{\boldsymbol{Ven}}{\boldsymbol{Ren2}} - \mathbf{1\mu A}}$$

$$\boldsymbol{Ren1(min)} = \frac{\mathbf{24V - 3.5V}}{\frac{\mathbf{1.25V}}{\mathbf{7.7k\Omega}} - \mathbf{1\mu A}} = \mathbf{127k\Omega}$$

$$\boldsymbol{Ren1(max)} = \frac{\mathbf{24V - 3.5V}}{\frac{\mathbf{1.25V}}{\mathbf{12.6k\Omega}} - \mathbf{1\mu A}} = \mathbf{208k\Omega}$$

$$\boldsymbol{Ren1(delta)} = \mathbf{208k\Omega - 127k\Omega = 81k\Omega}$$

$$\boldsymbol{Resistor\ in\ Series\ with\ 100k\Omega\ potentiometer} = \mathbf{208k\Omega - 100k\Omega = 108k\Omega}$$

**Equation 28:** Solving for potentiometer ranges and series resistor

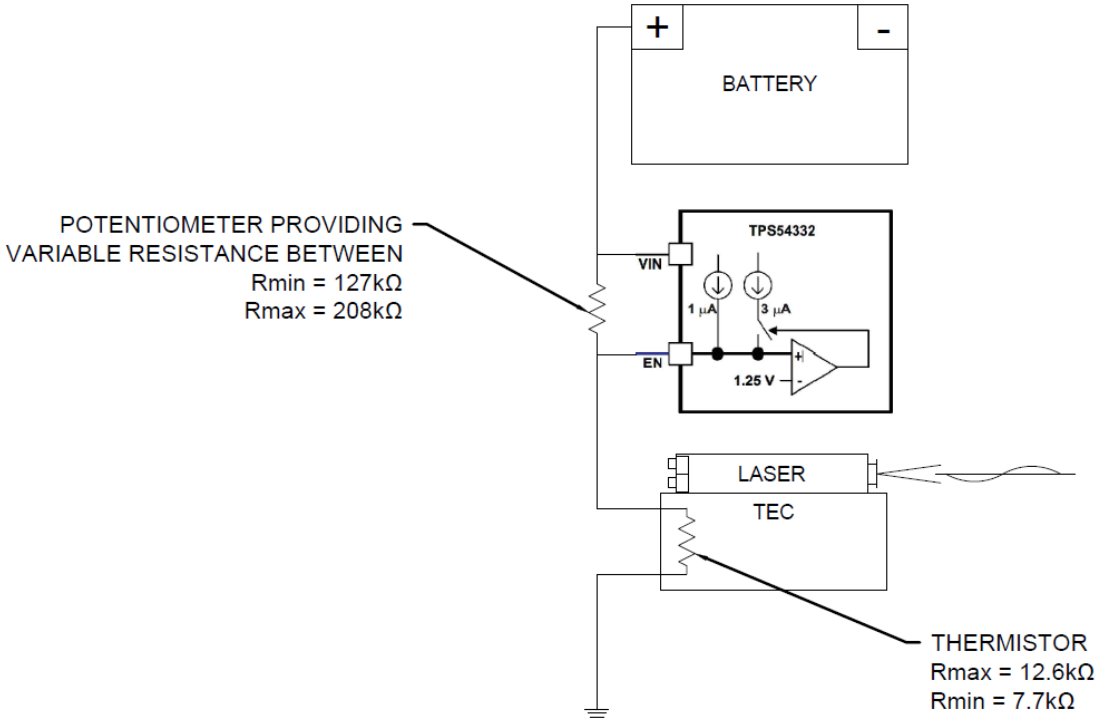



**Figure 71:** TEC control portion Diagram

# 5.3.3 Electrical Final Photodetector OP-Amp

In this section we will discuss the photoreactor circuit shown on the next page. The main components in the center are for the reference voltage provided, the op amp on the left side of the circuit will be connected to the photodetector and supplemental circuit components previously mentioned. The output pins will be connected to the serializer PCB and will take the data from the detector and input into the micro controller. This is the main optical link components other than the laser and will require more testing for optimal components for filtering noise. The filter will be a critical component to avoid data corruption and miscellaneous bits being inputted. For the Op-Amp to function properly the output voltage will need to match the input voltage of the serializer, the input of the serializer reads above and below 1V thresholds. Above 1V being a ‘1’ or a high bit, and below 1V being a ‘0’ or a low bit. This configuration of the op-amp and the serializer will be critical in being able to get our desired speeds of 1Gbps.

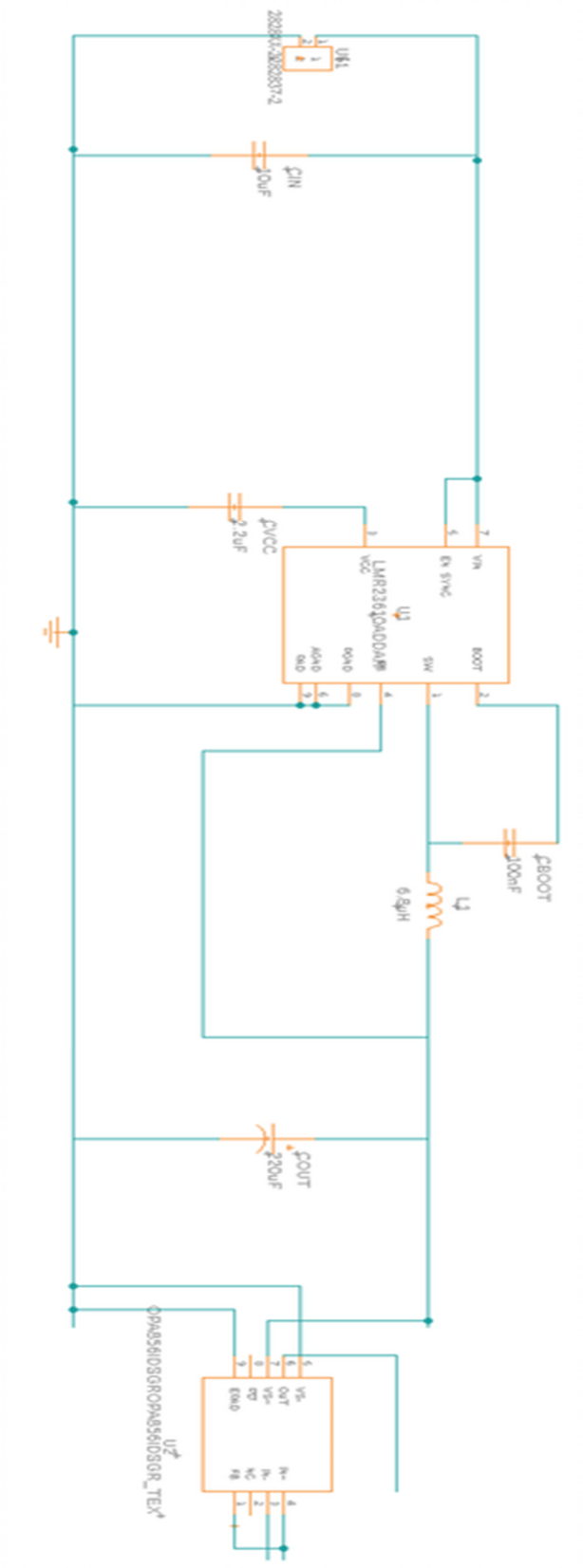


**Figure 72:** TEC control portion Diagram

# 5.3.4 Electrical Load Calculations

In this following section we will look at the electrical load parameters of the system. This is important to know the load on the proposed system for a drone mount application. With a drone mount application this load is considered a parasitic load to the overall function of flying. Therefore it is critical to keep the components as efficient as possible. To calculate the system life time, I combined all the loads in watts as it is a common ground where voltage does not affect the final outcome. The total load came out to be 21.31W at 24V. With a battery life of 14000mAh we can take our total load and divide that value and we will get our theoretical run time on a single charge.

**Table 15:** Electrical Load Calcs

| Load | Voltage | Amps | Watts |
|---|---|---|---|
| Microcontroller | 5V | 3.5A | 17.5W |
| Laser | 1.5V | 200mA | 300mW |
| TEC | 2.5V | 1.4A | 3.5W |
| Photodetector | 1V | 10mA | .01W |
| Battery Information | | | |
| Total Load at Battery | 24V | 888mA | 21.31W |
| | | | |
| | Supply Voltage | Overall Life | System Life |
| Life of Battery | 24V | 14000mAh | 15.765 Hours |

# 5.4 Initial Computer Design

The following sections describe the computer subsystem of the S.T.E.A.L.T.H. project. The functionality of the serializer and de-serializer are described, as well as the initial designs that were considered.

# 5.4.1 DS92LV16 Functionality

The serializer and de-serializer are two very important components for the S.T.E.A.L.T.H. system. With these two components, the team will be able to translate 16 bits of data coming from 16 parallel pins of the controller into a differential serial stream and to be sent to the laser. The laser will transmit the serial stream of data to the photodetector over free space. The photodetector then sends the stream to the de-serializer to translate it back to 16-bit parallel LVCMOS data. For this reason, the DS92LV16 functionality was studied to completely understand how to implement this component into the design. The following

sections are a breakdown of how the DS92LV16 works, with important characteristics described, as well as the operating states of the component.

# 5.4.1.1 Characteristics of the DS92LV16

The following table shows the electrical and timing characteristics of the DS92LV16 that are important for the design of the system. The understanding of these characteristics will deepen the understanding the team has when it is time to program the DS92LV16 and lead to better results.

**Table 16**: Electrical and Timing Characteristics of the DS92LV16

| Parameter | Pins | Ratings (Nominal) | Units |
|---|---|---|---|
| Supply Voltage ($V_{CC}$) | | 3.3 | V |
| Clock Rate | | 25-80 | MHz |
| **LVCMOS Specifications for Serializer** | | | |
| High Level Input Voltage | TCLK, DIN, RCLK, REFCLK, SYNC | 2.0 – $V_{CC}$ | V |
| Low Level Input Voltage | | GND – 0.8 | V |
| High Level Output Voltage | $R_{OUT}$, RCLK, LOCK | 3.0 | V |
| Low Level Output Voltage | | 0.33 | V |
| Transmit Clock Period | TCLK | $T^1$ | ns |
| TCLK Low-to-High Time | | 0.2 | ns |
| TCLK High-to-Low Time | | | ns |
| TCLK Input Jitter | | 80 | ps |
| **Bus LVDS Specifications for De-serializer** | | | |
| Common-Mode Voltage ($V_{CM}$) | RI +/- | 1.1 | V |
| Differential Threshold High Voltage | | +0.1 | V |
| Differential Threshold Low Voltage | | -0.1 | V |
| Differential Output Voltage (DO+) – (DO-) | DO +/- | 0.5 | V |
| REFCLK Period | REFCLK | $T^1$ | ns |
| REFCLK Transition Time | | 6 | ns |
| REFCLK to TCLK Ratio | TCLK, REFCLK | 0.95 – 1.05 | |

[1] T signifies the desired input clock source. For example, if the input frequency of TCLK is 50 MHz, T is 2 ns.

Table 16 shows the electrical and timing characteristics that the team believed to be important to focus on. The DS92LV16 circuit accepts a supply voltage of 3.3 V. The voltages at the serializer's data input pins and de-serializer's output pins are therefore voltage signals between 0 and 3.0 V, nominally.

The timing characteristics are more interesting and more critical to the overall design. Figure 55 shows the serializer output pins (DO +/-) attached to the recommended load, as well as the output waveform with ideal transition times. Similarly, Figure 56 shows the de-serializer output pins (ROUT[0:15]) with loads and ideal transition times.

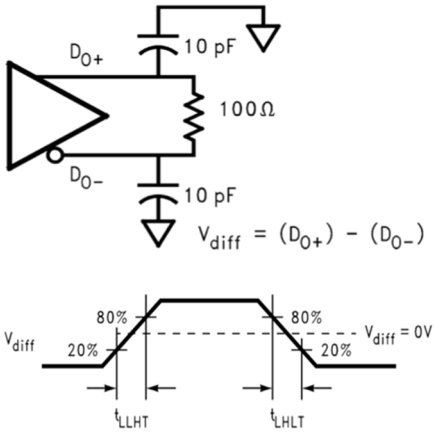



**Figure 73:** Serializer Output Load and Transition Times

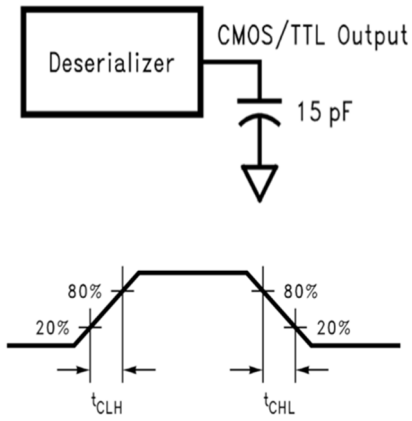



**Figure 74:** De-serializer Output Load and Transition Times

The low-to-high transition time of the serializer ($t_{LLHT}$) is measured between 20 and 80% of the transition. This transition time should ideally be 0.2 ns, and 0.4 ns at maximum to ensure proper functionality. The voltage difference ($v_{diff}$) between DO+ and DO- is 0V as the output transitions from low to high. Ideally, output voltages have a difference of 500 mV, at low and high levels. The same functionality applies at high-to-low transition times ($t_{LHLT}$). The two differential voltages should have a load resistance of 100Ω to ensure proper functionality.

The same functionality applies to the de-serializer output transition times, shown in Figure 56. These signals, however, are LVCMOS standards, so no differential calculations are required. It is important that the team pays attention to these transition times, as they directly affect how fast data will be transmitted in the S.T.E.A.L.T.H. system.

The common mode voltage of the de-serializer input is the voltage at 50% transition times. This voltage is 1.1 V, as listed in Table 16. The de-serializer reads

logical high when the voltage level at RIN is at 1.2 V, and logical low when RIN is at voltage level 1.0 V. This is the differential threshold voltage at RIN (+/- 0.1 V). REFCLK is the input clock signal of the de-serializer. This clock signal must be equal to that of TCLK, or, if using a different clock signal, it must be within 5% of TCLK. This is important to ensure that the data transmitted from the serializer will be translated back to the original 16 bits properly. Clock jitter is the measure of deviation of a signal from being truly periodic. It is important for the team to account for clock jitter, since the signals for TCLK and REFCLK must have a maximum of 80 ps.

# 5.4.1.2 Initialization State

Before the DS92LV16 sends or receives data, it must initialize the links to and from another DS92LV16. Initialization refers to synchronizing the serializer's and de-serializer's phase-locked loop's (PLL) to local clocks. The local clocks must be the same frequency, or within the specified range of +/-5% if from different sources. After the Serializers synchronizes to the local clocks, the de-serializers synchronize to the Serializers as the second and final initialization step. The following are a more in-depth breakdown of the two steps carried out in the Initialization state.

1. When VCC is applied to both serializer and/or de-serializer, the respective outputs are held in TRI-STATE and internal circuitry is disabled by on-chip power-on circuitry. When VCC reaches VCC OK (2.2V) the PLL in each device begins locking to a local clock. For the serializer, the local clock is the transmit clock, TCLK. For the de-serializer, the local clock is applied to the REFCLK pin. An oscillator from the controller or other source provides the specified clock input to the TCLK and REFCLK pin.

   The serializer outputs are held in TRI-STATE while the PLL locks to the TCLK. After locking to TCLK, the serializer block is now ready to send data or synchronization patterns. If the SYNC pin is high, then the serializer block generates and sends the synchronization patterns (sync-pattern).

   The de-serializer output will remain TRI-STATE while its PLL locks to the REFCLK. Also, the de-serializer LOCK output will remain high until its PLL locks to an incoming data or sync-pattern on the RIN pins.

2. The de-serializer PLL must synchronize to the serializer to complete the initialization. The serializer that is generating the stream to the de-serializer must send random (non-repetitive) data patterns or sync-patterns during this step of the Initialization State. The de-serializer will lock onto sync-patterns within a specified amount of time. The lock to random data depends on the data patterns and therefore, the lock time is unspecified.

Using a specificed sync-pattern will be easier to use and account for, because the TCLK and REFCLK will not be coming from the same source, as the receiving side and transmitting side of the system will be meters away from each other.

#### 5.4.1.3 Data Transfer State

After initialization, the DS92LV16 serializer block is able to transfer data to the de-serializer. The serial data stream includes a start bit and a stop bit appended by the serializer, framing the sixteen data bits. These two bits also function as embedded clock information. For simplicity, the start bit will always be high, and the stop bit will always be low. The serializer block transmits the data and clock bits at 18 (16 data bits + 2 clock bits) times the frequency of TCLK. If TCLK is 60 MHz, for example, the serial rate will therefore be 1,080,000,000 bits per second. With this functionality in mind, the 1 GHz transmission from the Raspberry Pi to the laser is feasible.

When the de-serializer synchronizes to the input from a serializer, it drives the LOCK pin low and delivers valid data on the output. The de-serializer locks to the embedded clock, uses it to generate multiple internal data strobes, and then drives the recovered clock on the RCLK pin. The RCLK is synchronous to the data on the ROUT[0:15] pins. While LOCK is low, data on ROUT[0:15] is valid. Otherwise, ROUT[0:15] is invalid.

#### 5.4.1.4 Resynchronization State

Whenever the de-serializer loses lock, it tries to resynchronize automatically. The logic state of the LOCK signal indicates whether the data on ROUT is valid; when it is low, the data is valid. The system must monitor the LOCK pin to determine whether data on the ROUT is valid. Because there is a short delay in the LOCK signals response to the PLL losing synchronization to the incoming data stream, the system must determine the validity of data for the cycles before the LOCK signal goes high.

### 5.4.2 Computer Design #1

With the DS92LV16 serializer and de-serializer circuits studied, a more useful understanding of how to interface with this component was gained. This section provides an overview of how the system controller will interface with the rest of the components. The main objective of the computer sub-system is to enable communication between the microcontroller and the optical subsystem. This includes the transmitting side Raspberry Pi microcontroller, as well as the receiving side Raspberry Pi. The computer sub-system is also in charge of enabling transmissions at high speeds. The design will incorporate a serializer and d-serializer to achieve this transmission goal, since the Raspberry Pi GPIO pins are not sufficiently fast to achieve this without the usage of many more pins than what is available. It was established in previous sections that the Raspberry Pi 4 Model B would be the microcontroller of choice, and that TI's DS92LV16 would be used

to serialize parallel data into a serial stream and deserialize the stream back to parallel. The designs at the optical and power levels are not shown in detail since they will be discussed in other sections. Figure 57 shows the block diagram for computing side of the S.T.E.A.L.T.H. system.

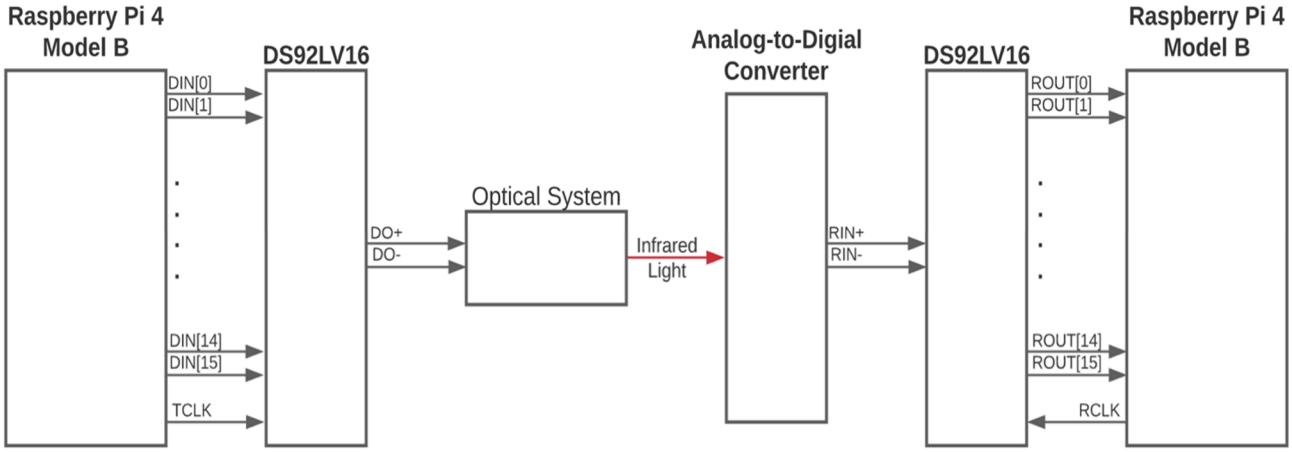



**Figure 75:** Block diagram of the computing system

The software block diagram is intended to help the team members outline a flow of steps that need to be carried out sequentially at the programming level. It provides a framework of all the important steps that will need to be met by the S.T.E.A.L.T.H. system to meet all functionalities. Figure 57 shows the software block diagram.

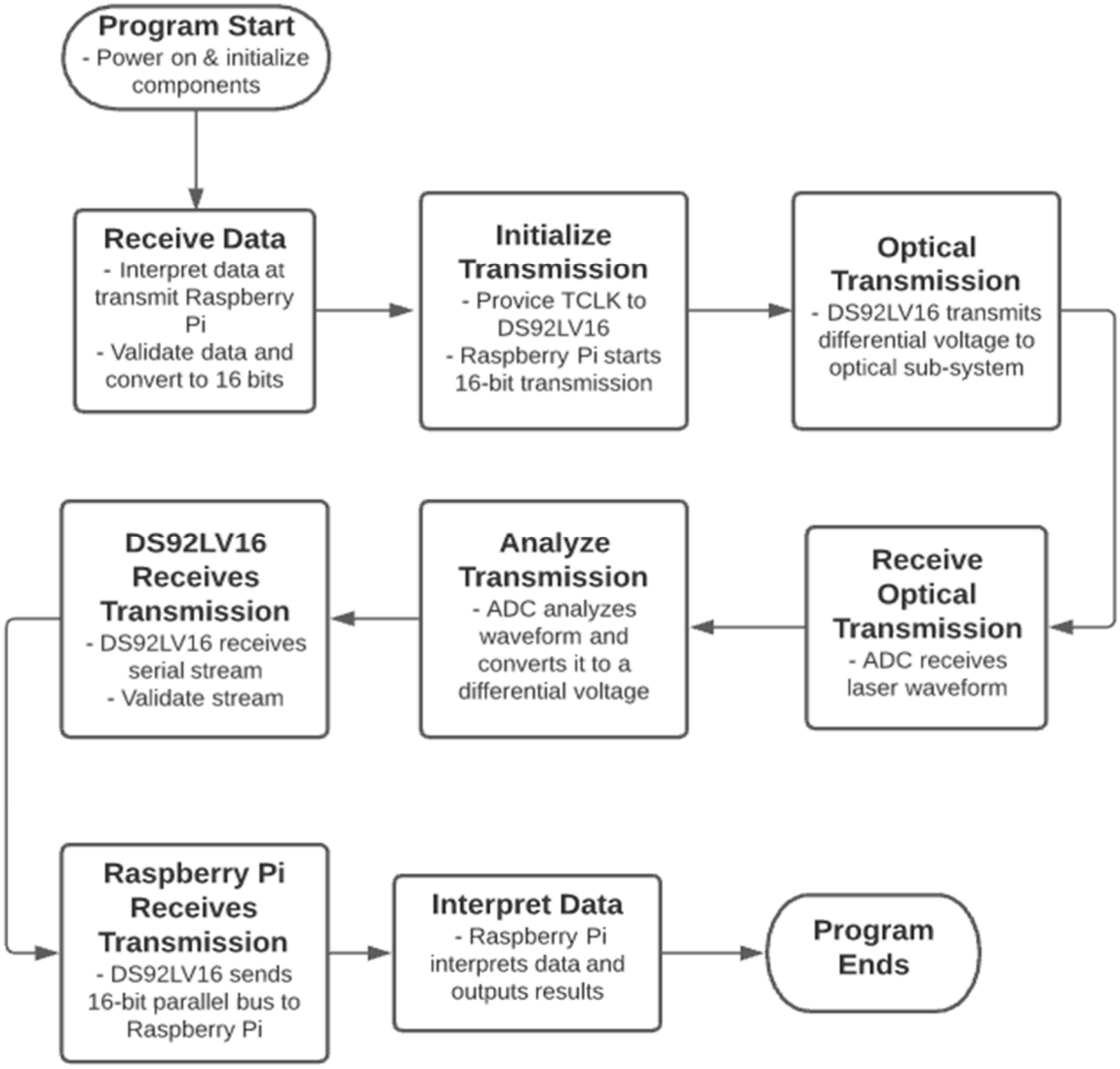



**Figure 76**: Software Block Diagram

After further research and more considerations taken into the design of the computer sub-system, it was decided that the Raspberry Pi 4 Model B would not provide adequate performance in the switching characteristics of the GPIO. For this reason, this initial computer design will not be further elaborated upon.

# 5.4.3 Computer Design #2

The previous system used a Raspberry Pi as a controller and also included an Analog-to-Digital converter (ADC) to capture the information from the photodetector. However, the Raspberry Pi as previously stated was not useful because of its low GPIO switching frequencies, and the usage of an ADC was similarly dismissed because the photodetector is capable of outputting an LVDS signal that will be read by the de-serializer at the receiving side of the system.

A new design for the computing sub-system is therefore proposed below. This sub-system uses Intel Altera's Cyclone IV development board, keeping the DS92LV16 integrated circuit. This combination was used due to a research paper written by Texas Instruments on how beneficial a component like the DS92LV16 is to reduce simultaneous switching noise of an LVCMOS signal.

The DS92LV16 is an integrated circuit with 80 pins available to be interfaced with. However, not all pins will be relevant at both sides of the system, since pins are specific to the serializer and de-serializer, and these two parts are independent of each other. The Cyclone IV must be able to interface with the data pins of the DS92LV16 at a similar frequency of the TCLK pin for the serializer and REFCLK for the de-serializer. The datasheet of the Cyclone IV specifies there is a bank of GPIO pins that capable of typical 200 MHz interfacing frequencies. This is more than enough for the S.T.E.A.L.T.H. system, as the DS92LV16 accepts a maximum frequency of 80 MHz for TCLK and REFCLK.

Using the functional specifications of the DS92LV16 datasheet, the serializer transmits the data bits with two embedded clock bits at 18 times the frequency of TCLK. Moreover, since only 16 bits are from input data, the serial payload rate is 16 times the TCLK frequency. This means that for the system to achieve a throughput of at least 1 gigabit per second, the frequency of TCLK must be set to at least 65 MHz, so the throughput is in total 1.040 gigabits per second.

The following figure shows a diagram of the system. More consideration was taken on this design, so the inclusion of an oscilloscope and a function generator was taken into account. The oscilloscope will help the team measure the frequency of the data going from the Cyclone IV to the serializer, as well as the serial stream. The function generator will allow the team to generate an external clock signal of 65 MHz to drive the FPGA and the DS92LV16.

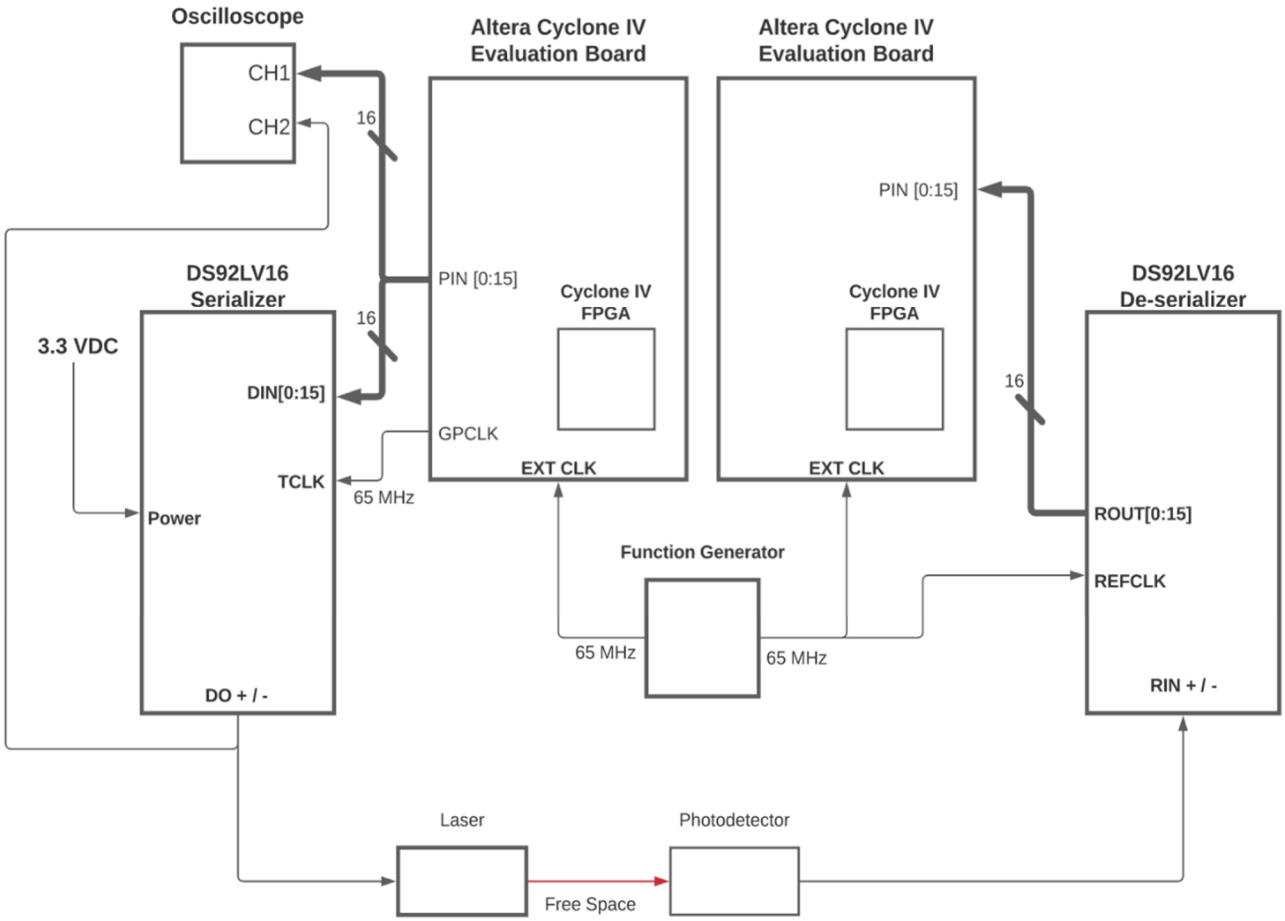



**Figure 77:** A schematic of the Computing Sub-System Design #2

# 5.5 Software Design

This section and its related subsections discuss the software of the S.T.E.A.L.T.H. system. The Cyclone IV development board will act as a computer that controls the data being transmitted and received. As stated before, two different FPGA's will be used, one on the receiving end and one on the transmitting end.

# 5.5.1 Design Methodology

As the team develops the code for the S.T.E.A.L.T.H. system, the team will go through multiple iterations of code development. Requirements may evolve as the team starts building different prototypes. To this end, the team will be using a method of project management called Agile Methodology. This methodology is a way to manage projects by breaking up tasks into several, smaller phases. Agile development focuses on intensive collaboration between team and work is done

in various stages, called sprints. The use of this methodology is due to Moises Cruz's experience while working on FPGA development with his co-workers.

As the team develops the system, new challenges that were not foreseen by the team will arise, such as incompatibility between devices, or software development issues. Agile development also uses what is called "scrum meetings," where a leader tries to clear challenges and obstacles to complete work. The team should hold scrums frequently to maintain communication while the project is being assembled.

## 5.5.2 Development Tools

The Cyclone IV can be programmed using Intel's design software called Quartus Prime. The Quartus Prime software offers a 'Lite' alternative that is free to download and use, at the expense of not offering support to all Intel FPGAs. The Cyclone IV, however, can be programmed using the Lite version, reducing the team's overall spending. An Intel account was required to download the software, but a free account alternative was also offered. The version of Quartus Prime that will be used by the team is version 21.1, the latest version available. The Quartus Prime design software offers sample projects that will allow the team to become familiar with the device, as well as how to program hardware with Verilog or VHDL.

## 5.5.3 Software Functionality

The software in the S.T.E.A.L.T.H. system will have 4 tasks to carry out: read and interpret input data at the transmitter, send data from transmitter to the serializer, read data from the de-serializer at the receiver, and interpret and manipulate the data received. A breakdown of the software functionality is also shown graphically.

## 5.5.3.1 Reading Data

The S.T.E.A.L.T.H. system will receive data from a USB file. This data resolution will be 16 bits, given that the serializer used, the DS92LV16, accepts up to 16 bits in parallel. The Cyclone IV board that will be used includes a USB expansion module, which allows the user to connect a USB or a microSD card. The team will employ this USB expansion module to load the data to the FPGA. The USB module is attached to the development board through a JTAG connection.

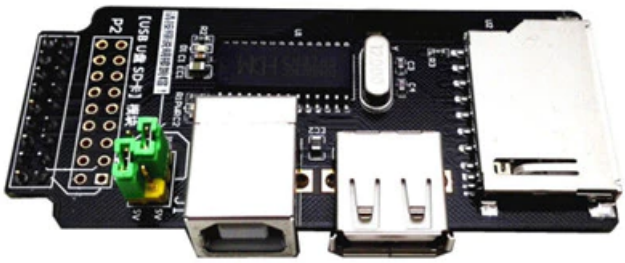


**Figure 78:** USB expansion module

To read data from a file, the TextIO library is the standard library used in VHDL to read and write. The syntax to open a file and read from it is as follows:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use std.textio.all;

-- Declare and Open file in read mode:

file file_handler     : text open read_mode is “filename.dat”;
Variable row          : line;
Variable v_data_read  : integer;

-- Read line from file
readline(file_handler, row);

-- Read value from line
read(row, v_data_read);

constant NUM_COL               : integer := 2;   -- number of column of file

type t_integer_array       is array(integer range <> )  of integer;
file test_vector               : text open read_mode is "file_name.txt";
variable row                   : line;
variable v_data_read           : t_integer_array(1 to NUM_COL);
variable v_data_row_counter    : integer := 0;
```

# 5.5.3.2 Transmitting and Receiving Data from DS92LV16

To transmit logic through the GPIO of the FPGA, the following code will be used as a basis to set the state of the pins.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity output_top is
    Port ( OUT_1 : out  STD_LOGIC;
           OUT_4 : out  STD_LOGIC_VECTOR (3 downto 0));
end output_top;

begin
    OUT_1 <= '0';
    OUT_4 <= "0110";

end Behavioral;
```

```
begin

  if(rstb='0') then

    v_data_row_counter     := 0;
    v_data_read            := (others=> -1);

    i_op1                  <= (others=>'0');
    i_op2                  <= (others=>'0');

  elsif(rising_edge(clk)) then

    if(ena = '1') then  -- external enable signal

    -- read from input file in "row" variable
      if(not endfile(test_vector)) then
        v_data_row_counter := v_data_row_counter + 1;
        readline(test_vector,row);
      end if;

    -- read integer number from "row" variable in integer array
      for kk in 1 to NUM_COL loop
        read(row,v_data_read(kk));
      end loop;

      value1_std_logic_8_bit    <= conv_std_logic_vector(v_data_read(1),8);
      value2_std_logic_8_bit    <= conv_std_logic_vector(v_data_read(2),8);

    end if;

  end if;
end process p_read;
```

The declaration ‘OUT_1 : out STD_LOGIC’ will set exactly one pin as an output, and it is later set to low with ‘OUT_1 <= 0’. Alternatively, 4 pins can be set as outputs by using the declaration ‘OUT_4 : out STD_LOGIC_VECTOR(3 downto 0)’. In the case of the S.T.E.A.L.T.H. system, this declaration would change to ‘OUT_16 : out STD_LOGIC_VECTOR(15 downto 0)’ to set the required 16 pins.

Similarly, to use a pin as an input, the following code could be used.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity input_top is
    Port ( IN_1 : in  STD_LOGIC;
           IN_16 : in  STD_LOGIC_VECTOR (15 downto 0));
end input_top;
```

# 5.5.3.3 Manipulate and Display Received Data

To ensure that functionality is being met, the team will have to display the data to ensure that it is complete and correct. It is necessary for the receiving end of the system to be connected to a monitor to show the data in real time. To this end, communication with the FPGA and an outside computer is necessary, using communication protocols such as UART. Using UART, the team will be able to display the incoming 16-bit words and compare them to the data being transmitted.

# 5.6 Summary of Design

In this section the team will discuss the design process, any design hurdles we faced, and outline how the process went. This section will provide insight to the design process from the teams perspective.

For electrical design there were some hurdles that were not in the initial scope. Such as interfacing with the laser is an ongoing hurdle as vendor support is non-existent and if the spec sheets provided are lacking to say the least. All that is provided is a PIN layout. Which is understandable as these lasers are typically for lab environment testing. So the design hurdle is being able to interface properly and being able to modulate the current sufficiently for the speeds desired. Another hurdle has been learning how to use fusion 360 from Autodesk. As eagle software we learned from junior design was not capable of having multiple components that I required for some reason. Learning how to utilize fusion 360 is a good skill I am still developing and creating the PCBs that I have with the required components. These components are much more technically advanced than the components we used in junior design. I have been utilizing resources that I have available online and in person through friends and colleagues. We have been in communication with a couple PCB printing companies that have been helpful but unfortunately our components are very small and soldering them will take an experienced person to do this. These components only have nanometers of clearance between pins due to the nature of the components being of a high-speed capability.

# 6.0 Project Prototype Construction and Coding

A prototype is an initial sample, model, or release of a product built to test a concept or process. It is almost impossible to find a product that is currently sold in the world that did not start with a prototype. Prototyping is the process of creating specifications for a real, functioning system and not just a theoretical one. Any professional engineer will these terms as they a part of engineering life. As stated before, a prototype does not just apply to tangible objects. New workflow and system organization prototypes are very common. There are entire companies that produce products that are designed to allow rapid prototyping. Rapid prototyping is exactly what the name suggests, producing prototypes rapidly. These companies do this by using an array of lasers to scan the surface features of the original prototype, then upload these features into 3D space. Once in 3D space, a 3D printer can be used to reproduce the original prototype. This process is advantageous because it is usually much cheaper and faster than conventional methods such as machining and building everything by hand.

# 6.1 Initial Optical Prototype Demo

As part of the optics requirements for the Senior Design process, it was required that a demonstration of a subset of optical features was constructed and given in the undergraduate lab at CREOL. Though our laser which states a maximum lead time of 2 weeks was ordered over 4 weeks prior to the date of this demonstration, it did not come in in time for the demonstration. To compensate, and to make the demonstration easier to understand visually, a visible LED and photodiode pair were substituted for the 1550 nm components. The phenomena we sought to demonstrate as a proof of concept of the base underlying principle was the Free Space Optical transmission of a signal. Our goal was to modulate a light source with a digital signal driven by a function generator and read the recovered signal from a photodiode circuit using an oscilloscope.

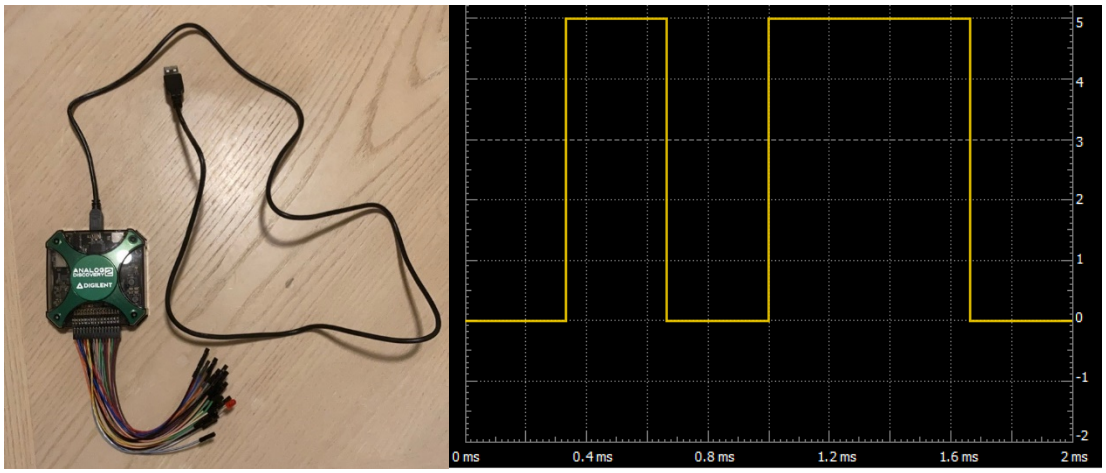



**Figure 79:** Digilent Analog Discovery 2 control board used to create and drive digital input signal of visible LED (Left) and the digital signal created using Digilent Waveforms Wavegen consisting of the serial bit stream 0 1 0 1 1 0 (Right).

For testing purposes, our team received a discovery kit containing electrical components and devices for rapid initial prototyping and early testing. In place of the IR DFB Laser, a 632 nm LED was used so that at low frequencies the modulation could be visibly seen for demonstration purposes. The LED was driven using the modulatable voltage output pins on the Digilent Analog Discovery 2 board included in the discovery kit seen above in Figure 78. There is potential for this device to be further used to for easily controllable modulation input to test our laser's functionality independent of having a finished modulation solution using our microcontroller.

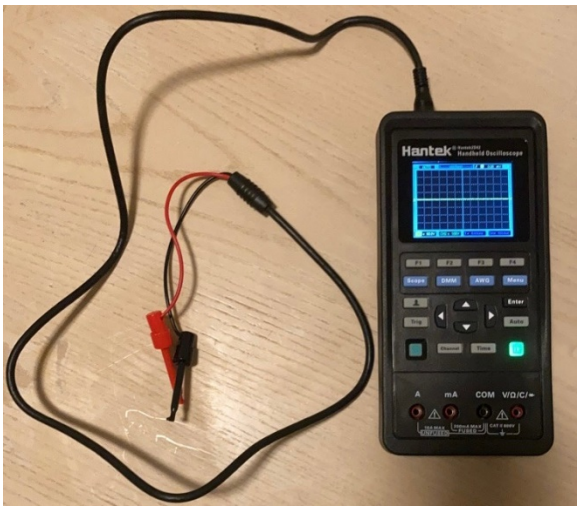



**Figure 80:** Hantek 2D42 3-in-1 Oscilloscope used to read photodiode output

The photodiode used was a Thorlabs Si PIN Photodiode whose optimal circuit is relatively equivalent to the Thorlabs InGaAs Photodiode we have ordered for the telecom IR band our laser will operate in. The photodiode was separated by a few

centimeters of free space and the signal it produced was measured across a series resistor by the Hantek handheld oscilloscope seen above in Figure 79. The photodiode circuit contained an RC noise filter as recommended by Thorlabs whose schematic can be seen in Figure 80. The received signal witnessed on the oscilloscope followed the same features and bit sequence as the transmitted signal. It was observed in the demonstration that as the LED moved farther away, the signal clarity decreased with irradiance until the low power LED was no longer overcoming the ambient room light for a visible photodiode. This problem is mitigated two-fold by our actual intended photodiode at 1550 nm due to both lower ambient light in that band as well as spectral filtering. The RC filter used in the prototype demonstration used a higher capacitance than that seen in Figure 80 due to component availability. This increases the RC time constant of the circuit, thusly increasing the rise time and corresponding response time of the photodiode. Additionally, to increase the voltage read by the oscilloscope, the largest value available for resistor $R_L$ (10k Ohms) was used in order to increase $V_O$ via Ohm's Law.

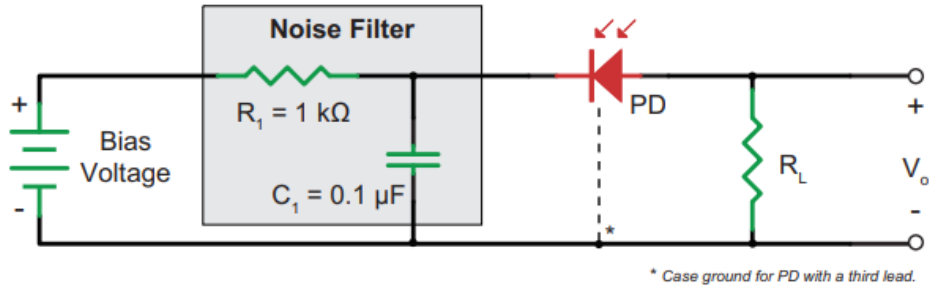



**Figure 81:** Photodiode circuit used for initial prototype demonstration including RC noise filter.

# 6.2 DS92LV16 PCB Design

To test the serializer and de-serializer circuit, a printed circuit board (PCB) needed to be designed, since the chip is not able to be plugged into a breadboard. The PCB for the DS92LV16 will be designed using Eagle, since the software functionality was used in Junior Design in previous semesters. The following figure shows a prototype of a schematic layout using the DS92LV16 built on Eagle. This schematic was built using recommendations and guidelines found in the device's datasheet.

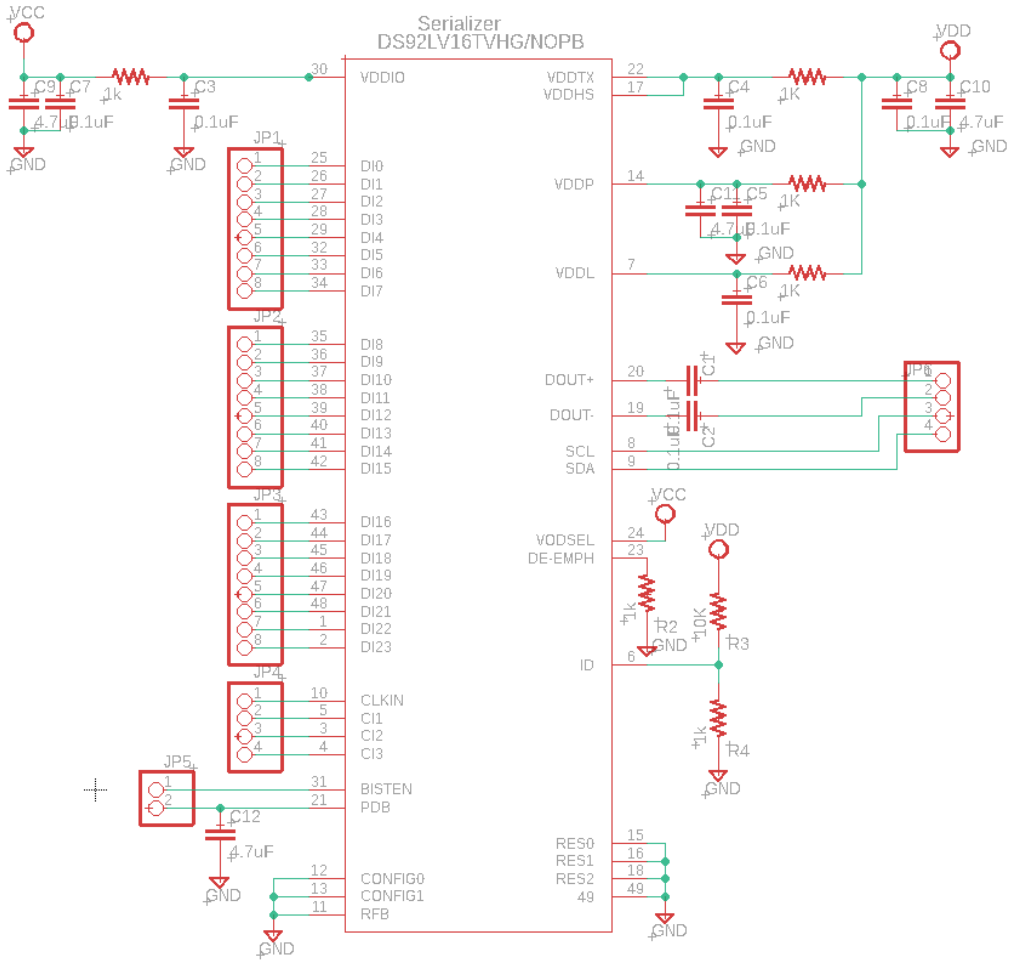



**Figure 82**: The schematic built on Eagle for the DS92LV16

Consequently, the team built a PCB layout using Eagle. The PCB for this device is shown in the figure below. A bill of materials for the components used on this layout can be found in Section 8 of this report.

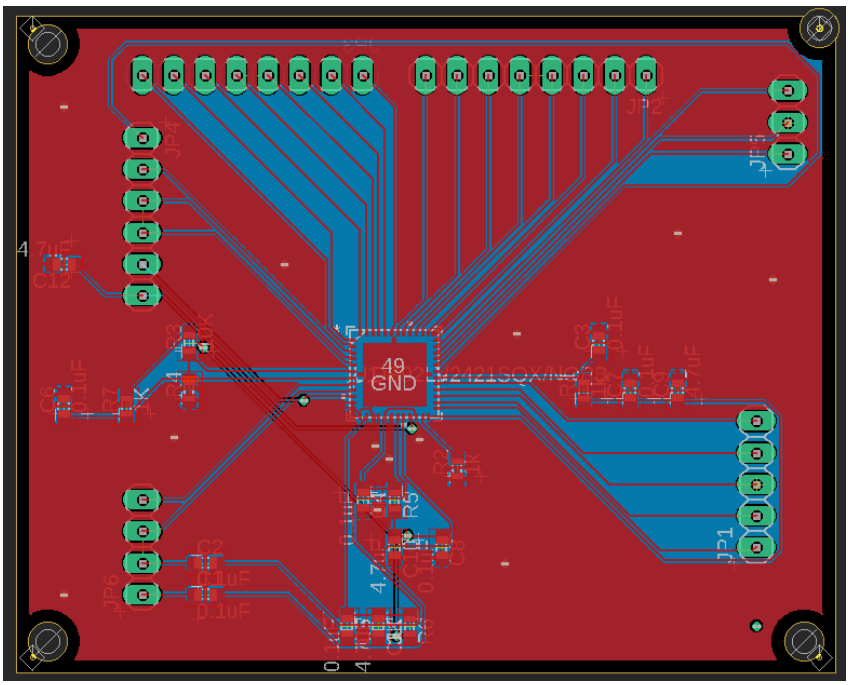



**Figure 83:** PCB Layout of the DS92LV16

# 7.0 Project Prototype Testing Plan

In this section we will detail early plans for future project testing. It is important to keep testing plans in mind throughout the design process, as there needs to be considerations made in some design decisions to ensure that when the project physically comes together it is feasible to be tested. These considerations were also tied to the requirements specifications as it is importance that in order to be useful, a requirement specification is verifiable, and some requirements may be verified via the test process. As discussed in the constraints section, it is also important to ensure that a viable test plan exists within your constraints. The test plans and constraints inform each other. For example, it is useful for testing flexibility and safety that our laser is eye safe which informs the need for eye safety to be a constraint. Then when it comes to potentially testing this project at desired ranges, due to FAA constraints, it is essentially required that the laser be eye safe.

# 7.1 Hardware Test Environment

In this section the team will outline all testing that has been done up to this point. This section will cover what each member has done to test the project hardware.

For electrical testing I have been simulating all of my circuits that have required free hand design. Including the laser modulation circuit, and the photodetector circuit. Utilizing multisim online I have been able to gain knowledge of how the expected circuits should work and will be able to implement them in a physical manner when we receive our final PCBs for testing. Unfortunately, due to the nature of the products we are using no development boards were available. The pins on these devices as mentioned previously are only nanometers apart. This made testing on a breadboard impossible. The work around to this has been that we have expedited PCB designs and should be receiving them shortly to continue testing them over the winter break.

# 7.2 Software Testing

Testing the software is an important step for the system to perform according to the desired functionality. Intel's Quartus Prime development environment provides support for testing and simulating the hardware design before connecting the FPGA. The use of testbenches will be crucial to ensure that the system is meeting the timing constraints of 1 GHz transmission.

Moreover, the DS92LV16 device provides ways to test the operation. The DS92LV16 includes two modes for testing, the Line Loopback, and the Local Loopback. Using the Line Loopback control signal connects the de-serializer data input (RIN +/-) to the serializer data output (DO +/-). The serializer output will go

through the de-serializer and output data on pins (ROUT[0:15]) to ensure that the device is functioning as expected.

The Local Loopback control signal will connect the parallel inputs of the serializer (DIN[0:15]) to the parallel outputs of the de-serializer (ROUT[0:15]). These two tests will help the team have a look at the timing constraints of the DS92LV16. Using an oscilloscope connected to the serializer output and function generators at the serializer inputs, the team will be able to ensure that the data that is being sent from the function generators is received accurately at the output.

# 8. Administrative Content

In this section the team will discuss and plan all administrative / managerial tasks. This includes budgeting, work ethics, and time management planning. This is crucial for project deliverables and accountability.

On the electrical end of this project the team has been working together very well. We all assumed managerial status in keeping tabs on everyone and holding each other accountable. With three of the team members previously knowing and working each other through classes we had a good communication system in place that transferred very well into senior design with being able to hold respect for each other while being able to approach each other when we had issues. Ethically we had a conversation at the beginning of the course that made each other aware of one another's capabilities and work load through the semester. Communication was a crucial thing for me, and the team exceeded my hopes. Any information that I needed for my design responsibilities was met in a timely manner. I took it upon myself to make sure everyone held their own and pulled their own weight. Although it was not needed, I made it a point to have weekly and sometimes bi weekly meetings for brainstorming and even friendly hangouts. Moises being the new person to our existing friendship trio integrated without hiccup. He came into the group friendly, and eager to work. He has exceeded expectations as a group member.

# 8.1 Milestone Discussion

At the beginning of this project, we laid out a projected timeline for milestones that we needed to achieve throughout the design process. As we get more stuff into the purchasing and ordering timeline, we intend to create a more informed project timeline that involves more concrete plans of subsystem construction and system integration.


**Figure 84:** Gantt Chart of the initial project milestones

# 8.2 Budget and Finance Discussion

Above a list of our budgetary considerations to date can be seen in Table 7. We are thankful to have the support of Dr. Kyle Renshaw on this project as both an advisor as well as sponsor. As far as power supply goes, drone batteries have been made available to us to use that we do not have to buy. While the lasers may seem expensive, the fact that it is directly modulated at up to 4 GHz inherently allows us to forego the need to externally modulate our signal. High quality external electro-optical modulators can themselves be more expensive than the sticker price of our laser, which in the end was actually a budget friendly choice relatively speaking. This table currently does not account for additional spare parts that may be required to replace any components that we may burn up or damage. A price for housing is not listed but we intend to design a 3d printed housing which we do not expect to be of significant cost.

**Table 17:** Current bill of materials

| Component | Cost per each | Quantity needed | Total expense |
|---|---|---|---|
| 4 GHz DFB Laser | $825 | 2 | $1,650 |
| IR Photodiode | $58.35 | 2 | $117 |
| Voltage Converters | $3 | 30 | $90 |
| Bandpass Filter | $189 | 2 | $378 |
| Receiving Lens | $73 | 2 | $146 |
| Microcontroller | $107 | 2 | $1 |
| Total: | | | $2,491 |

The following table shows the bill of materials generated in Eagle for the DS92LV16 serializer and de-serializer.

**Table 18:** Bill of materials for the DS92LV16 PCB layout

| Device | Value | Quantity | Price | Total Cost |
|---|---|---|---|---|
| **C-EUC0603** | 0.1uF | 8 | $0.13 | $1.04 |
| | 4.7uF | 4 | $0.33 | $1.32 |
| **R-US_R0603** | 1k | 6 | $0.10 | $0.60 |
| | 10k | 1 | $0.10 | $0.10 |
| **Pin Headers** | 1x3 | 1 | $4.80 | $4.80 |
| | 1x4 | 1 | $4.81 | $4.81 |
| | 1x5 | 1 | $5.52 | $5.52 |
| | 1x8 | 2 | $3.55 | $7.10 |
| **DS92LV16** | | 2 | $19.72 | $39.44 |

# 9.0 Senior Design II Discussion

Chapter 9 of this report will provide an update of the S.T.E.A.L.T.H. project, any successes the team was able to achieve, and the difficulties that were faced. From Senior Design I to Senior Design II, many design changes occurred, specifically in the Optical and Electrical subsystems. Part availability and lead times of components severely hindered the ability of the team to build a working prototype as it was originally envisioned in Senior Design I. The following subsections will provide details on how the team tested the system. The image below shows a general block diagram of the finalized system and what the working prototype that was delivered in the final hardware demonstration.

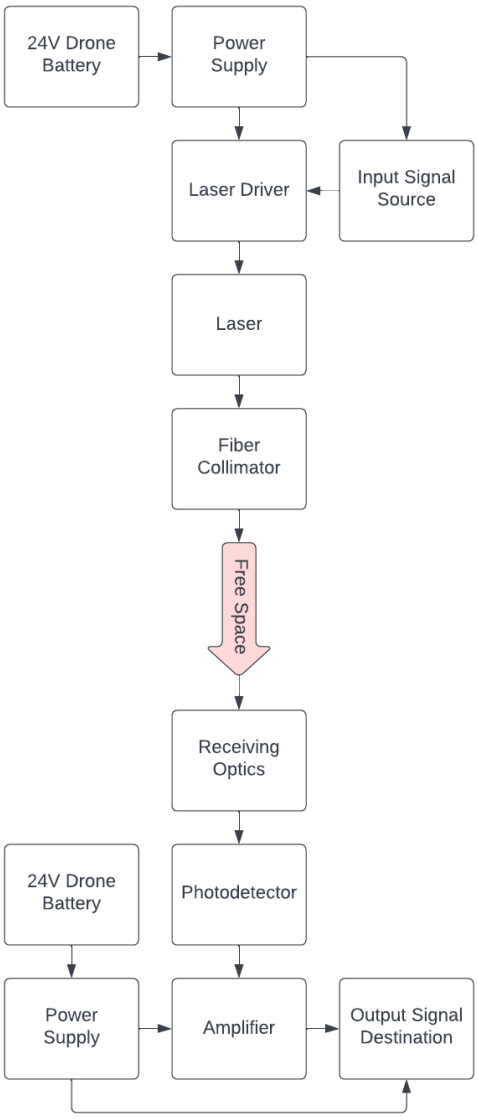



Figure 85: Generalized Overall System Diagram

# 9.1 Optical

The core optical challenge of this project was to align, instantiate and analyze an optical that would serve as a substitute for an electrical connection (i.e. wire) or RF connection in a communication system. In Senior Design 1, we estimated theoretical atmospheric impact on optical power transmittance up to 1 km, and designed the optics around reaching 1 km while estimating and mitigating ambient solar noise from the sun to improve OSNR. In Senior Design 2, some of this design was tweaked and optimized. Additionally, Zemax was used to inform component spacings used to design a 3d housing that not only holds components in place, but maintains their axially alignment.

## 9.1.1 Optical Design Updates

In Senior Design 1, optical power calculations were made based using a 2 inch lens to collect irradiance from a 1mrad diverged beam at 1 km, which yields a 2 meter diameter beam at range. In Senior Design 2, these calculations were formalized into a simple but more traditional link budget analysis table in units of dBm seen below.

| Link Budget | | | |
|---|---|---|---|
| Parameter | | Value | dB |
| Transmit Power (Peak) | $P_{tx}$ | 20 mW | 13.01 dBm |
| Divergence | $\theta_{div}$ | 1mrad | |
| Link Distance | L | 1 km | |
| Receiving Aperture | $D_{rx}$ | 50.8 mm | |
| Divergence Loss | $A_{div}$ | 93.6% @ 1 km | -31.9 dB |
| Atmospheric extinction | $A_e*$ | 0.004345 dB/km | -0.004345 dB |
| Received Power | $P_{rx}$ | 12.899 μW | - 18.894 dBm |

Table 19: Simple link budget analysis which informed signal power and consequently OSNR expectations

At the start of Senior Design 2, an attempt was made to redesign the transmitting optics with hand selected off the shelf lenses in order to create a 3-lens divergence controller. The working principle is based on that of a beam expander, with the addition of an intermediary negative lens to the ordinarily 2f system which changes the output divergence of the system as a function of distance between the 2nd and 3rd lenses. This would allow the user to effect the divergence of the transmit module just by changing the spacing of the intermediary lens. This idea was ultimately scrapped for multiple reasons and reverted back to the original intended design of using an aspheric fiber collimator to more accurately control beam divergence. The primary reason the design was reverted was that even for an idealized system, the minimum volumetric size of the components was still much greater than the size of the fiber collimator, which risked the project missing the requirement specification of volumetric footprint. Even if volume was inconsequential, the

additional challenge of keeping all 3 lenses axially aligned nicely in a jittering system added undue complication to furthering the system's UAV platform compatibility, which is something we sought to optimize at every opportunity in order to maximize the system's usefulness in the future. Below, one of the simpler designs of the divergence controller can be seen.

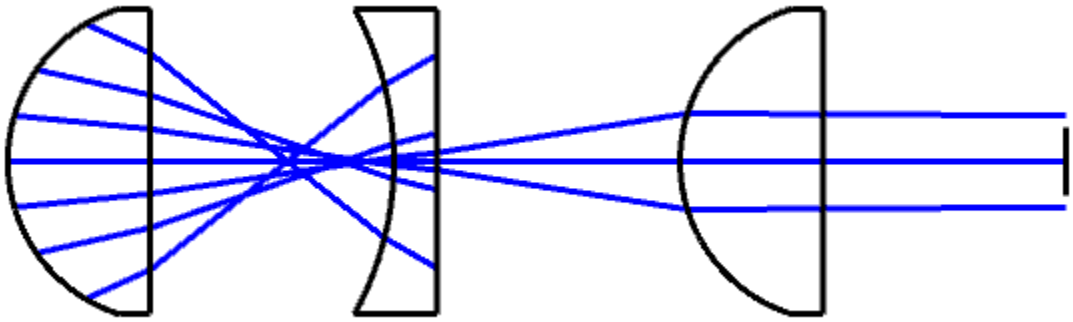


Figure 86: Flipped divergence controller prototype design attempt in Zemax

It is also worth noting that designing such a system is especially challenging in Zemax OpticStudio, which is the optical design and optimization tool used in this project. Zemax thrives at designing focal systems meant to bring ray's to an image, however it is not as intentionally useful for designing illumination or defocusing systems. While light at 1 mrad is fairly collimated, the way Zemax would traditionally optimize a collimator is by attempting to minimize the divergence toward 0. Trying to target a specific small nonzero number such as 1/1000 is more challenging, as there is not as much native support for such an optimization. The above figure may seem strange as light which should be diverging from the front lens is seen as converging. This is because one novel approach to designing defocusing systems is to use Zemax's strengths of designing focal systems to your advantage by flipping the system. In this figure, a negatively spaced virtual object was used based on the desired beam diameter at a specified distance whose ratio would yield 1 mrad. In theory optimizing the focal spot to and distance to represent the size and spacing to your source (in our case, the fiber laser output) would give the desired divergence into free space at the system output, however before making these difficult optimizations, the design was reverted for the above stated reasons that make even an ideal divergence controller less suitable for this project than an optic designed for fiber collimation into free space.

## 9.1.2 Optical Component Changes

The original design for the transmitting optics intended to use a fiber collimator. During the early stages of Senior Design 2, an attempt was made in designing and optimizing a 3-lens divergence controller leveraging the properties of a beam expander with the inclusion of an additional intermediary negative lens to offset the paraxial output of paraxial input rays of the 2f system. This solution was ultimately

not implemented because despite optimization efforts it was less efficient in the categories of volumetric efficiency, on axis stability (more susceptible to platform jitter), and cost to using a fiber collimator to maintain a small constant divergence more reliably. The fiber collimator also has the advantage of being the same price or cheaper depending on the choice of glass optics for the divergence controller. The fiber collimator selected was chosen based on the goal of having a 1-meter beam radius at a 1-kilometer range, thus requiring a 1/1000, or 1 mrad divergence angle.


Figure 87: Fiber Optic Collimator with
0.053 degree ≈ 1 mrad divergence

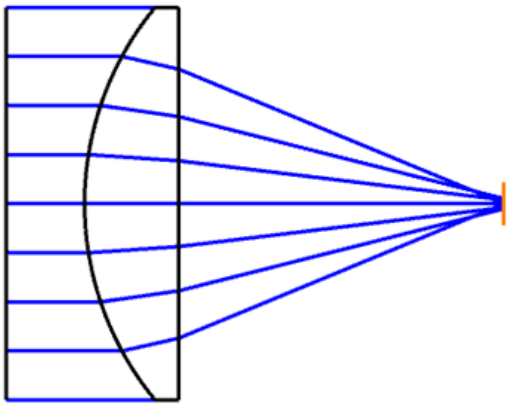


Figure 88: Receiving lens Zemax focal distance analysis

On the receiving end not much changed about the original design, aside from additional Zemax analysis used to inform the system housing design to align the photodiode active area with the point of best focus. We still wanted to collect as much of light as possible so to compensate for the lowered irradiance at long ranges due to beam divergence we chose to trade some form factor for collecting aperture area, opting for a 2-inch diameter plano-convex lens in order to collect a sufficient amount of light to recover enough signal amplitude for signal recovery. The lens that was selected was a fast N-SF11 lens with F/1 as seen being benchtop tested below in Figure X. This short ~50mm focal length lens allows the minimum optical train length on the receiving end to be more compact axially, further supporting form factor goals, which further eases pointing requirements for use cases such as UAV integration.

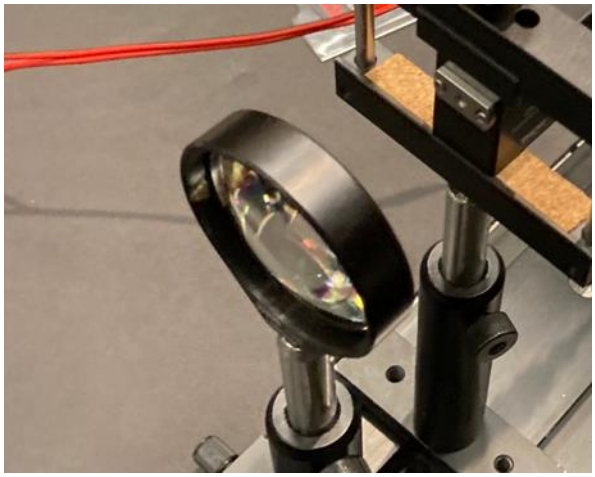


Figure 89: N-SF11 Receiving module collection lens

## 9.1.3 Prototype Construction

A prototype housing was created for the receiving end optics, bandpass filter, and photodetector. The purpose of the housing was to properly secure and align the components to mitigate the effects of jitter if the system was to be mounted on an aerial platform. There were two main challenges to overcome for this design to be successful. One was finding the optimal focal distance between the lens and the active area of the photodetector, and the other was designing the actual lens mount to properly hold the lens so that the focal point was on axis with the photodetector and bandpass filter.

Four generations were created to work out any design flaws, with the fourth generation shown in the figures below. A measured slot for the bandpass filter was added directly in front of the active area to minimize the chances of any undesired wavelengths making it passed the filter. An unforeseen problem was the extra weight added on the back of the photodetector from the data connection. This caused it to want to lean back, thus moving the active area off the optical axis. A countersunk hole was added to the bottom of the housing so that a washer and screw could be installed to properly secure the photodetector, while keeping the bottom surface flat.

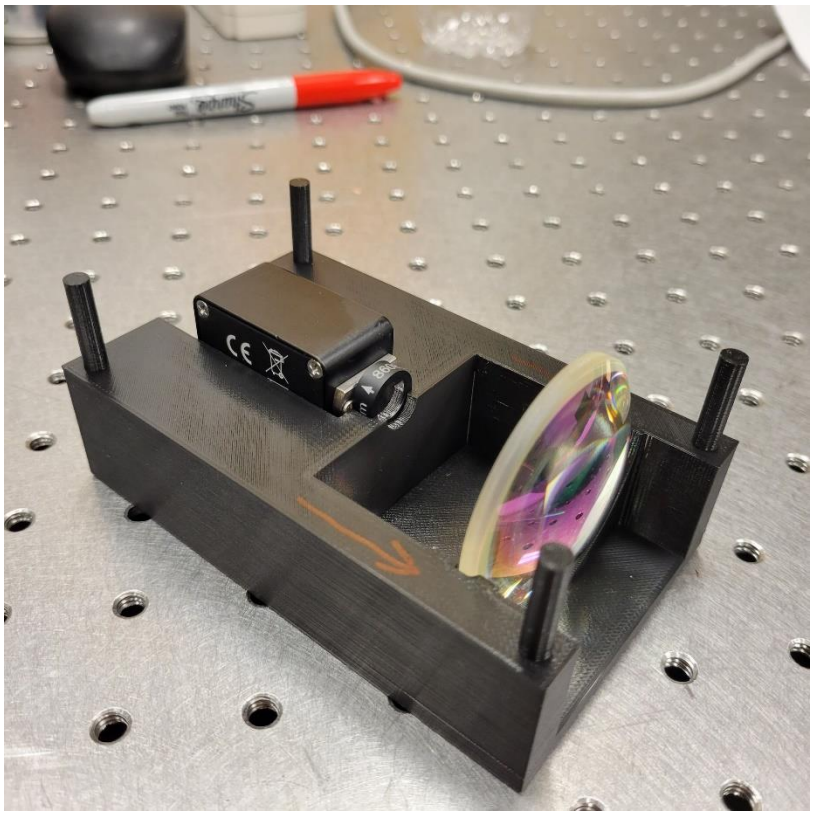


Figure 90: Bottom Half of Receiving End Optics Prototype

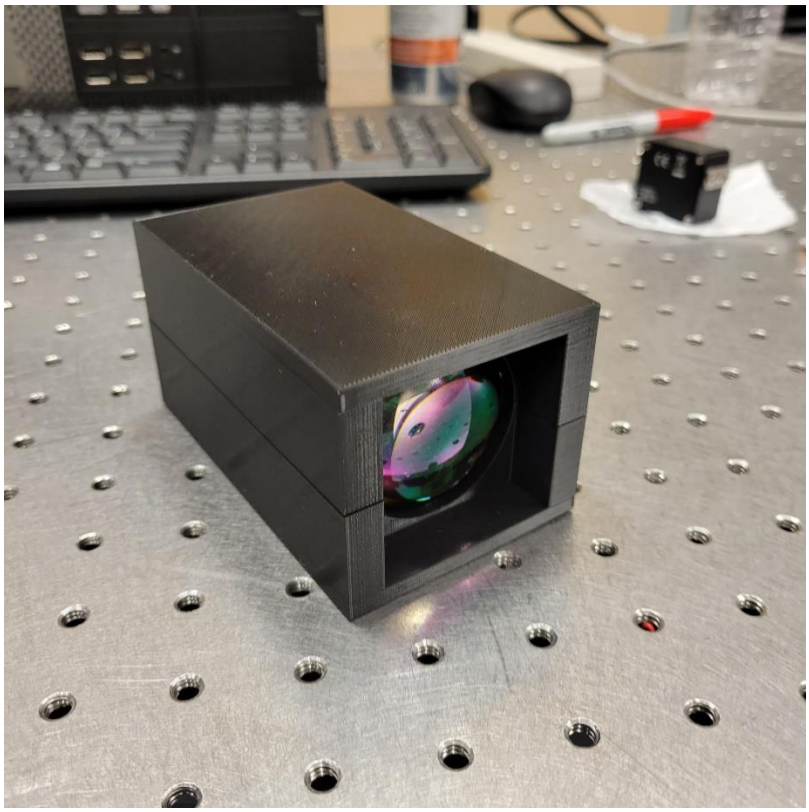


Figure 91: Fully Assembled Receiving End Optics Prototype

# 9.2 Computer Hardware & Software Discussion

The computer subsystem for S.T.E.A.L.T.H. consists of the Altera Cyclone IV FPGA and DS92LV2421 Serializer and DS92LV2422 De-serializer. This section will provide a discussion of these components and how the designed has changed from that of Senior Design I.

## 9.2.1 Updated Computer Design

In the Senior Design I discussion, the Computer Hardware design included the DS92LV16 chip, which contains a serializer and de-serializer developed by Texas Instruments, whose function is to serialize and de-serialize a 16-bit parallel bus into a serial stream and back. In Senior Design II, the procurement for this chip proved difficult since TI updated the design and manufacture of this chip for a 24-bit alternative, which also separates the serializer and de-serializer pair into their own chips. These two chips are the DS92LV2421 and DS92LV2422, respectively. The operation of Serializer and de-serializer pair remained largely the same as the 16-bit alternative that was originally researched for Senior Design I, so the information from those sections regarding operation remain relevant. The only differences are the parallel bus channel increase to 24 bits versus 16, the clock frequency ratings for the clock input changing from 25-80MHz to 10-75MHz, the serializer and de-serializer design being transferred to their own separate chips, and new enable and control pins added to the chips' designs. For simplicity's sake, the serializer and de-serializer pair will henceforth be referred to in this paper as DS92LV242X.

The team designed printed circuit boards for the DS92LV242X. The designs for these PCBs are shown in the figures below, which contain the footprints and 3D rendering for said PCBs built on Autodesk Fusion 360. These were designed according to the specifications of the datasheet.

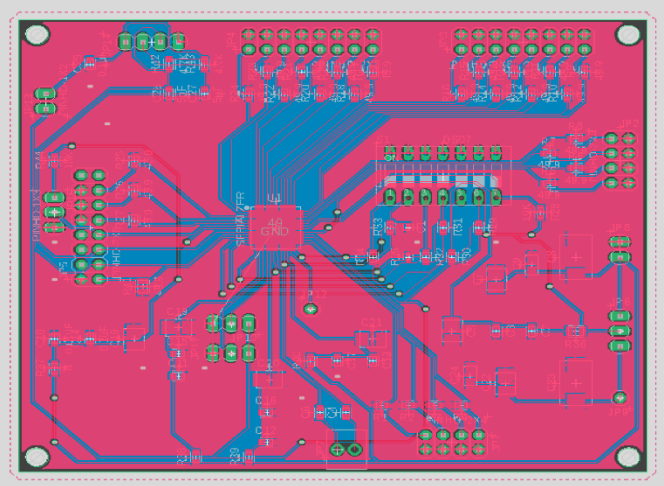


Figure 92: DS92LV2421 Serializer PCB footprint

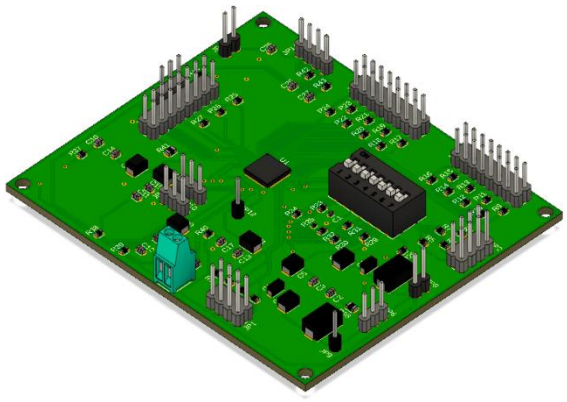


Figure 93: DS92LV2421 Serializer PCB 3D rendering

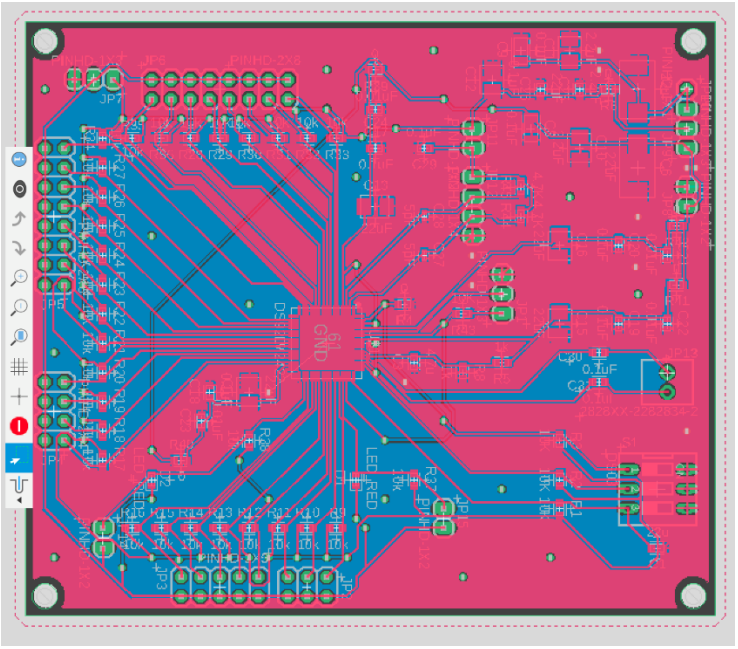


Figure 94: DS92LV2422 De-serializer PCB footprint

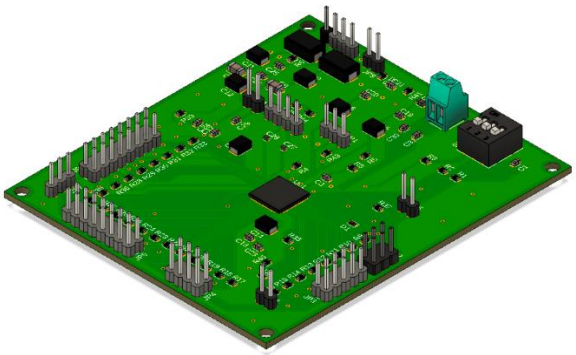


Figure 95: DS92LV2422 De-serializer PCB 3D rendering

The built prototypes for these PCBs are shown below, assembled by Quality Manufacturing Services in Orlando, FL.

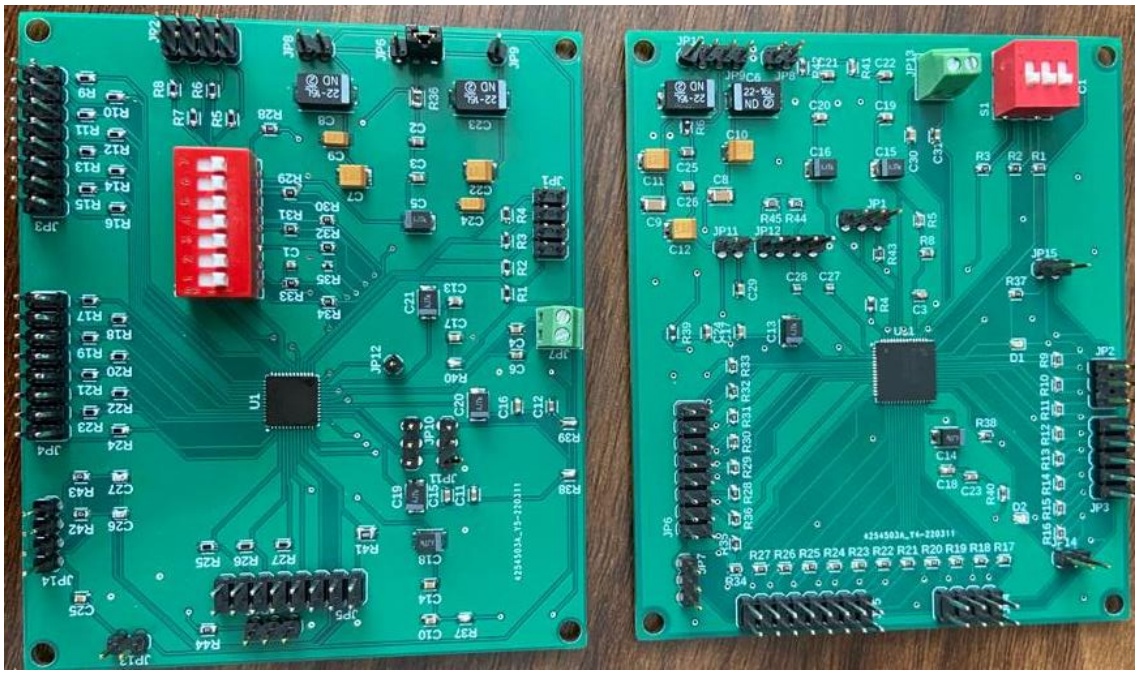


Figure 96: Assembled DS92LV242X boards

The team had also acquired a development board for this chip pair, designed by TI. After testing of the designed PCBs, was being transmitted between the two. Some fault must have occurred in the design of the PCBs, and given the time constraints of the project, as well as finding out that, being an optics project, the PCB requirements are relaxed, the team decided to use the acquired development boards and focus instead on learning how to program said boards and assemble a working prototype of the entire system. These are show below.

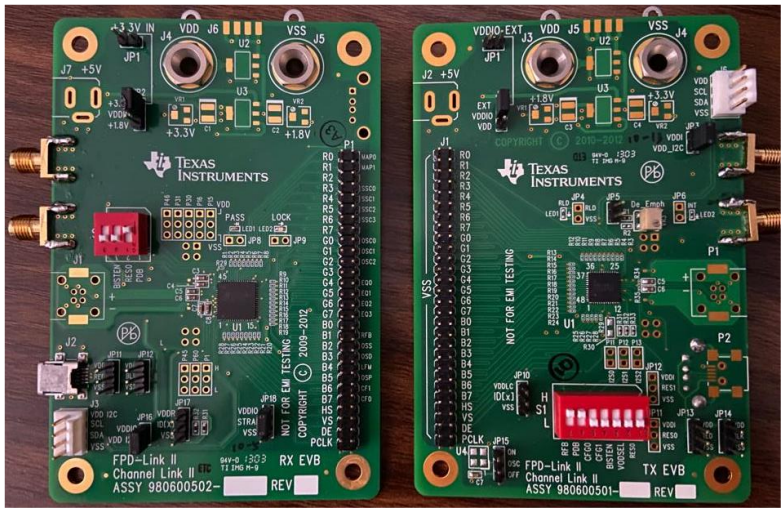



Figure 97: DS92LV242X boards used

The Cyclone IV FPGA selection remained the same, since it met the requirements and did not need adjustments.

## 9.2.2 Hardware and Software Testing

To test the Cyclone IV and DS92LV242X operation, a timer operation was programmed on the transmitting FPGA that counts up every second. This timer was displayed on the FPGA board's 4-digit 7-segment display. The controls for the timer where then transmitted through the FPGA's GPIO pins to the serializer, along with control signals for the DS92LV242X system to be able to serialize data and a clock input of 50 MHz being generated from the FPGA. The operation was intended to be tested electrically to prove that data was being successfully transmitted between the two ends of the system, to then connect everything optically. The serializer was connected through a USB to the de-serializer. As mentioned in previous sections, the DS92LV242X system inserts clock bits into the serial stream to aid the de-serializer decode the message back into a parallel bus. Electrically, the information transmitted between serializer and de-serializer was proven successful, and more importantly, asynchronously. The 50 MHz clock on the transmitting side remained isolated from the 50 MHz clock of the receiving side, meaning that the only connection between the two sides was the USB transmitting the serial stream. The asynchronous clocks between both sides was an instrumental concept for S.T.E.A.L.T.H. since both systems would be meters apart with no connection between each other, except for the optical link. The de-serializer was connected to the receiving FPGA through the latter's GPIO pins and the output displayed on that FPGA board's 4-digit 7-segment display. The setup is shown in the figure below.

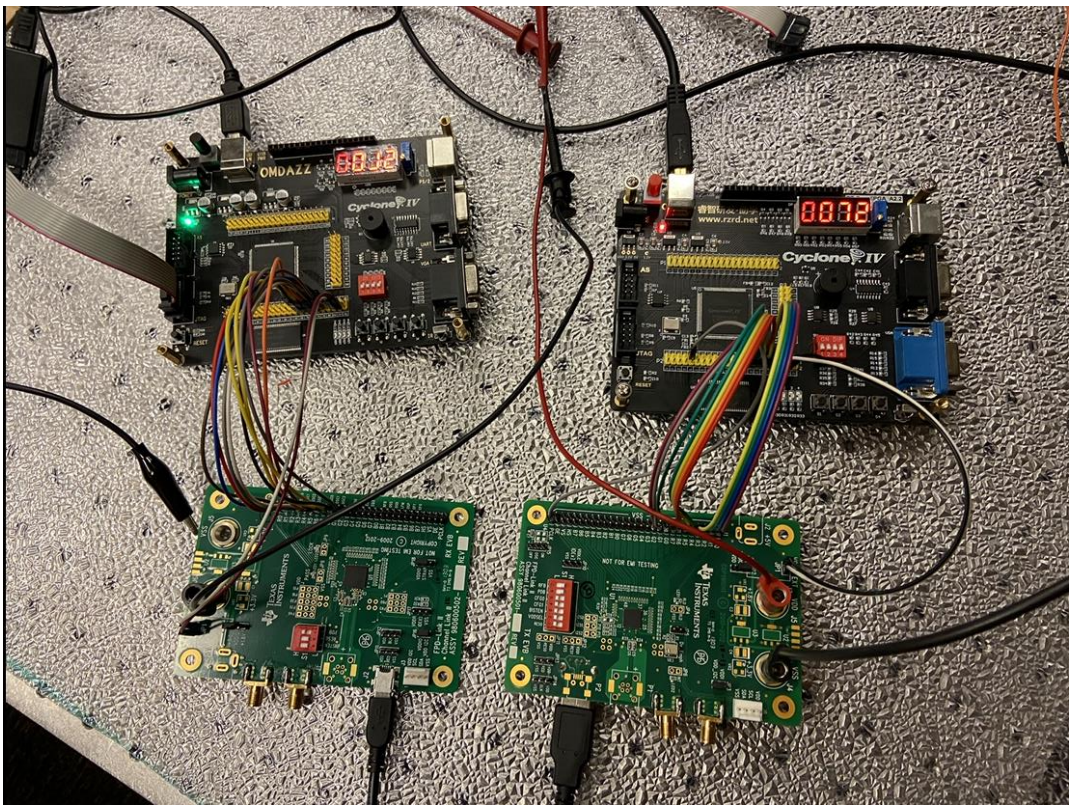



Figure 98: DS92LV242X test setup

The test program was coded using Intel's FPGA Programming software Quartus II Prime using Verilog.

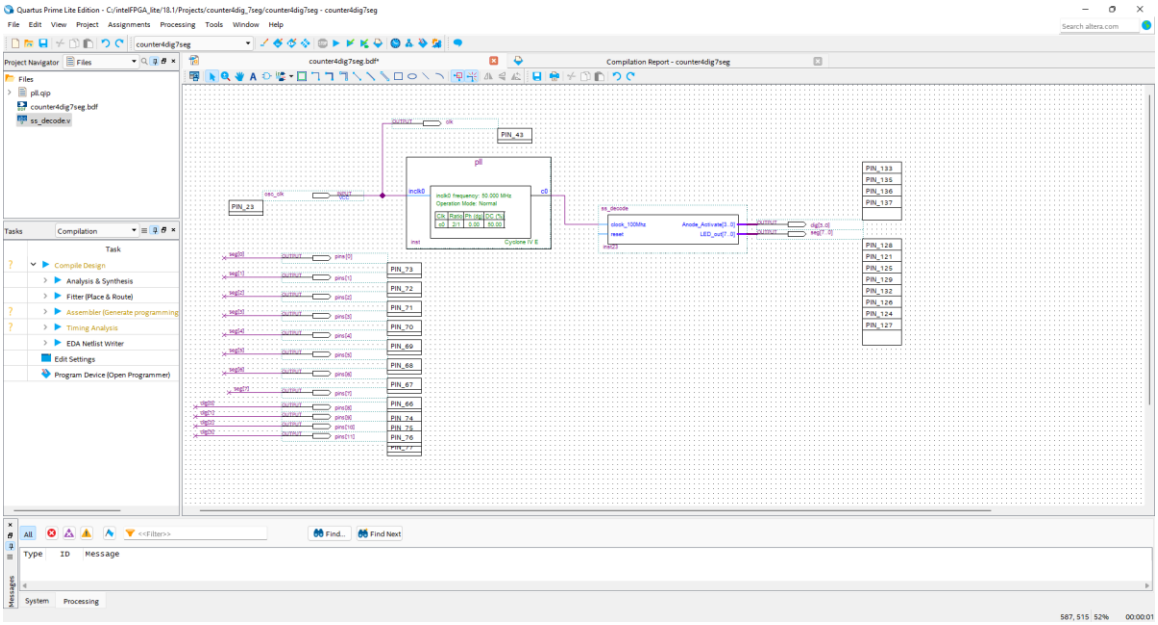


Figure 99: Quartus II block diagram for programming the Cyclone IV

A snippet of the code is shown below for the block ss_decode, which programs the 4-digit 7-segment timer counter.

```
module ss_decode(
    input clock_50Mhz,
    input reset, // reset
    output reg [3:0] Anode_Activate, // anode signals of the 7-segment LED display
    output reg [7:0] LED_out// cathode patterns of the 7-segment LED display
    );
    reg [26:0] one_second_counter; // counter for generating 1 second clock enable
    wire one_second_enable;// one second enable for counting numbers
    reg [15:0] displayed_number; // counting number to be displayed
    reg [3:0] LED_BCD;
    reg [19:0] refresh_counter
    wire [1:0] LED_activating_counter;

    always @(posedge clock_50Mhz or posedge reset)
    begin
        if(reset==1)
            one_second_counter <= 0;
        else begin
            if(one_second_counter>=99999999)
                 one_second_counter <= 0;
            else
                one_second_counter <= one_second_counter + 1;
        end
    end
    assign one_second_enable = (one_second_counter==99999999)?1:0;
    always @(posedge clock_100Mhz or posedge reset)
    begin
        if(reset==1)
            displayed_number <= 0;
        else if(one_second_enable==1)
            displayed_number <= displayed_number + 1;
    end
    always @(posedge clock_100Mhz or posedge reset)
    begin
        if(reset==1)
            refresh_counter <= 0;
        else
            refresh_counter <= refresh_counter + 1;
    end
    assign LED_activating_counter = refresh_counter[19:18];
    // anode activating signals for 4 LEDs
    // decoder to generate anode signals
    always @(*)
    begin
        case(LED_activating_counter)
        2'b00: begin
            Anode_Activate = 4'b0111;
            // activate LED1 and Deactivate LED2, LED3, LED4
            LED_BCD = displayed_number/1000;
            // the first digit of the 16-bit number
              end
        2'b01: begin
            Anode_Activate = 4'b1011;
            // activate LED2 and Deactivate LED1, LED3, LED4
            LED_BCD = (displayed_number % 1000)/100;
            // the second digit of the 16-bit number
              end
        2'b10: begin
            Anode_Activate = 4'b1101;
            // activate LED3 and Deactivate LED2, LED1, LED4
            LED_BCD = ((displayed_number % 1000)%100)/10;
            // the third digit of the 16-bit number
                end
        2'b11: begin
            Anode_Activate = 4'b1110;
            // activate LED4 and Deactivate LED2, LED3, LED1
            LED_BCD = ((displayed_number % 1000)%100)%10;
            // the fourth digit of the 16-bit number
               end
        endcase
    end
    // Cathode patterns of the 7-segment LED display
    always @(*)
    begin
        case(LED_BCD)
                                4'h0 : LED_out   <= 8'hc0; //"0"
```

```
                4'h1 : LED_out   <= 8'hf9; //"1"
                4'h2 : LED_out   <= 8'ha4; //"2"
                4'h3 : LED_out   <= 8'hb0; //"3"
                4'h4 : LED_out   <= 8'h99; //"4"
                4'h5 : LED_out   <= 8'h92; //"5"
                4'h6 : LED_out   <= 8'h82; //"6"
                4'h7 : LED_out   <= 8'hf8; //"7"
                4'h8 : LED_out   <= 8'h80; //"8"
                4'h9 : LED_out   <= 8'h90; //"9"
                4'ha : LED_out   <= 8'h88; //"a"
                4'hb : LED_out   <= 8'h83; //"b"
                4'hc : LED_out   <= 8'hc6; //"c"
                4'hd : LED_out   <= 8'ha1; //"d"
                4'he : LED_out   <= 8'h86; //"e"
                4'hf : LED_out   <= 8'h8e; //"f"
                default LED_out  <= 8'hff;
        endcase
    end
endmodule
```

As shown in the figure above, the choice of the DS92LV2421 and DS92LV2422 serializer and de-serializer pair was the correct one, since both FPGAs show the same timer value with no delay between transitions while remaining asynchronous systems.

# 9.2.2.1 Follow-Up Testing

After some major mishaps with the equipment during previous testing which are discussed in other sections, the team continued testing the system by optically transmitting a message over the laser and recovering the signal on an oscilloscope. The images below show a comparison between the transmitted message's waveform and the received message's waveform. The signal was transmitted across the room of the undergraduate lab of the CREOL building. Amplitude of the signal is lowered, but due to the laser driver procured arriving late, the modulation depth provided by it was not as expected, so that could be a reason for the loss of amplitude in the wave.

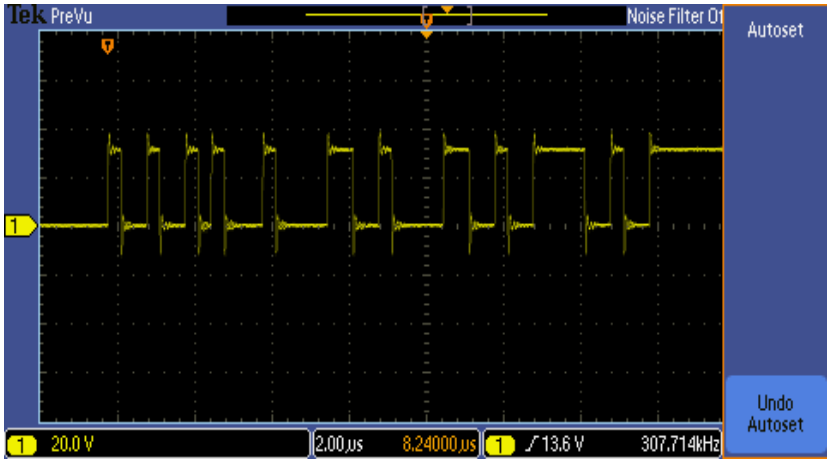



Figure 100: Transmitted signal message waveform

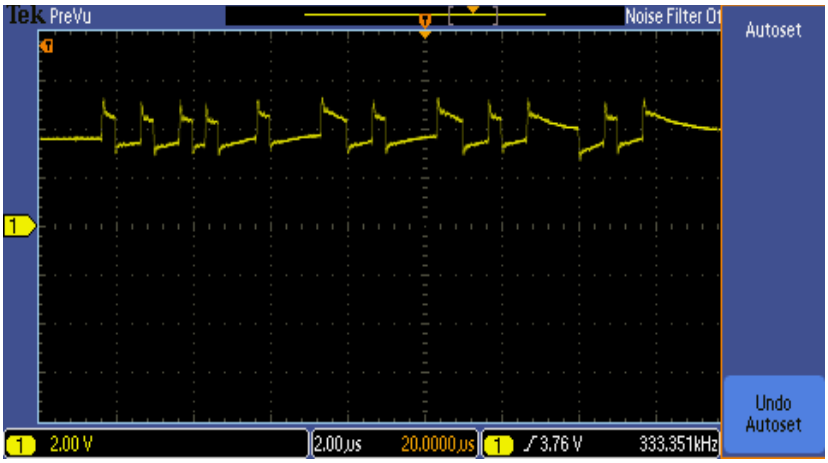


Figure 101: Received signal message waveform

# 9.2.3 Computer Testing Mishaps

The signal between the serializer and de-serializer could not be achieved optically, so no testing results were able to be gathered by the team. This was an issue that was tested extensively to try to pinpoint a cause, and any possible solutions. One of the main culprits for the signal not being recovered by the receiving FPGA was due to the major loss of amplitude in the signal as it travel optically, as discussed in section 9.2.2.1. Again, after many design changes in the electrical power and optical designs due to limited part availability, the laser driver board that was procured did not provide modulation like the team was expecting it to, and as a result it inhibited a successful recovery of the signal in the receiving side.

To circumvent this issue, the team decided to amplify the signal coming from the photodetector and into the de-serializer, the team designed an operational amplifier found in the undergraduate lab. After many tests performed, signal would still not be able to be recovered. One of the

Continued testing with the operational amplifier lead to one of the major issues that hindered any possibility of establishing a successful transmission of data any further. The operational amplifier's supply voltage range used was +18V and -18V for the positive and negative supplies, respectively. The supply voltage needed for the serializer and de-serializer was of +1.8V, which was provided externally, as well as +3.3V provided by the FPGA. In between setting up tests, a voltage of +18V was **accidentally** provided to the de-serializer board, 10 times the range of its rating. Needless to say, the board was no longer functioning as of 04/25/2022, since the power supply used was showing that the voltage provided was actually sinking to ground. Video evidence is shown in the final hardware demo. Apart from being way over budget as it is, the lead times for procuring a new board were of 4 weeks, so it was impossible to obtain a new board and continue testing.

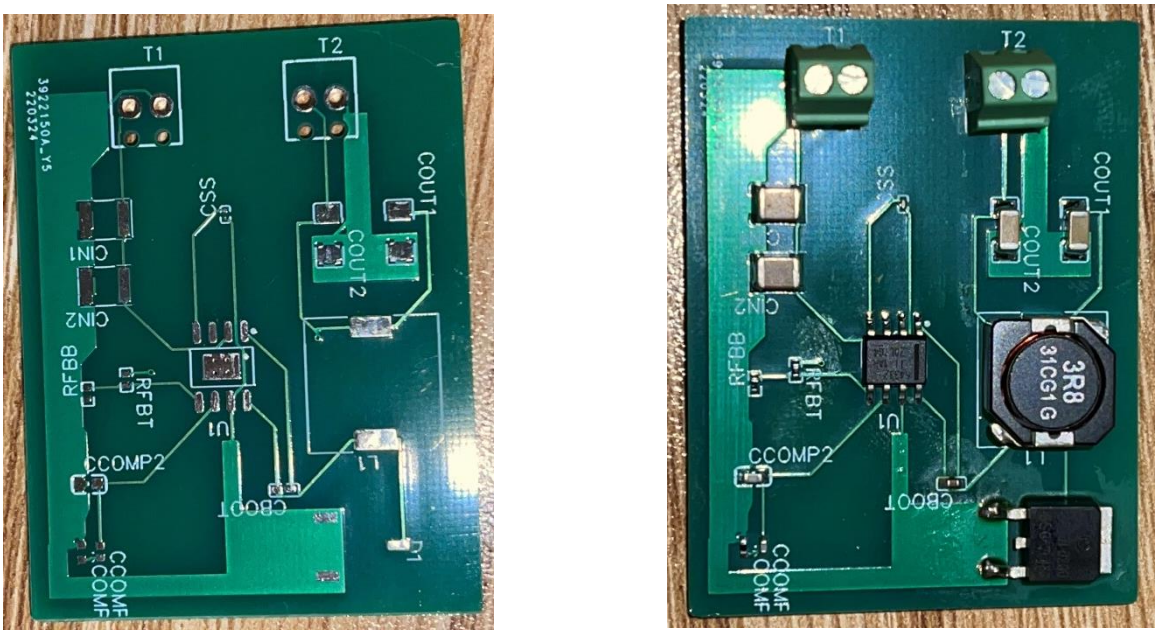
For this reason, the optical link was tested and demonstrated with an analog connection, because power designs were made to work with the DS92LV242X system's power input/outputs in mind, and the fact that recovery was just not being registered on the optical link to begin with.

# 9.3 Electrical

In this section the team will discuss the updates made to the progress throughout the senior design two semester. The team went through a roller coaster of successes and failures but at the end we delivered a functioning proof of concept with all of the systems working separately but during integration into one prototype some unforeseen challenges were met. The following sections will outline those challenges and how we overcame them.

## 9.3.1 Prototype Construction

In this section we will showcase the different power distribution and amplification systems used to create our final prototype through chronological order. Firstly, to showcase the designed power management PCB's shown in the below figures.




**Figures 102 & 103:** Designed Power Supply PCB No.1

In the figures above we see the un-assembled and assembled power supply PCB for the laser driver and TEC control board. As well as the FPGA power supply.This was designed in Easy EDA, the free PCB design software. I found this software the most user friendly that I was able to easily understand and efficiently design and test my circuit. In the figures below showcases the proof that this board functions as designed, but unfortunately due to late-stage design changes this board became nonapplicable to the project as the laser driver board acquired we

learned that it requires +5Vdc and -5Vdc. During testing we tried to supply power to the board using two of these boards as one would do with a power supply. In doing this one of the boards back fed into the other board and fried the buck converter. This board also wasn't the best applicable solution for the FPGA as it can be powered with 5Vdc, but it would have to be through the USB port on the board. As this would have resulted in a less than desirable appearance and not very sturdy construction through the use of a USB PIN out converter, we opted for another solution discussed later.

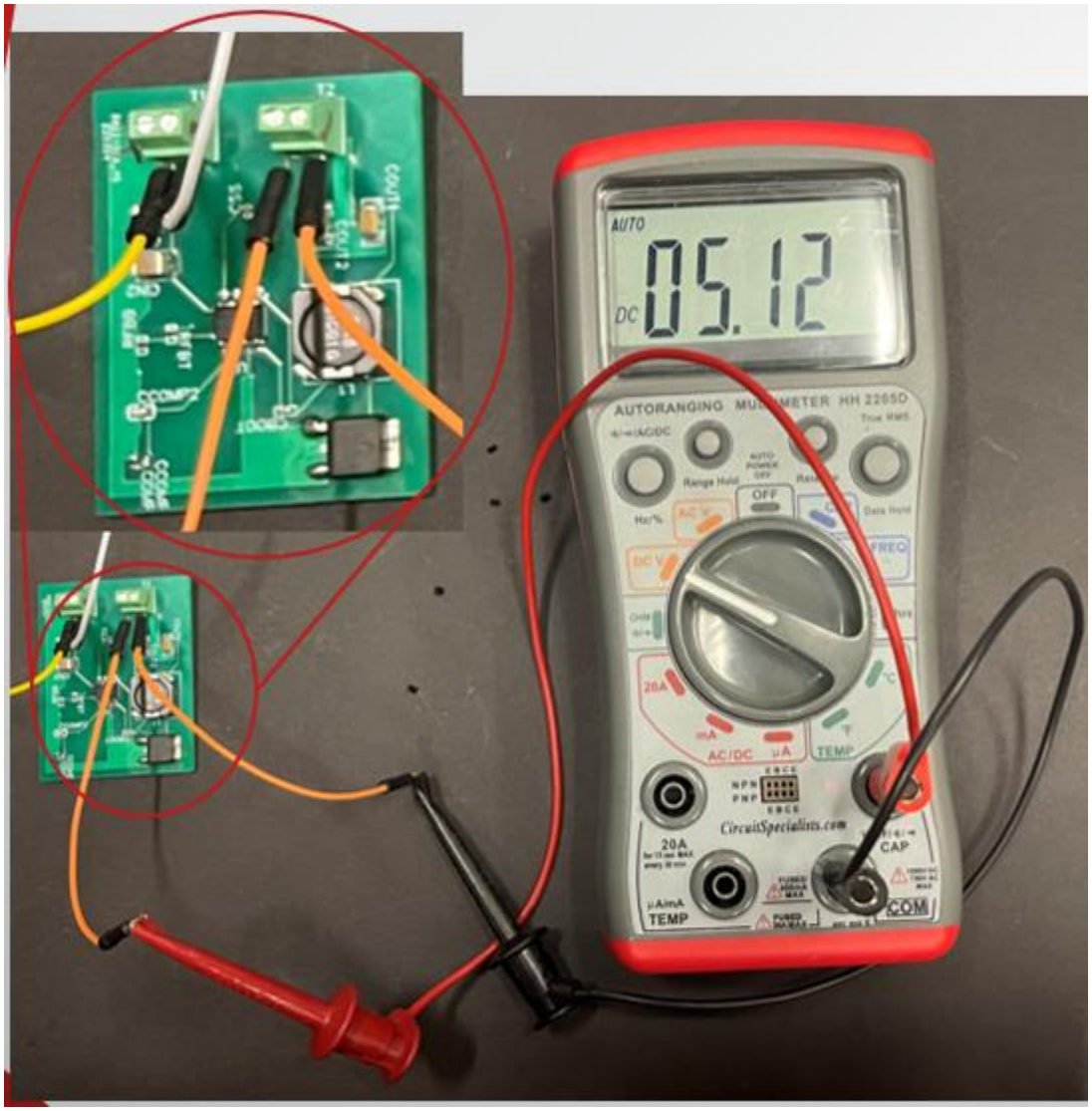
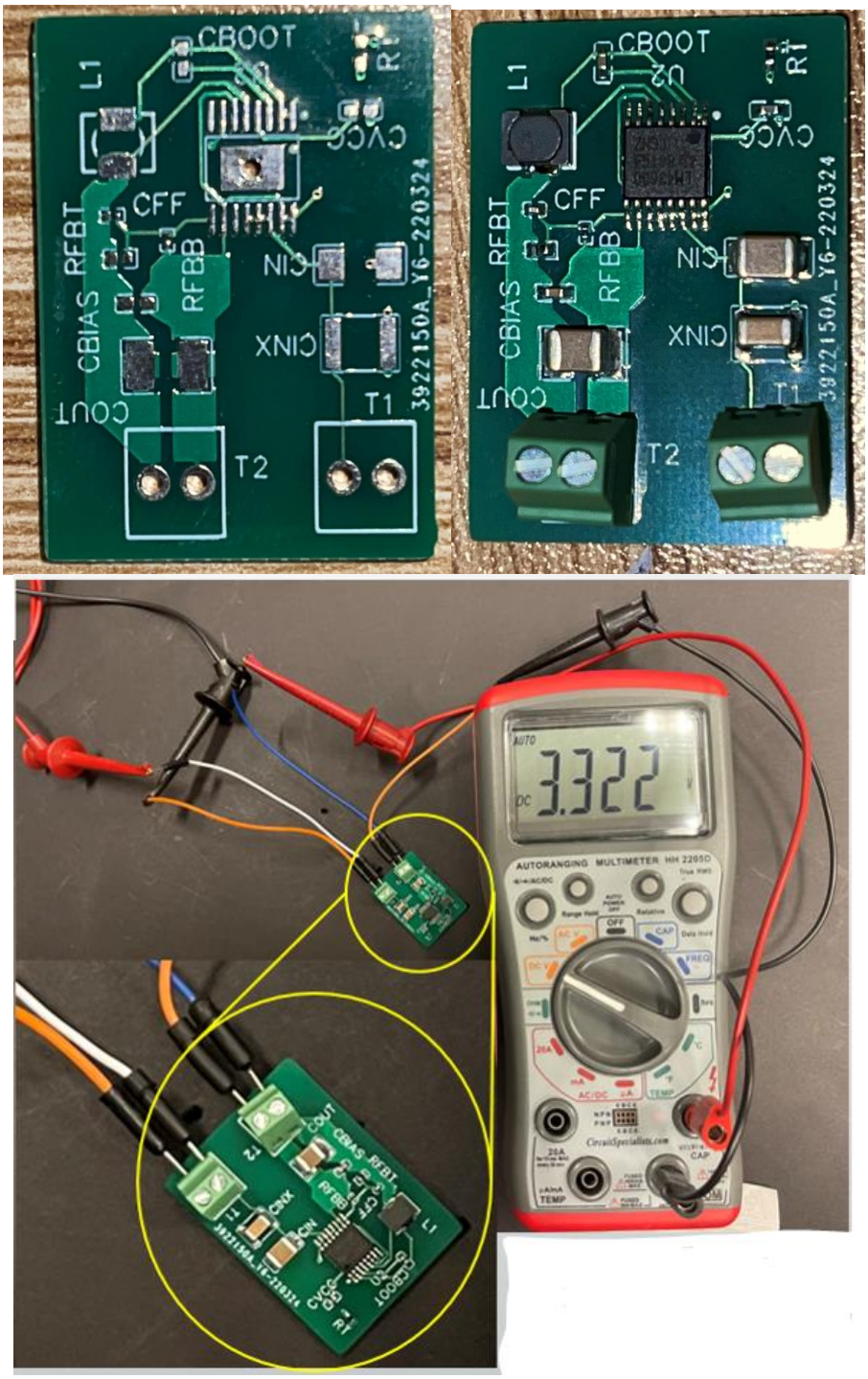



**Figure 104:** Designed Power Supply PCB No.1 Functionality

Next we showcase the power supply of the serializer and deserializer. This board was also designed in Easy EDA. This board also functioned as designed, but due to multiple challenges was also nonapplicable to the design. The first challenge was a miscommunication between team members where it was thought to be supplied with 3.3Vdc to operate. It turns out that the development boards that were

acquired required 1.8Vdc to operate. In the three figures below you will see the unassembled, assembled, and proof of operation of this board.




**Figures 105, 106, & 107:** Designed Power Supply PCB No.2

To properly secure the power supply PCBs, two 3D housings were created. The design was very straight forward. The housings needed to hold the PCBs in a

way that allowed them to be easily accessible, while keeping the sensitive elements protected, as shown the Figures below.

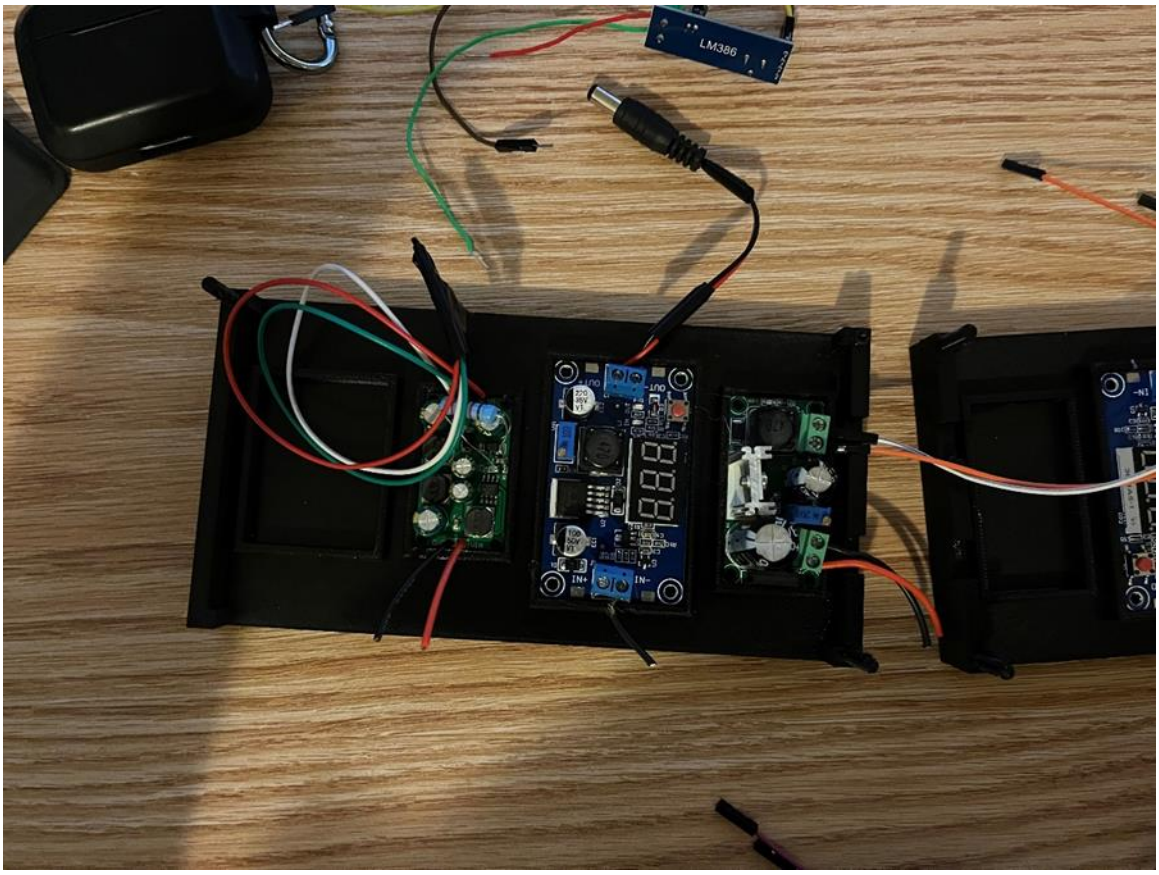



**Figure 108:** Bottom Half of Power Supply PCB housing

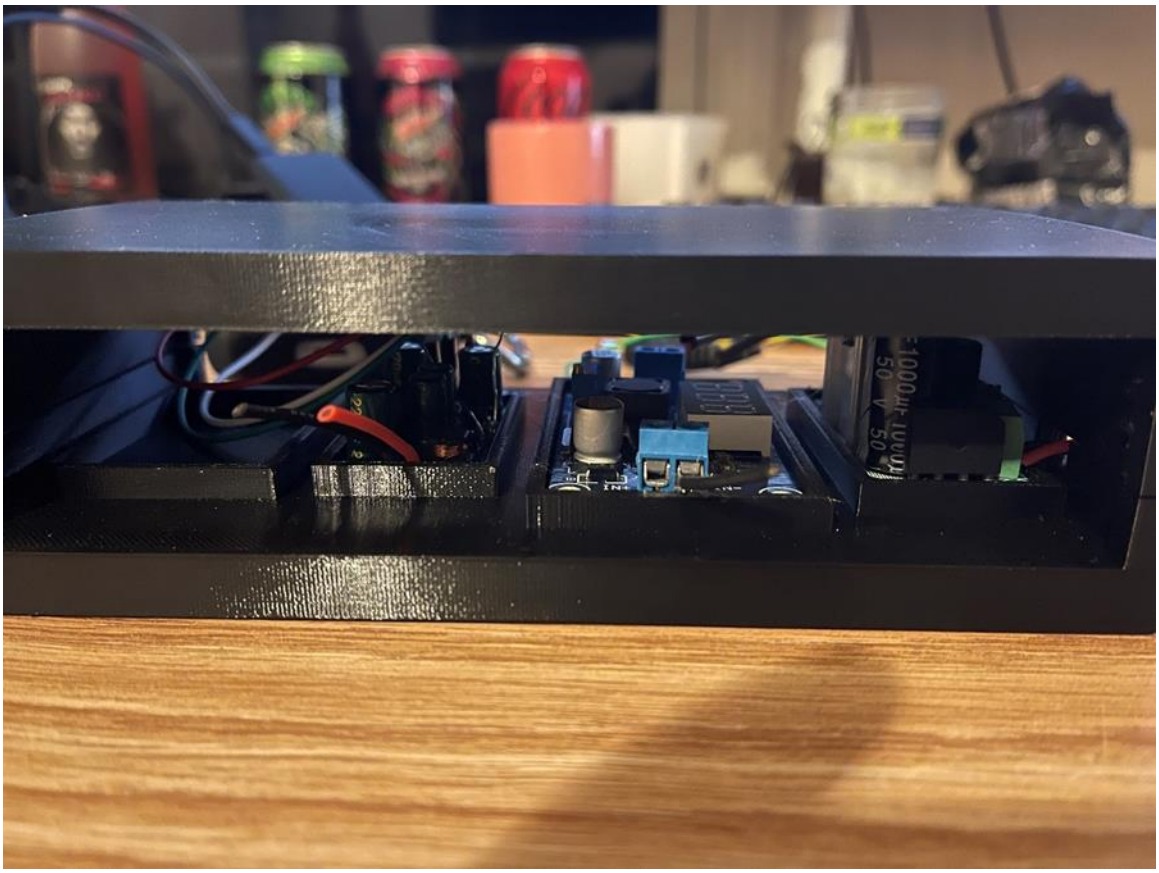
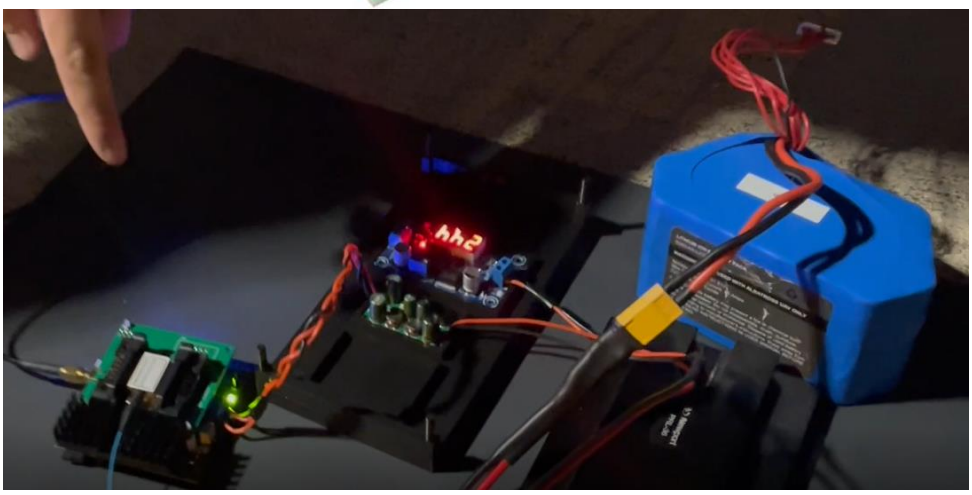



**Figure 109:** Fully Assembled Power Supply PCB housing

# 9.3.2 Project Operation

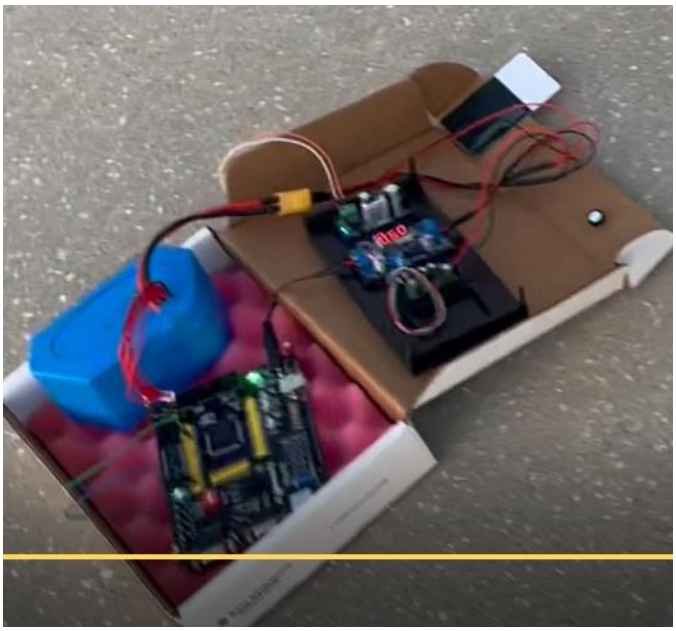
Finally, in this section we will discuss the boards that were acquired in short notice as to enable the project function on battery power as specified. I did not want to hinder the group members due to the failing of some components, so I did what all engineers worth their salt would do. Regrouped, found parts that would work, and rectified the design for successful operation.

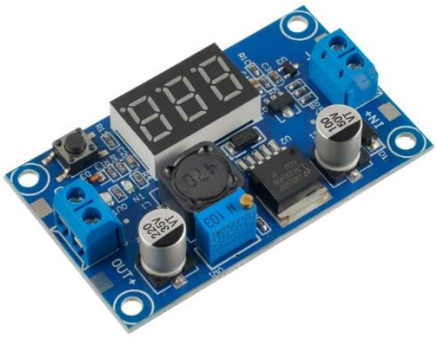
The first solution to be rectified was to power the laser driver board. In doing some research I was able to find a board that supplied both +5 and -5Vdc. Realizing the boards I had would not work I did some research on why and came to found that these voltages need to share a reference ground (0Vdc). If they do not, the error I had occurs. There are many circuits that can do this but due to time constraints ordering the components required would have taken too long. So that was out of the picture. Next was to try to and find some premanufactured boards that would arrive quickly. The following board was found. Below you will see the board showcased in some application use. As well seen in the 3D printed housing in the optics section 9.

**Figures 110 & 111:** Procured Laser Driver and TEC Power Supply

The next challenge that was overcome was the power supply to the FPGA, this was accomplished in a neater fashion with a acquired PCB as well. This specific PCB was a good technology find, as this board has a potentiometer that adjusts the output voltage. My strong background in circuits assumes this is accomplished through a voltage divider or an adjustable buck converter. This PCB can be seen below as well as a shot of it in action.





**Figures 112 & 113:** FPGA Power Supply

There were some miscellaneous loads that also needed power for our final demonstration such as the audio amplifier and the USB powered speakers. This was achieved by the aforementioned boards due to their adjustable output voltages. Some examples of this are shown below.

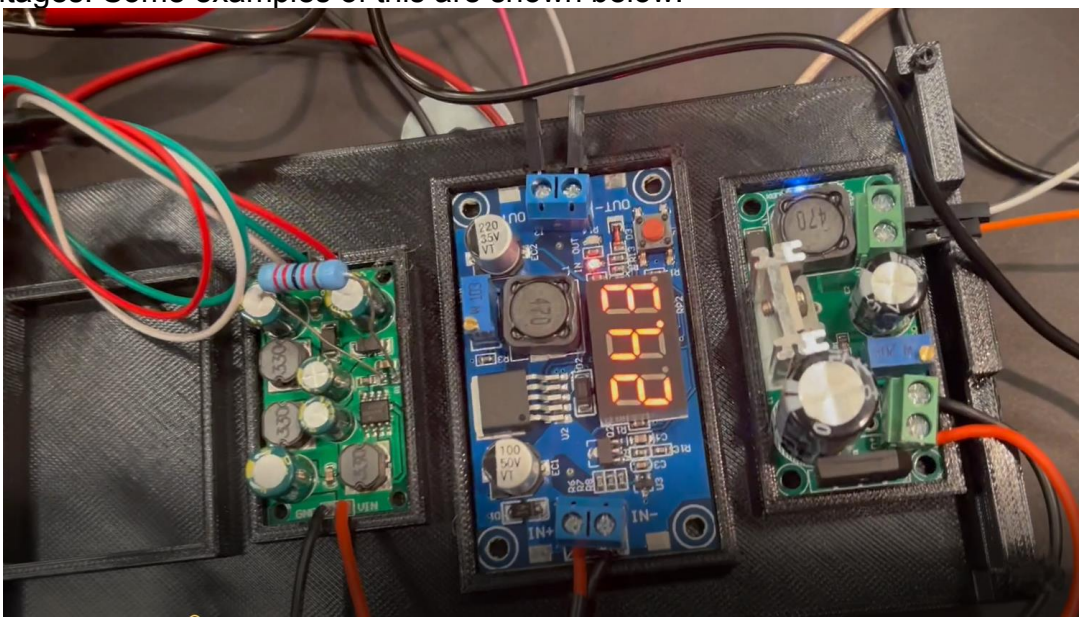


**Figure 114:** Power Supply Boards and Housing

# 10.0 Project Summary and Conclusions

This section of the report will provide a summary of the S.T.E.A.L.T.H. system, the difficulties that the team faced, as well as the successes, and any conclusions the team had after working on this project for the academic year.

One of the requirements set by the team for this project was sending a signal at a transmission speed of 1Gbps or faster. After the discussion of section 9.2 and its subsections of this document, the hardware procured for the computing subsystem of S.T.E.A.L.T.H. proved to be adequate to achieve this requirement. By connecting the serializer and de-serializer pair directly through the USB operation was as expected and performed well. The issue that arose and the team could not overcome was the fact that over the optical link, the amplitude of the wave is severely decreased. Even when trying to amplify the signal, the wave's shape is distorted and lost, so recovery of the signal proved to be incredibly difficult. At the start of this project, this was expected to cause issues, but the issues that the team were expecting were related to the asynchronous nature of the project. How would the receiving side of the system be able to decode when a message starts and stops? That question was something the team tried to answer. By using the DS92LV242X, however, the team proved that the only connection required by those two chips are the serial stream of data, and it successfully is able to decode the message accurately while remaining asynchronous. The laser driver that was procured did not provide modulation like it was expected to, so that hindered any signal recovery efforts significantly. The biggest issue in delivering a final working product for the computing subsystem, however, was the powering mishap that was discussed in Section 9.2.3, which detailed how the de-serializer board was taken out of commission by accidentally being fed a voltage level 10 times larger than the absolute maximum rating detailed by the datasheet. In any case, the biggest lesson learned from Senior Design would be to triple-check the voltage levels being selected on the power supplies before connecting anything and turning the supply on.

In conclusion this senior design experience was a great insight on how engineers need to be problem solvers. Electrically speaking when working with other disciplines you are constantly dealing with change. In this change you either need to be the last to start, or flexible. In hindsight I should have designed my power supply boards to be adjustable as this would have solved a majority of our issues electrically. As the senior design experience progressed through the semesters, I realized how lucky I was to have great team members. Even through challenges we were able to band together and be solve them in good spirits, there were never tense or challenging moments between us. The best engineer can accomplish great things, but a good team of engineers can solve any problem.

# Appendix A

# References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# Appendix B

# Software

The software used for this project was Intel Quartus II Prime, which was used to program the FPGA Cyclone IV. A free version is available on Intel's website. A link to download the program has been added to the Group 5 website in case the reader is interested in acquiring it. The project files the team developed have also been added to the website.