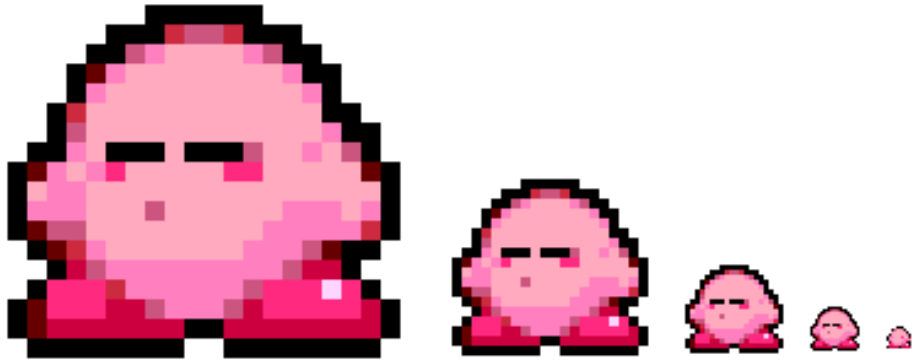
The Super Doubler

Group 31



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Motivation

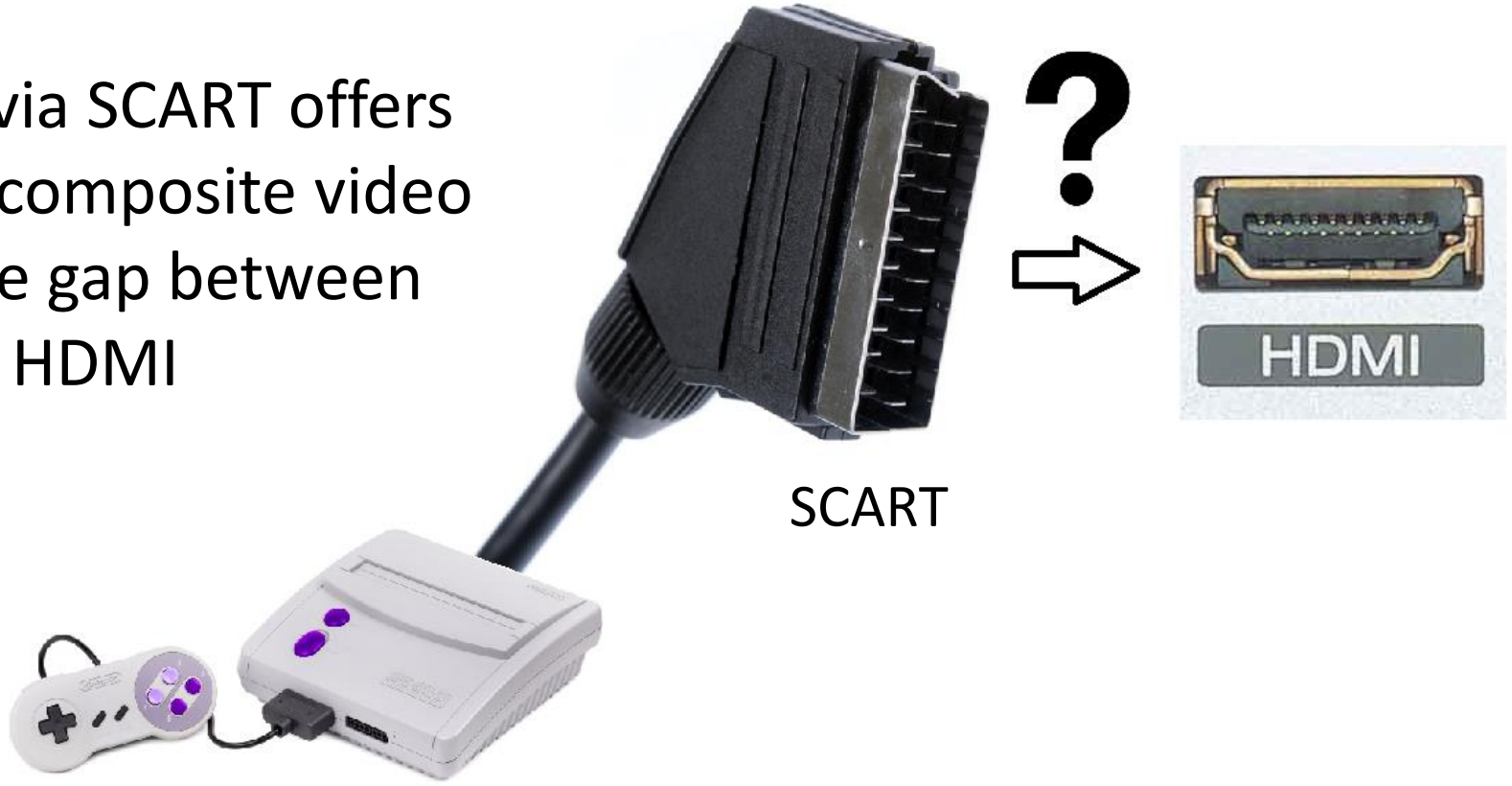
- Digital TVs have limited analog video support
- Typically only support composite video
- Situation will worsen with time

Analog video (240p) processed by a digital TV

Analog video (240p) on a digital TV with a video pre-processor

Video System Compatibility

- Using RGB video output via SCART offers large improvement over composite video
- Need device to bridge the gap between analog SCART and digital HDMI



SCART

XRGB mini- Framemeister

Features of the Framemeister

- Improved 240p handling
- Supports SCART
- Fine grain control of image settings

Flaws of the Framemeister

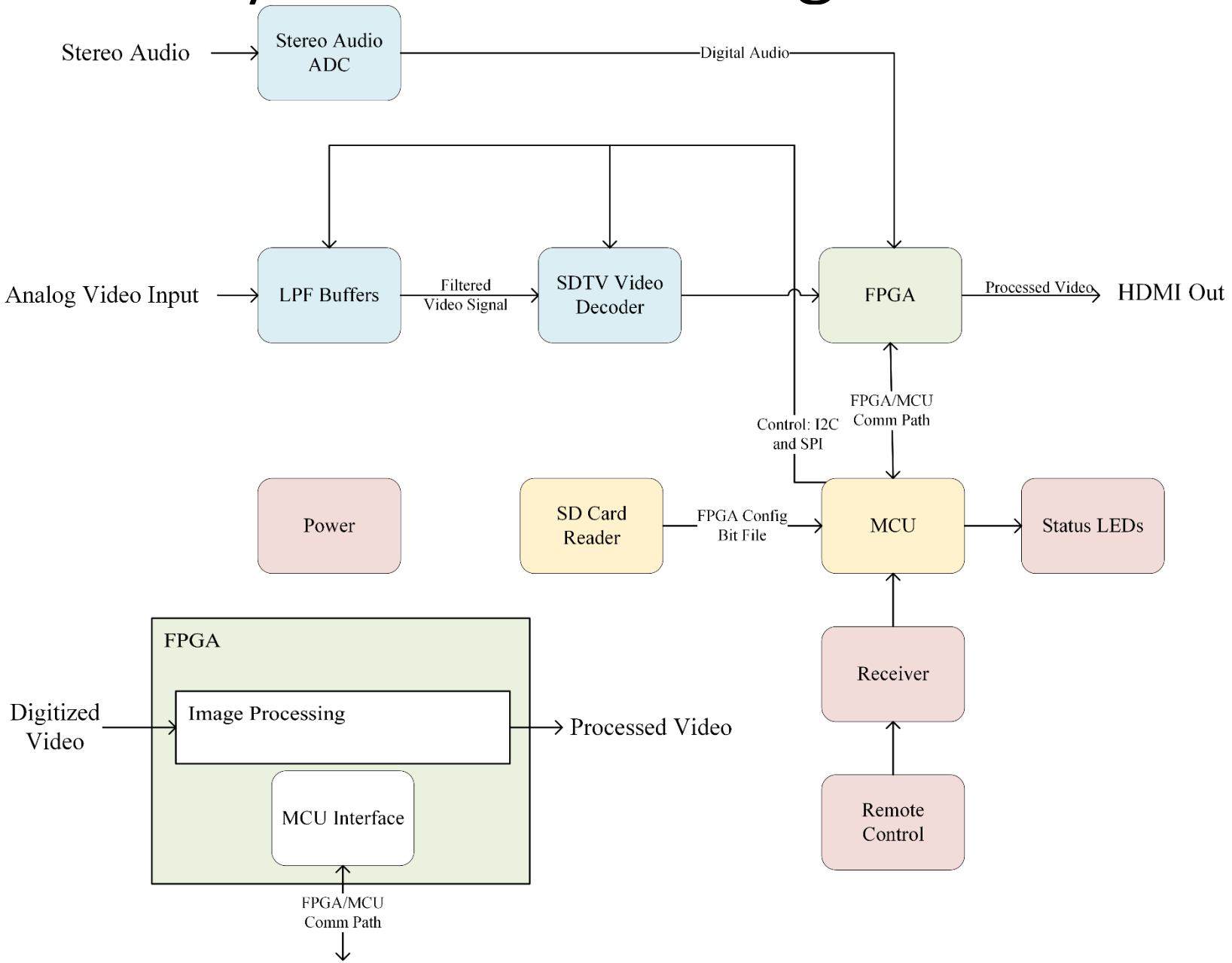
- No dedicated line double mode
- Results in higher latency
- 240p <-> 480i mode switch time
- $340 shipped

The Super Doubler

- Low cost high-speed scaling device
- Versatile input selection
- Digital audio/video via HDMI output
- Fills gap between cheap scalers and Framemeister
- FPGA video scaling hardware design can be updated via SD card

Requirements
Scaling factor ≥ 2
BOM $\leq$ $150
FPGA block latency < 28ms
240p <-> 480i mode switch < 33ms
Supported input: VGA, SCART, component, s-video

System Block Diagram

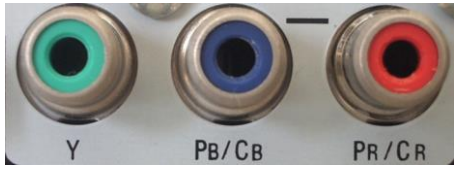


Input Signals

- Wide input selection
- Support most common retro consoles
  - SEGA Genesis – SCART
  - SEGA Dreamcast – VGA
  - Nintendo 64 – S-Video
  - etc…

SCART (RGB)

COMPONENT(YPbPr)



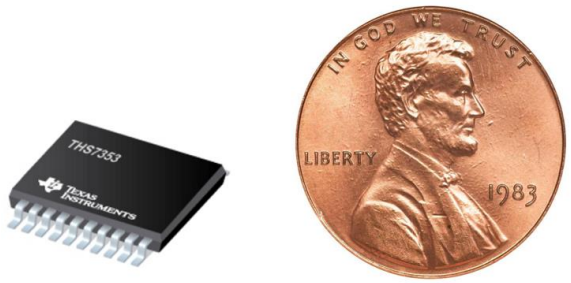
VGA

S-VIDEO

Input Video Filtering

- 2 3-Channel Input Low Power Video Amp with I2C Control
  - Channels individually configurable

- 5th Order Butterworth Characteristics
  - Configurable cutoff frequency



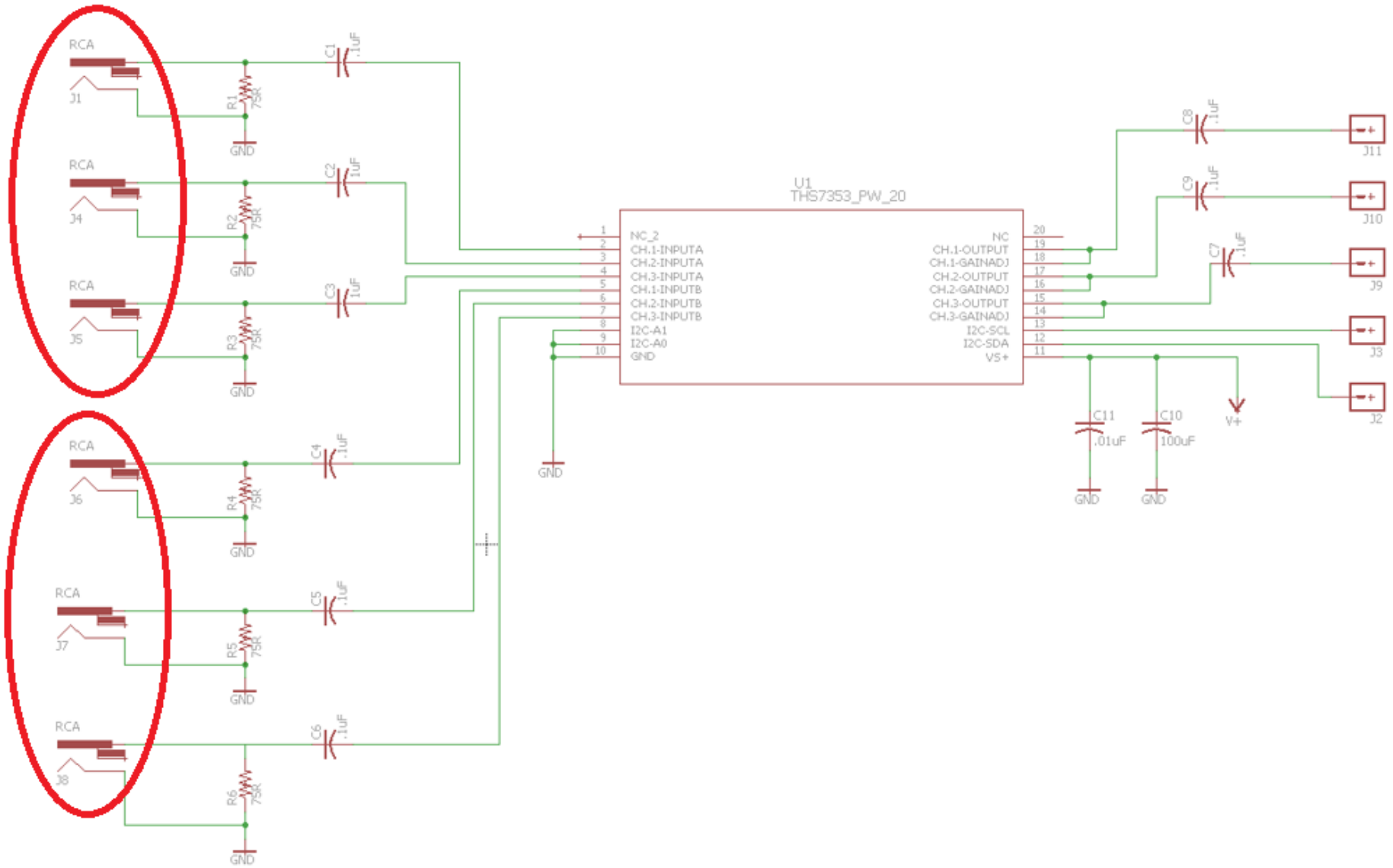
Texas Instruments - THS7353

THS7353 Low pass filter	
Device Control Method	I2C (Individually configurable)
Number of channels	3
Gain(dB)	Adjustable
Size	4.4 x 6.5 ~ 42 mm^2
Price	$1.49

THS7353 – Schematic

Component

SCART/VGA



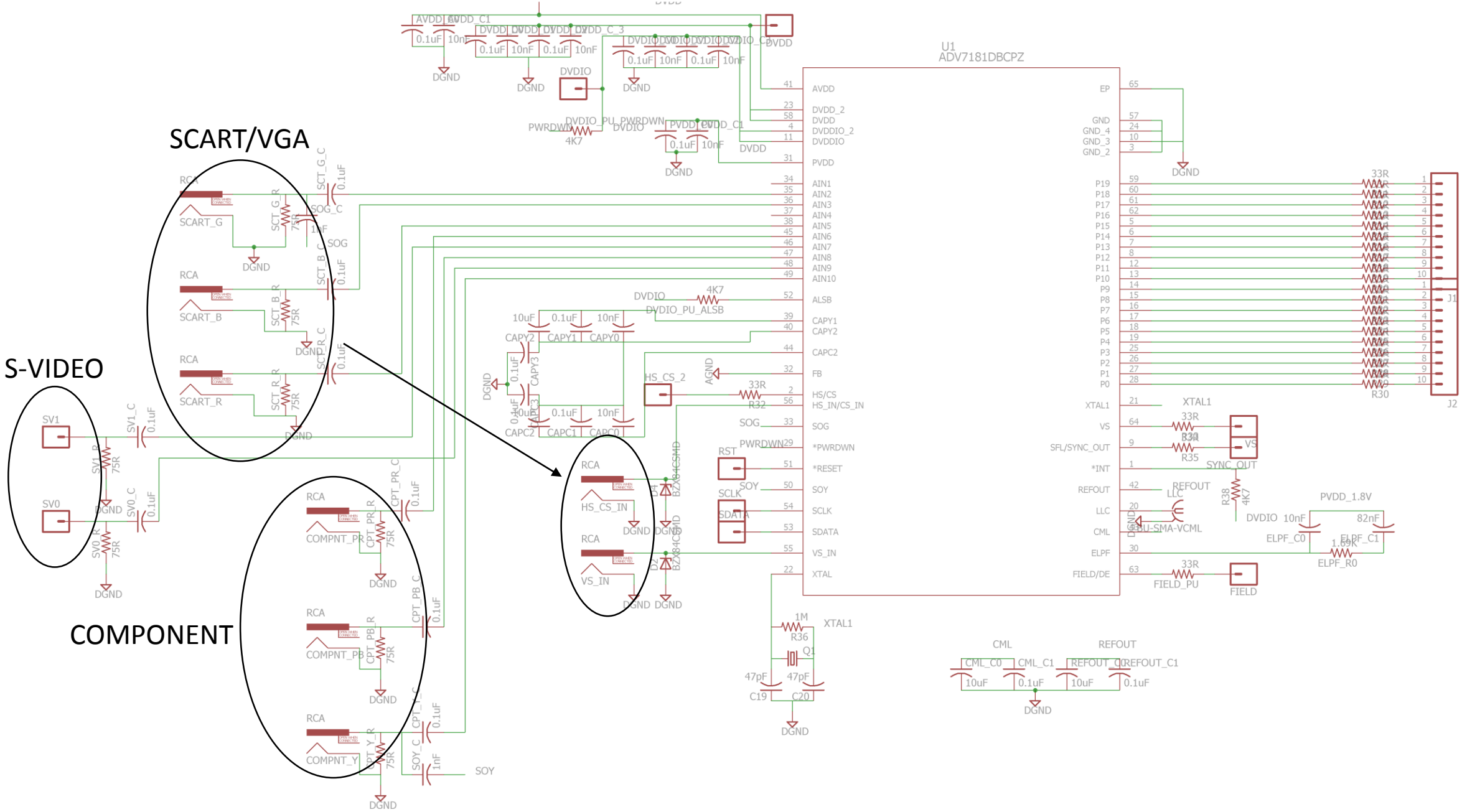
ADV7181 - Video Decoder

- Detects and converts analog video signals to digital format
- Compatibility with various video standards – NTSC, PAL and SECAM
- Six analog video input channels
- Accepts: SCART (RGB), Component (YPbPr), S-Video and VGA video signals
- Video decoding and conversion in line-locked clock-based systems

ADV7181 Video decoder

ADV7181	
Family	Interface - Encoders, Decoders, Converters
Cost	$12.51
Category	Integrated Circuits (ICs)
Voltage - Supply, Analog	3.15 V ~ 3.45 V
Voltage - Supply, Digital	1.65 V ~ 2 V
Package / Case	64-LFCSP (9mm x 9mm)

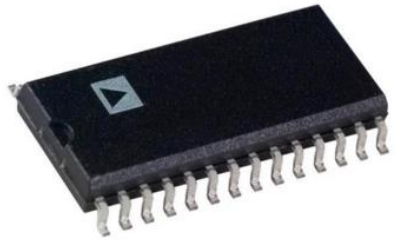
ADV7181 – Inputs



AD1871 – Audio Decoder

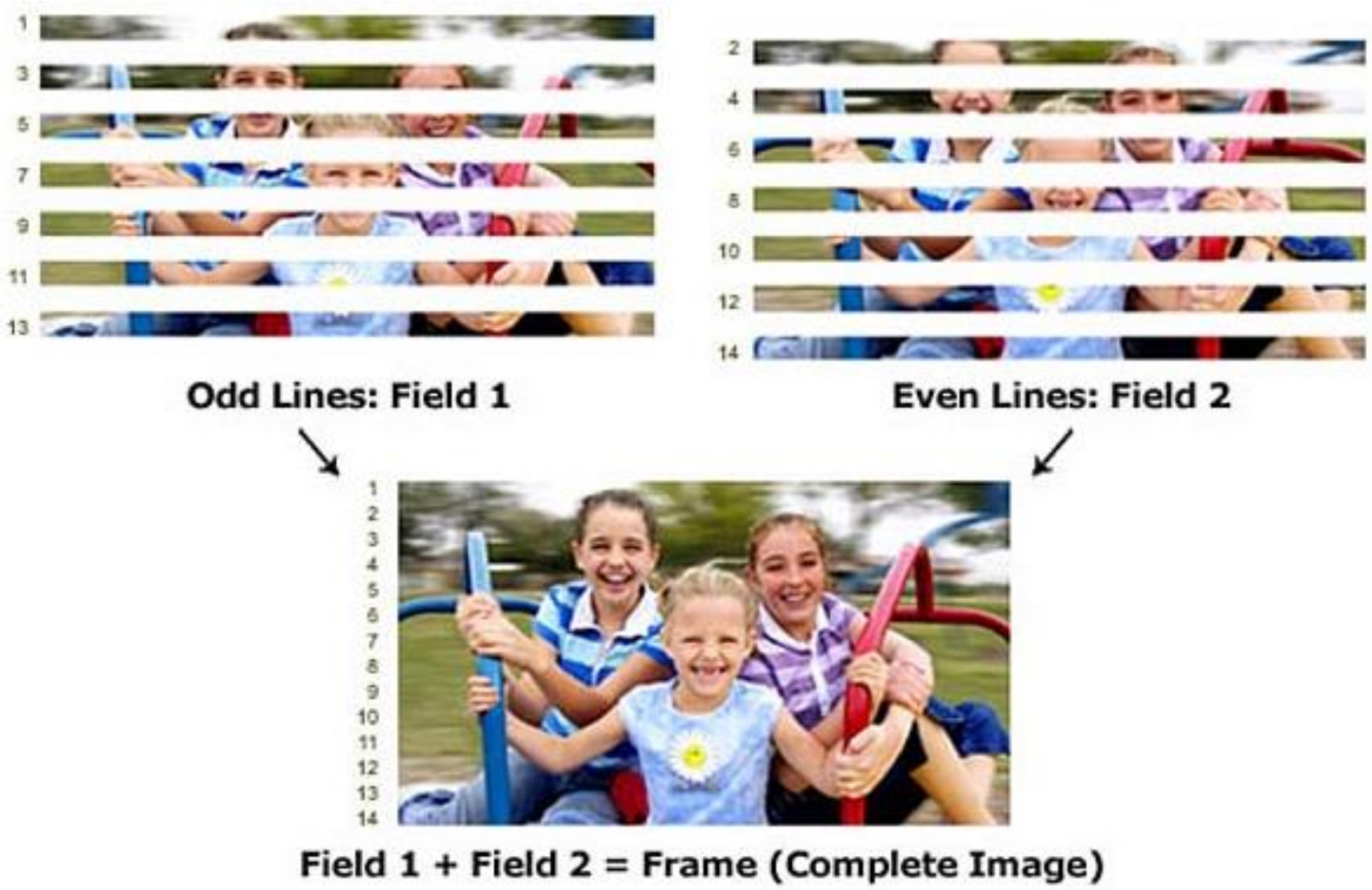
- 5.0 V Stereo Audio ADC
- Supports 96 kHz Sample Rate
- I2S audio data interface support
- Programmable-Gain Amplifier
- SPI compatible serial control port

AD1871	
Family	Data Acquisition - ADCs/DACs - Special Purpose
Cost	$10.27
Mounting Type	Surface Mount
Package / Case	28-SSOP (10.50 x 8.20 mm)
Resolution	24 bits
Data Interface	SPI



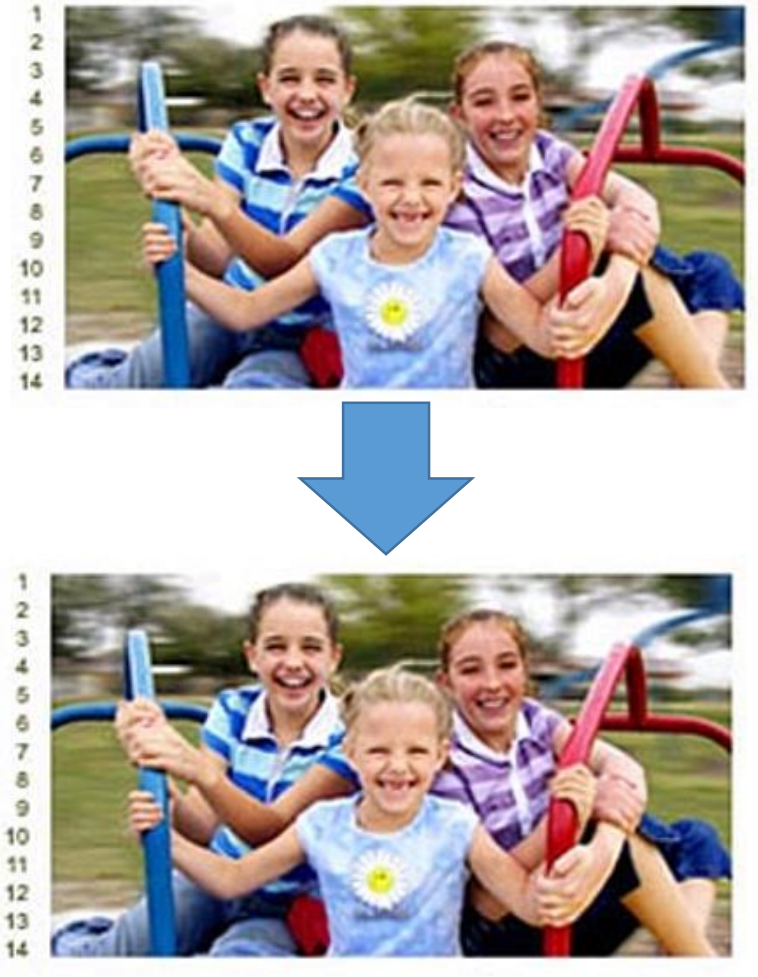
AD1871 – Audio decoder

Scan type - Interlaced

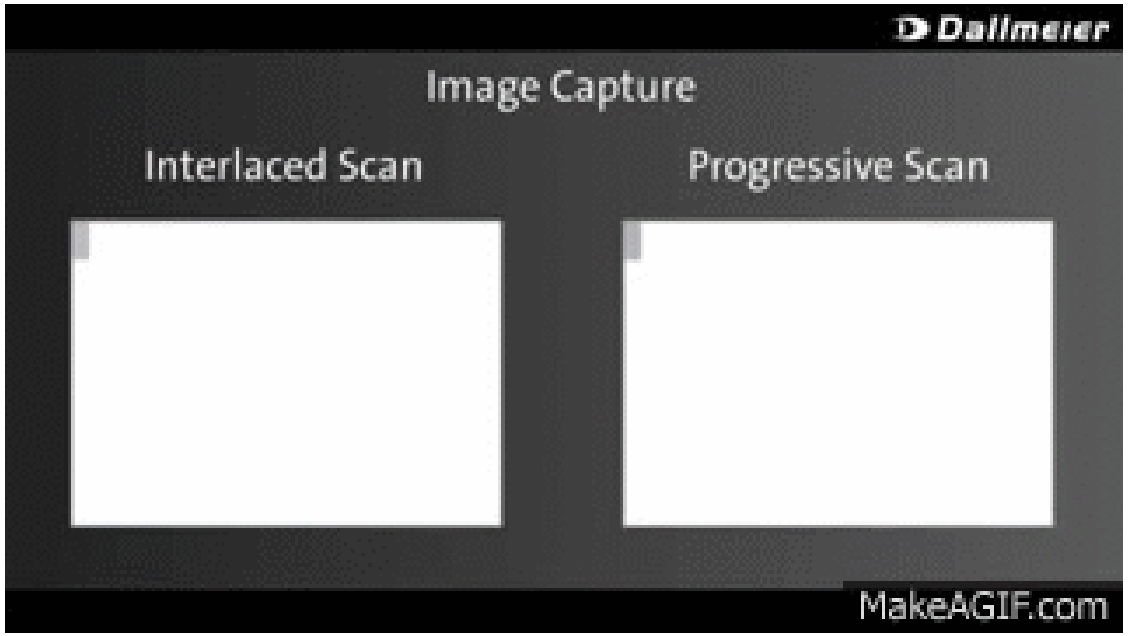


Scan type - Progressive

- Single field contains the entire frame
- 1 Field = 1 Frame
- New “Fixed resolution” displays (such as LCD, LED) all use progressive scan.



Interlaced versus Progressive

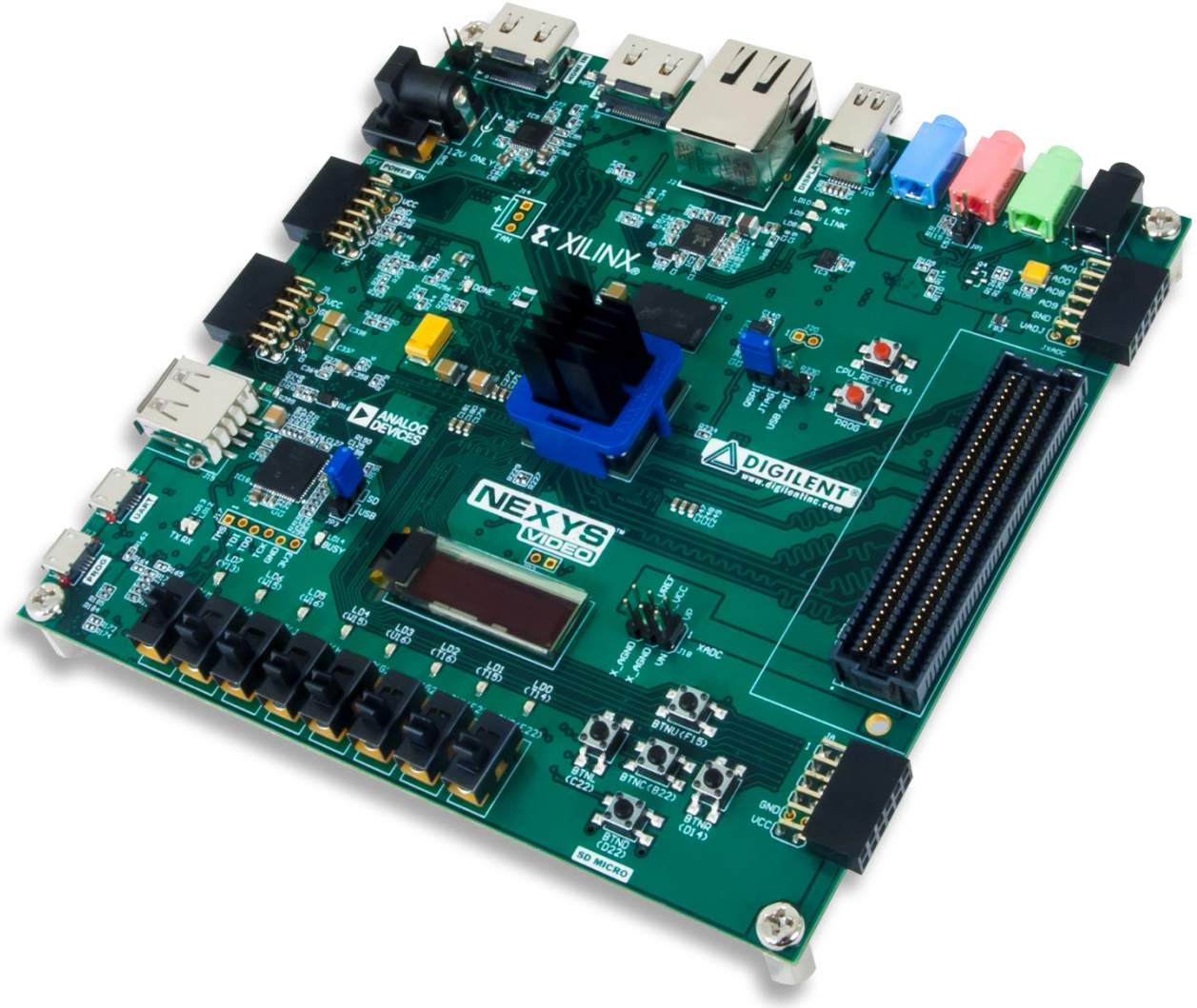


FPGA Audio/Video Processing Unit

- Xilinx Artix-7 FPGA Family
  - Low-cost FPGA giving access to latest tools
  - Wide range of devices to choose from
- Verilog HDL
- Vivado Design software
- Performs video scaling
- Manages digital audio data

FPGA Family	Artix-7
Cost	$32.13 - $251.25
FPGA Package	Various BGA
Logic Slices	2,600 - 33,650
Block Memory	900Kb – 13.14Mb
PLL	5 - 10

Nexys Video FPGA Development Board



- HDMI Output (1080p capable)
- “Bare metal” HDMI pin access
- Large number of high-speed I/O
- LPC FPGA Mezzanine Connector (FMC)

FPGA	**Artix-7** XC7A200T
Cost	$320
Size	5.25in x 5.50in
FPGA Package	484-BBGA
Logic Slices	33,650
Block Memory	13 Mbits
PLL	10

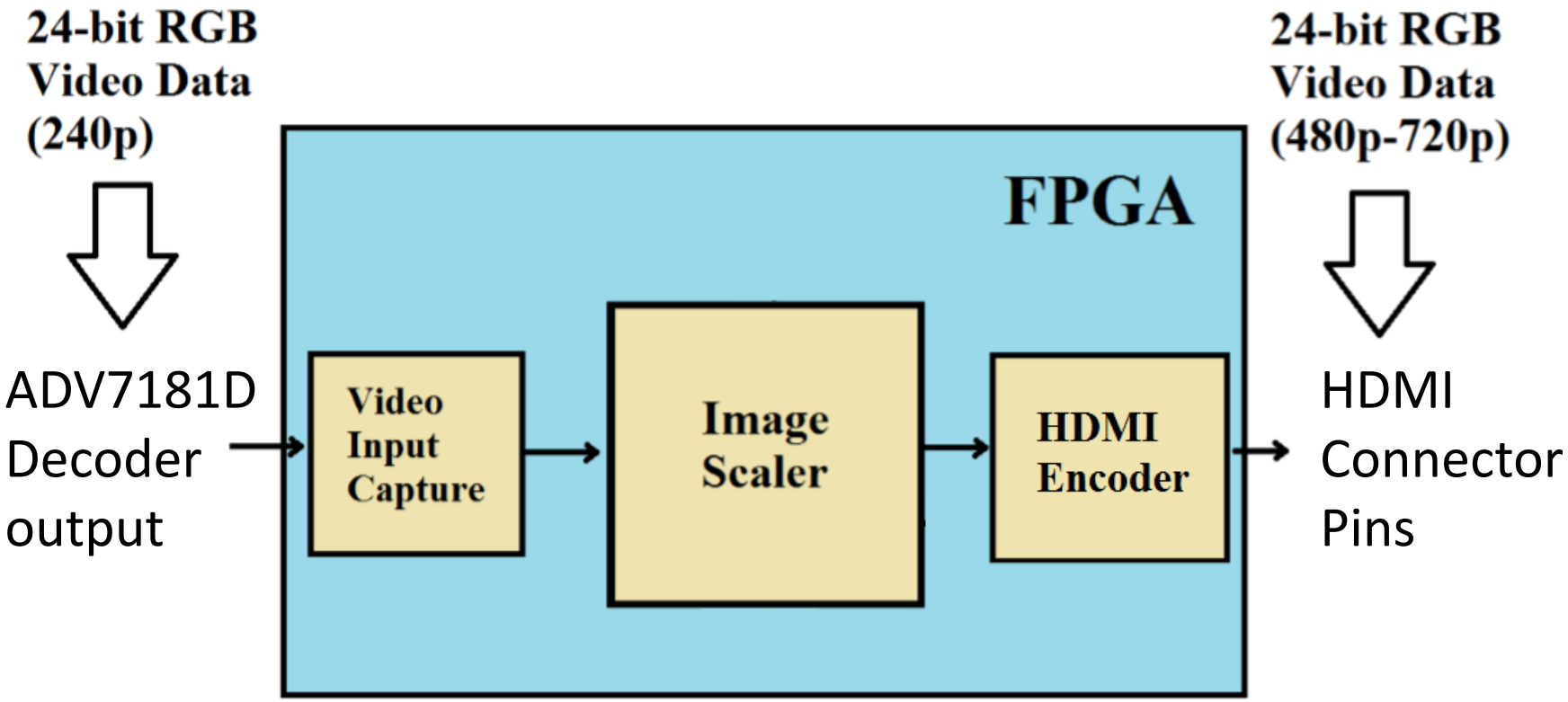
FMC I/O Access

XM105 Debug Card

- Gives access to FPGA FMC I/O
- Dedicated clock I/O
- Supports multiple I/O standards
- Signal breakout for debugging

Cost	$182.50
Size	4.50in x 2.75in
I/O	68 accessible
Oscillator	Si570, 10 – 945MHz

FPGA Block Diagram



Video Formatting

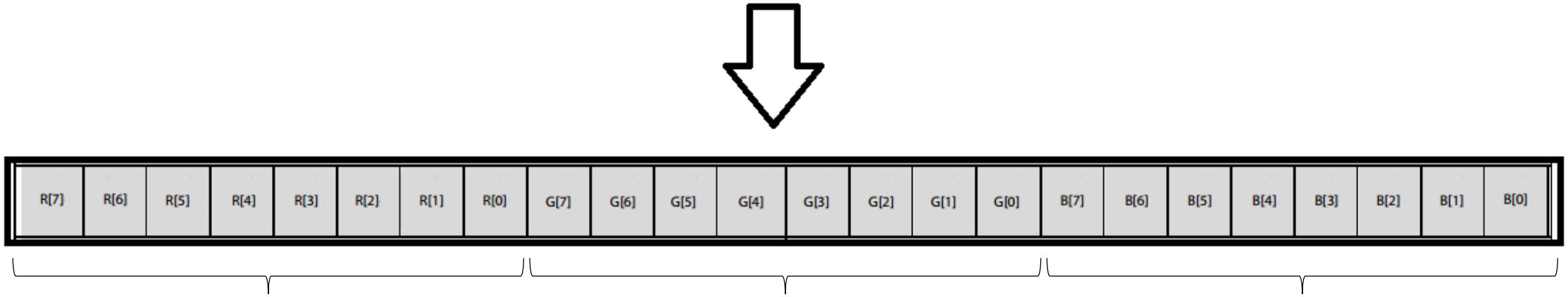
- FPGA receives video data in 12-bit RGB DDR format
- FPGA needs to reorder data before scaling

Processor, Format, and Mode		Pixel Port Pins [P19:0]																			
		19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDP	Video out 8-bit 4:2:2	YCrCb[7:0]$_{OUT}$								-	-	-	-	-	-	-	-	-	-	-	-
SDP	Video out 10-bit 4:2:2	YCrCb [9:0]$_{OUT}$										-	-	-	-	-	-	-	-	-	-
SDP	Video out 16-bit 4:2:2	Y[7:0] $_{OUT}$								-	-	CrCb[7:0]$_{OUT}$								-	-
SDP	Video out 20-bit 4:2:2	Y[9:0] $_{OUT}$										CrCb[7:0]$_{OUT}$									
CP	Video out 12-bit 4:4:4 RGB DDR	D7 B[7]↑ R[3]↓	D6 B[6]↑ R[2]↓	D5 B[5]↑ R[1]↓	D4 B[4]↑ R[0]↓	D3 B[3]↑ G[7]↓	D2 B[2]↑ G[6]↓	D1 B[1]↑ G[5]↓	D0 B[0]↑ G[4]↓	-	-	D11 G[3]↑ R[7]↓	D10 G[2]↑ R[6]↓	D9 G[1]↑ R[5]↓	D8 G[0]↑ R[4]↓	-	-	-	-	-	-
CP	Video out 16-bit 4:2:2	CHA[7:0] $_{OUT}$ (for example, Y[7:0])								-	-	CHB/C[7:0] $_{OUT}$ (for example, Cr/Cb[7:0])								-	-
CP	Video out 20-bit 4:2:2	CHA[9:0] $_{OUT}$ (for example, Y[9:0])										CHB/C[9:0] $_{OUT}$ (for example, Cr/Cb[9:0])									

Video Formatting

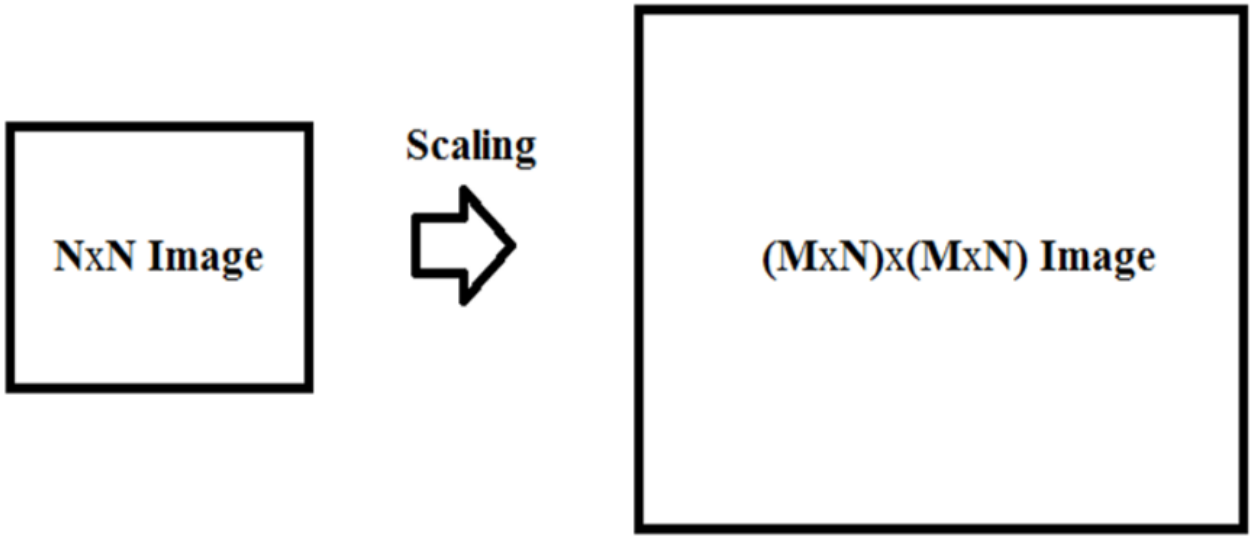
12-bit DDR RGB Pixel Data up to 75MHz

CP	Video out 12-bit 4:4:4 RGB DDR	D7 B[7]↑ R[3]↓	D6 B[6]↑ R[2]↓	D5 B[5]↑ R[1]↓	D4 B[4]↑ R[0]↓	D3 B[3]↑ G[7]↓	D2 B[2]↑ G[6]↓	D1 B[1]↑ G[5]↓	D0 B[0]↑ G[4]↓	-	-	D11 G[3]↑ R[7]↓	D10 G[2]↑ R[6]↓	D9 G[1]↑ R[5]↓	D8 G[0]↑ R[4]↓	-	-	-	-	-	-



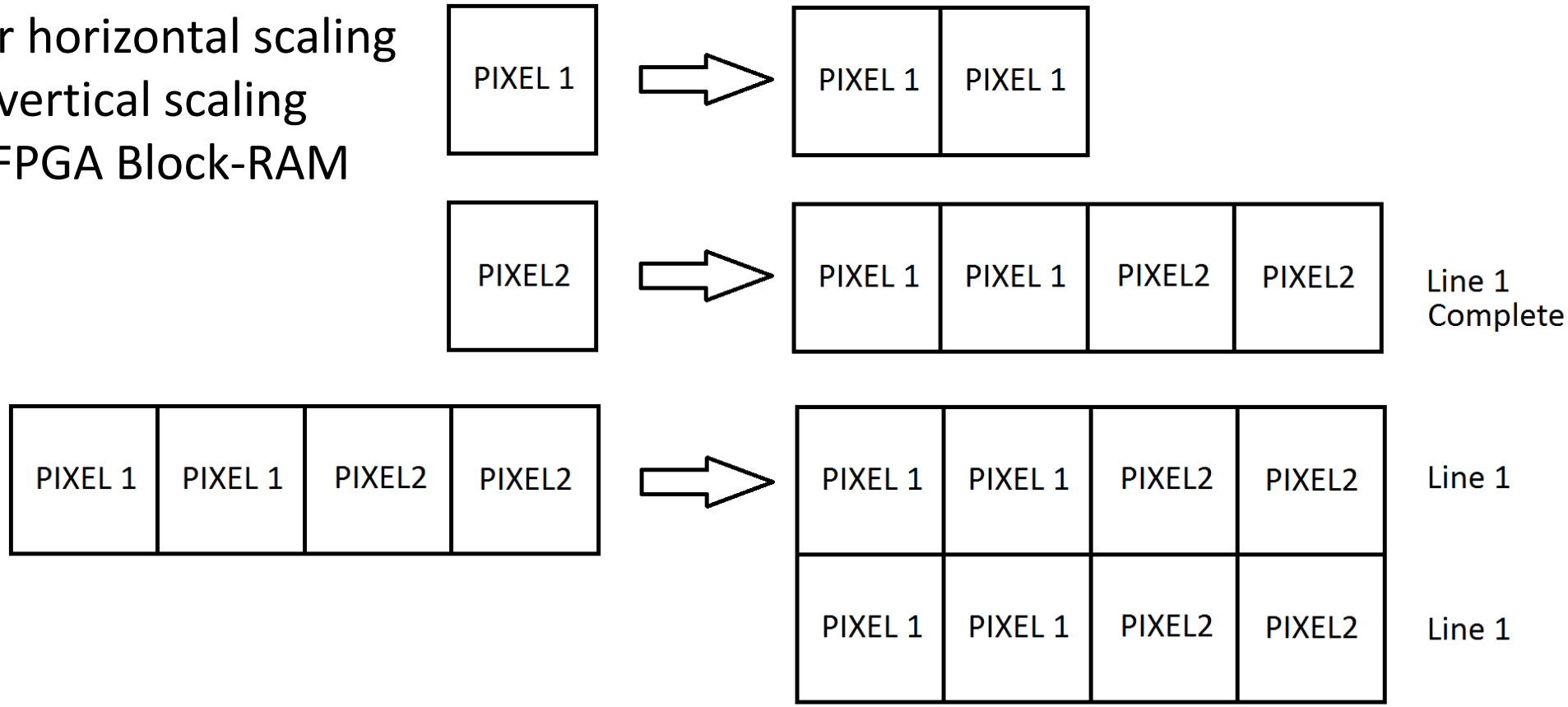
Scaling Methods

- Video sources dynamically change video output between 240p and 480i
- 240p for fast motion, 480i for static menus
- Require mode for interlaced and mode for progressive content
- FPGA must be able to quickly switch between scaling modes



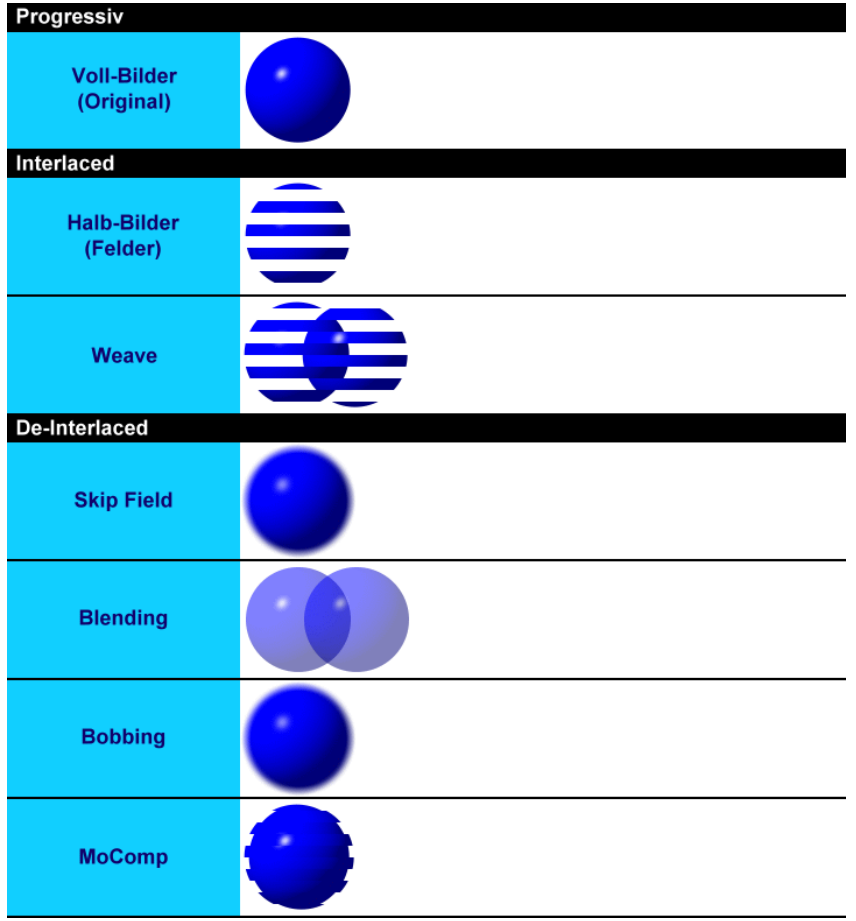
240p Video Scaling

- Pixels duplication for horizontal scaling
- Line duplication for vertical scaling
- Pixel data stored in FPGA Block-RAM



Dealing with 480i

- No ideal deinterlacing algorithm for field sequences with fast motion
- Luckily game consoles typically use 480i for static things like menus
- Therefore we choose method based on computational requirements, the lower the better
- Blending and bobbing will be supported

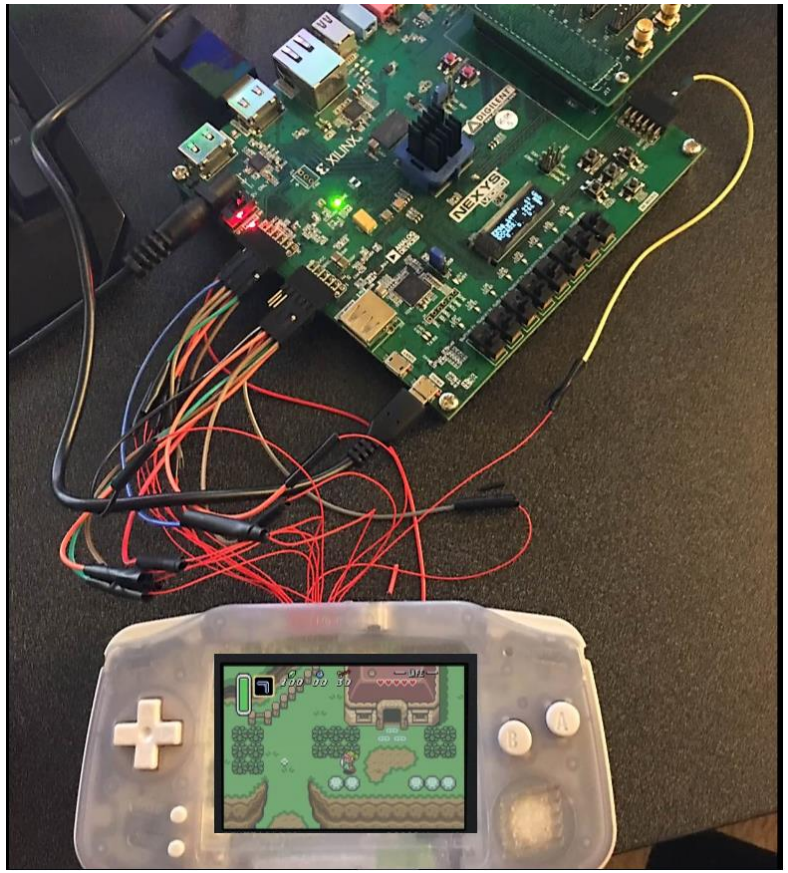


HDMI Output

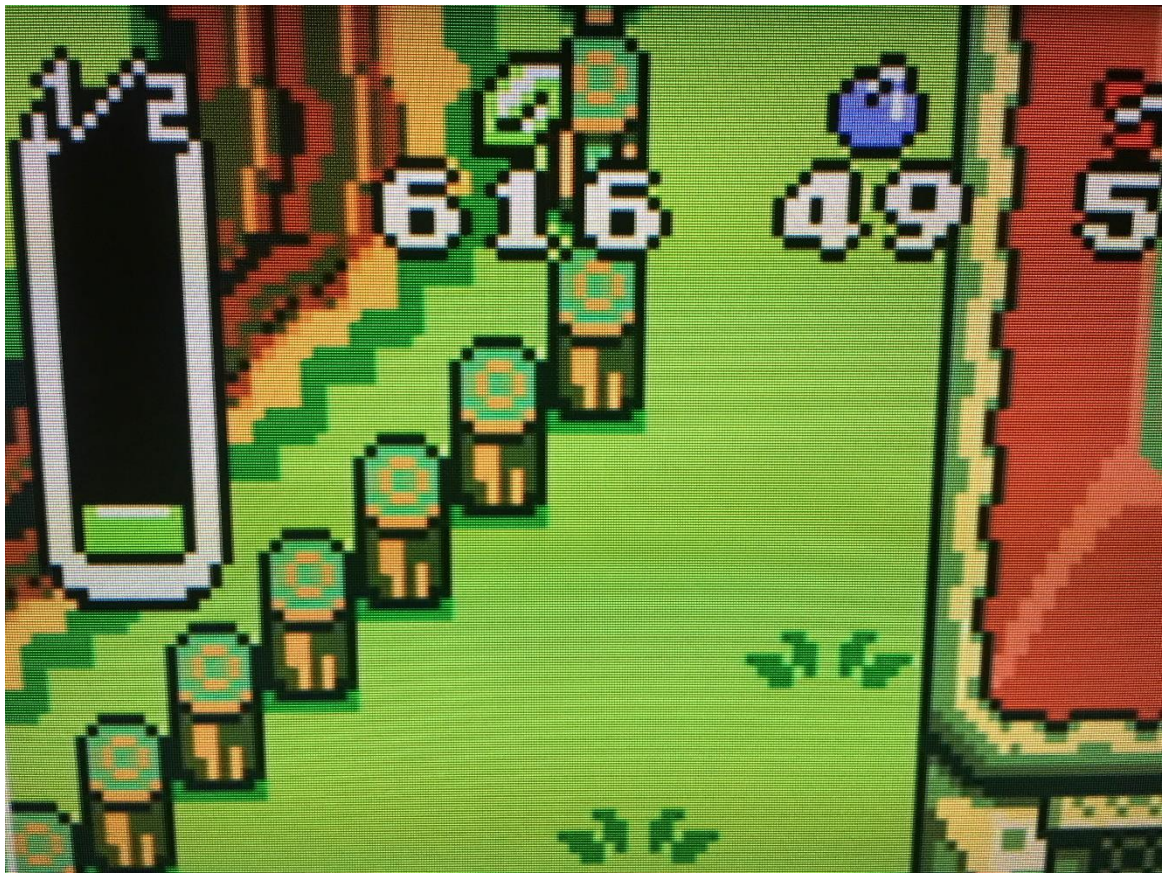
- HDMI uses 8 FPGA I/O versus 26 for VGA
  - Reduces PCB complexity
- Single Cable for both audio and video
- HDMI signal encoding performed in FPGA logic
  - Reduces BOM and PCB complexity

	Supported Video Modes
Scale 2x →	640x480p 60Hz
Scale 3x →	960x720p 60Hz
Scale 4x →	1280x960p 60Hz

Scaling and HDMI Test



Gameboy Advance: 15-bit
RGB 240x160p



HDMI: “line doubled”
15-bit RGB 480x320p

MCU Integration

Key Responsibilities

- FPGA programming from binary config file on uSD card
- Initialization of video buffer ICs, video decoder (I2C) and audio decoder (SPI)
- Handling user IR control requests
- Reconfiguring input stage ICs per user requests
- On-device feedback via LEDs

Microcontroller Comparison

Device	MSP430	TM4C123	STM32F030	**STM32F070**	STM32F103
Clock	16 MHz	80 MHz	48 MHz	**48 MHz**	72 MHz
Bus Width	16 bits	32 bit	32 bit	**32 bit**	32 bit
Package	Various	LQFP64	LQFP64	**LQFP64**	LQFP64
Code Mem	16 kB	256 kB	64 kB	**128 kB**	128 kB
Data Mem	512 B	32 kB	8 kB	**16 kB**	20 kB
I/O Pins	Up to 24	Up to 43	55	**51**	51
Timers	2	12+	7	**7**	7
Price	$2.80	$11.00	$2.11	**$4.70**	$7.14

- MSP430 considered for low cost and prior familiarity
- TM4C123 offers TI ecosystem and tools in a Cortex M4 design
- Several STMicro offerings, all ARM (F0 Cortex M0 and F1 Cortex M3

STM32F070RBT6

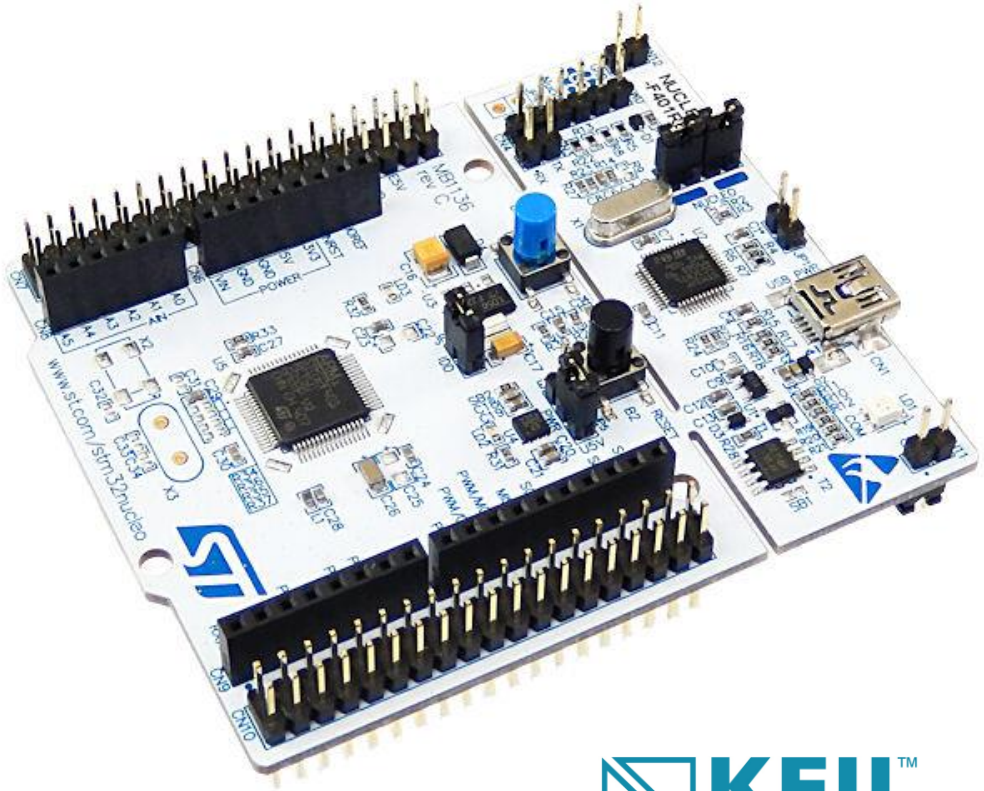
- Significant performance gain over MSP430
- Middle-ground in cost-performance
- Extensive peripheral support
  - Up to 51 GPIOs
  - 2 I2C hardware interfaces
  - 4 USART hardware interfaces
  - 2 SPI blocks
  - SWD (Serial Wire Debug) ready via ST-LinkV2
  - ST factory bootloader for program flashing over UART (enabled via single pin jumper configuration)
- Nucleo development boards

12mm x 12 mm

STM32 Development Tools

Nucleo Development Boards

- Full pin breakout from the LQFP64 package
- STLinkV2 emulation for SWD access
- Extremely low cost, typically < $10
- Available with our specific F070RBT6 MCU



Keil MDK and uVision IDE

- Professional development platform
- Compiler toolchain and RTOS kernel
- Large code size license (256k) for use with STM32 Cortex M0 devices

KEIL™ Tools by ARM

Reprogramming Options

Serial Wire Debug

- ARM standard programming and debugging interface
- ST provides interface via ST-LinkV2
- Small board footprint, only 5 pins required
- Adapter via Adafruit at right ($12.50), similar can be had for ~$5 on ebay
- Nucleo boards can also be configured as programmers

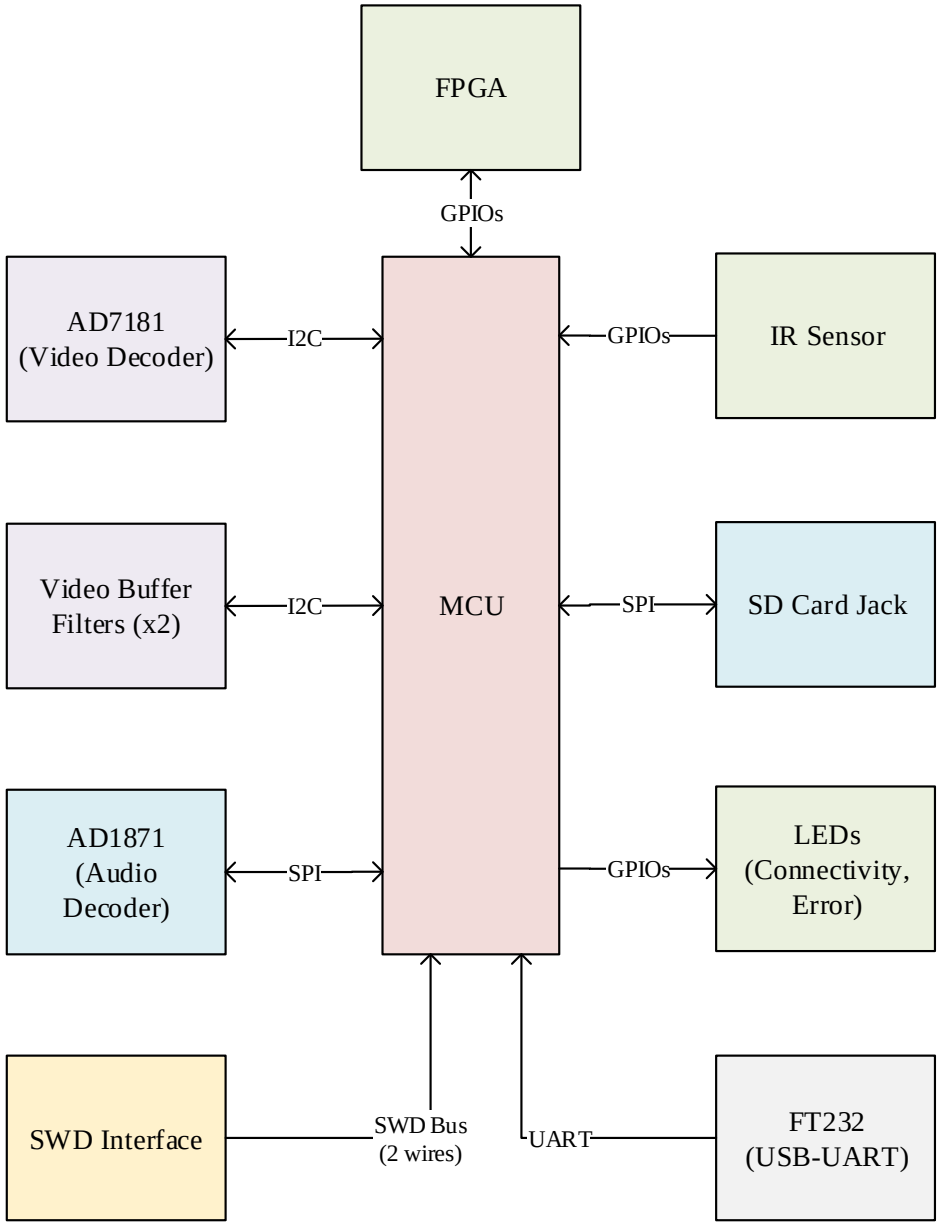
ST Bootloader

- Factory programmed boot option for STM32 devices
- Allows flashing chip via UART interface, no debug
- ST provided Flash Loader Demonstrator application

Microcontroller Interfaces

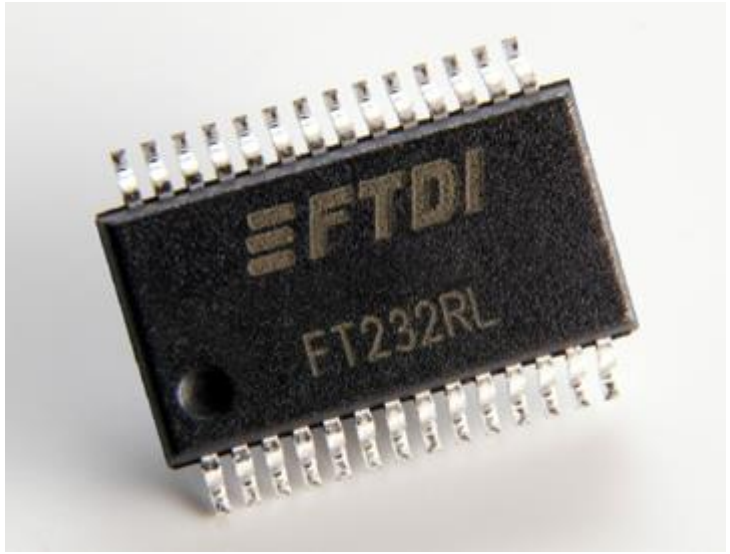
MCU chief responsibilities are system initialization, integration, and interface control

- GPIOs
  - IR receiver, LEDs, FPGA
- I2C bus
  - Video decoder, video buffers
- SPI
  - Audio decoder, uSD in SPI mode
- Reprogramming interfaces
  - SWD, UART-USB via FT232

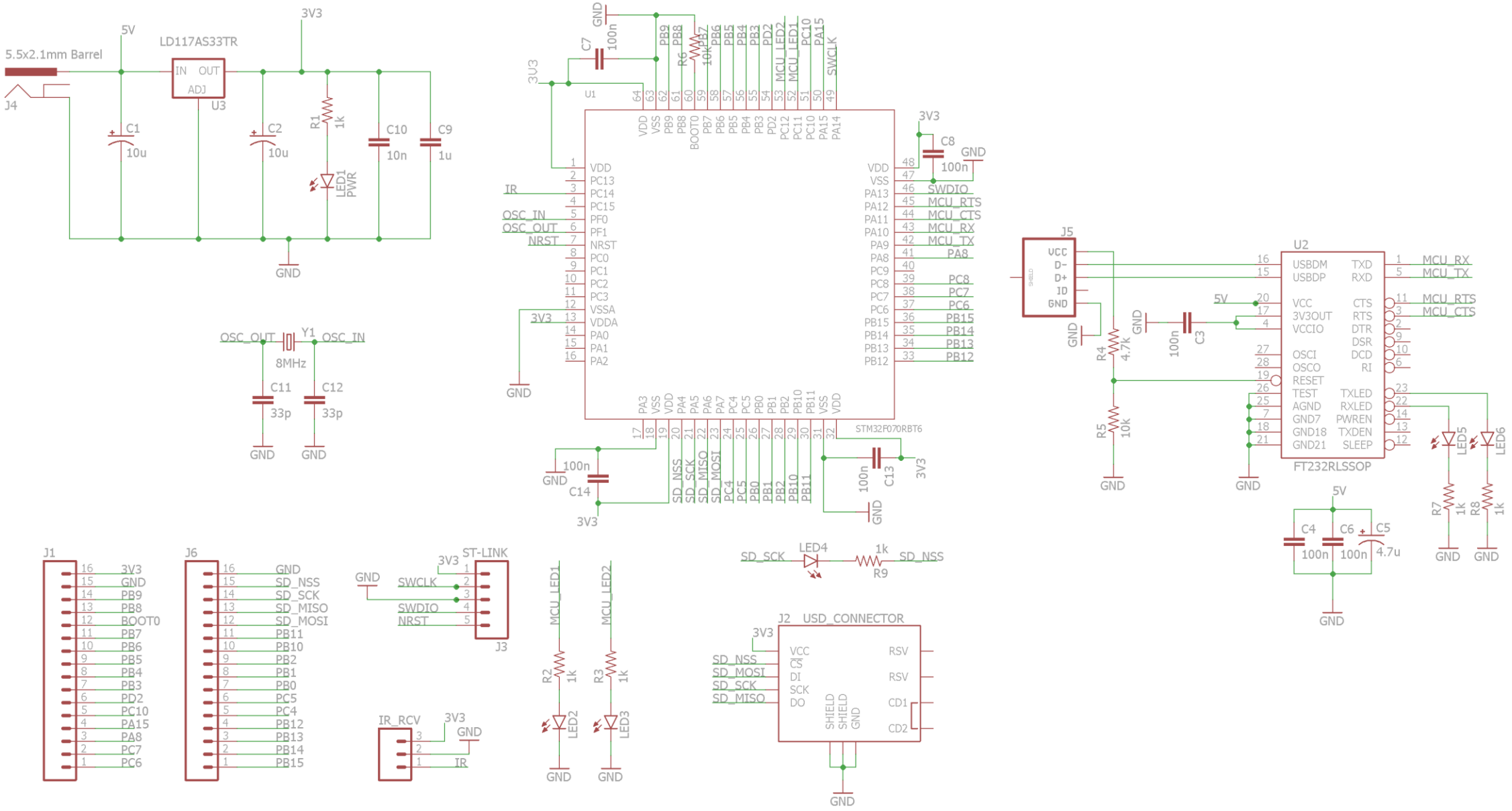


USB-UART IC (FT232RL)

- Translation from USB <-> UART
- Built in regulator to (optionally) convert logic levels from 5V to 3.3V. Configurable to other logic levels
- Used in previous projects and breakouts on hand
- Small board footprint, approx. 10x8 mm in SSOP-28 package (shown right)
- ~$4.50



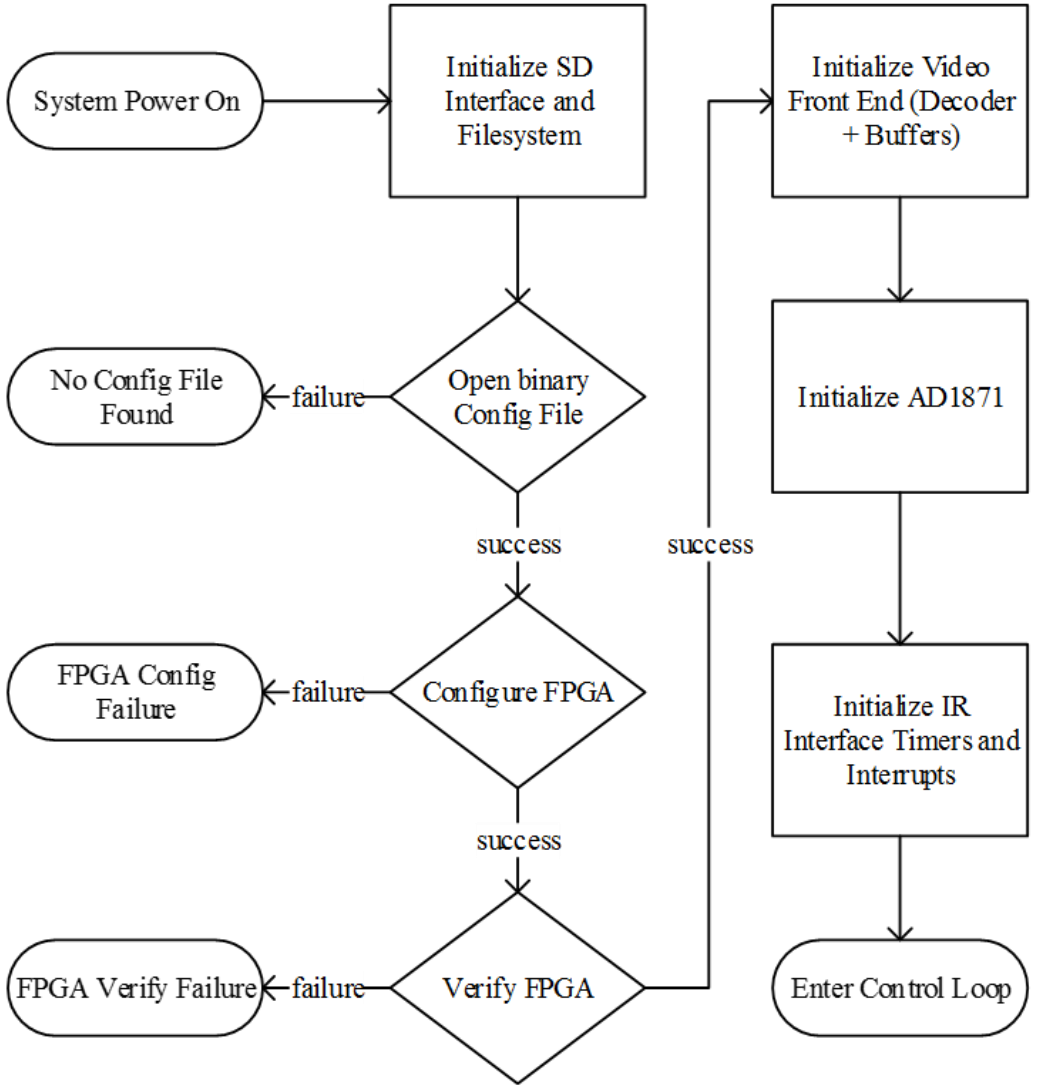
MCU Peripheral Board (Schematic)



System Initialization

- FPGA programming via slave serial method described in XAPP583
- Input select for video buffers, signal format select and other settings for video decoder (> 100 registers)
- Serial data format, mute control, etc for audio decoder

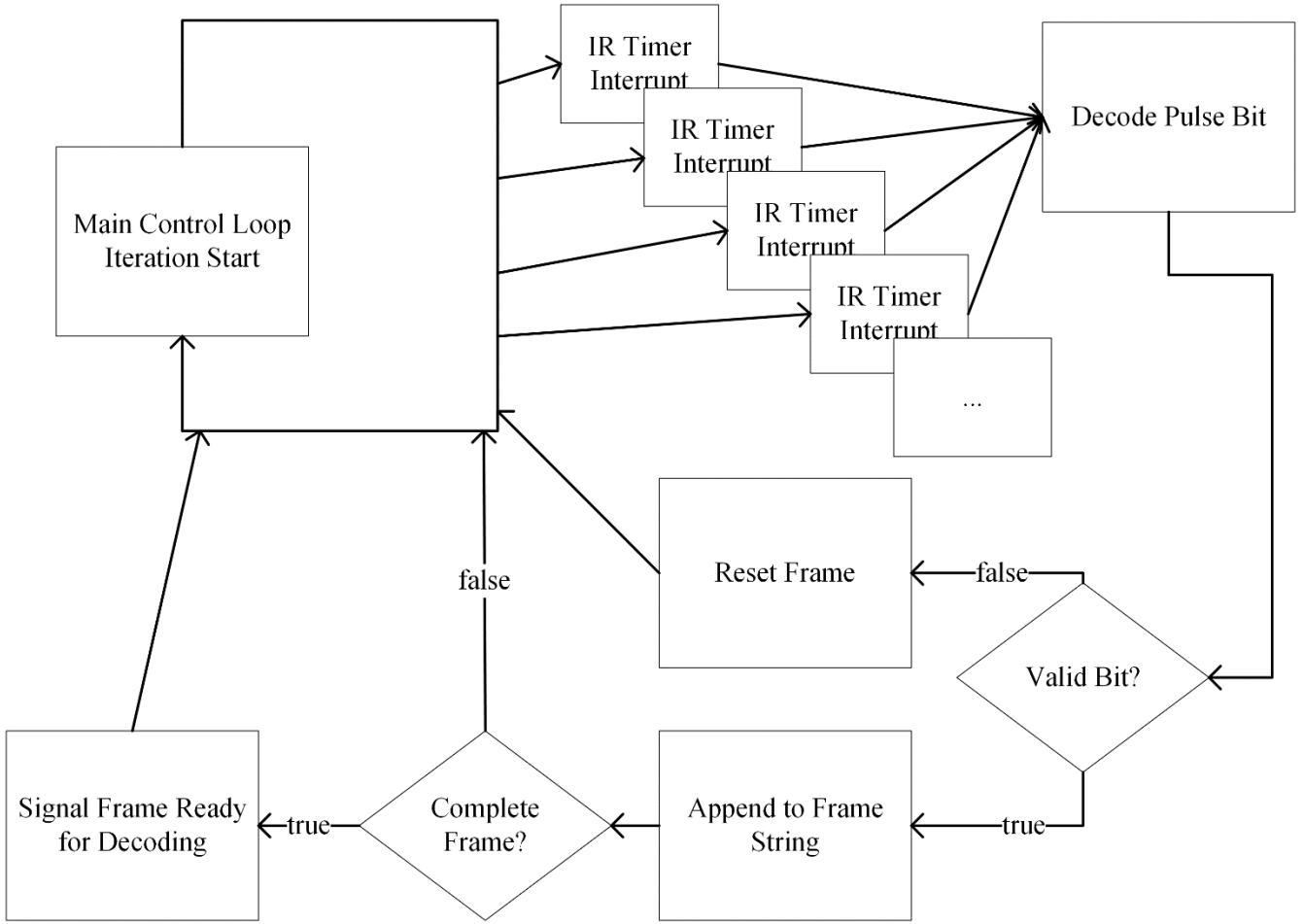
Failure modes indicated by LEDs



IR Receiver Configuration

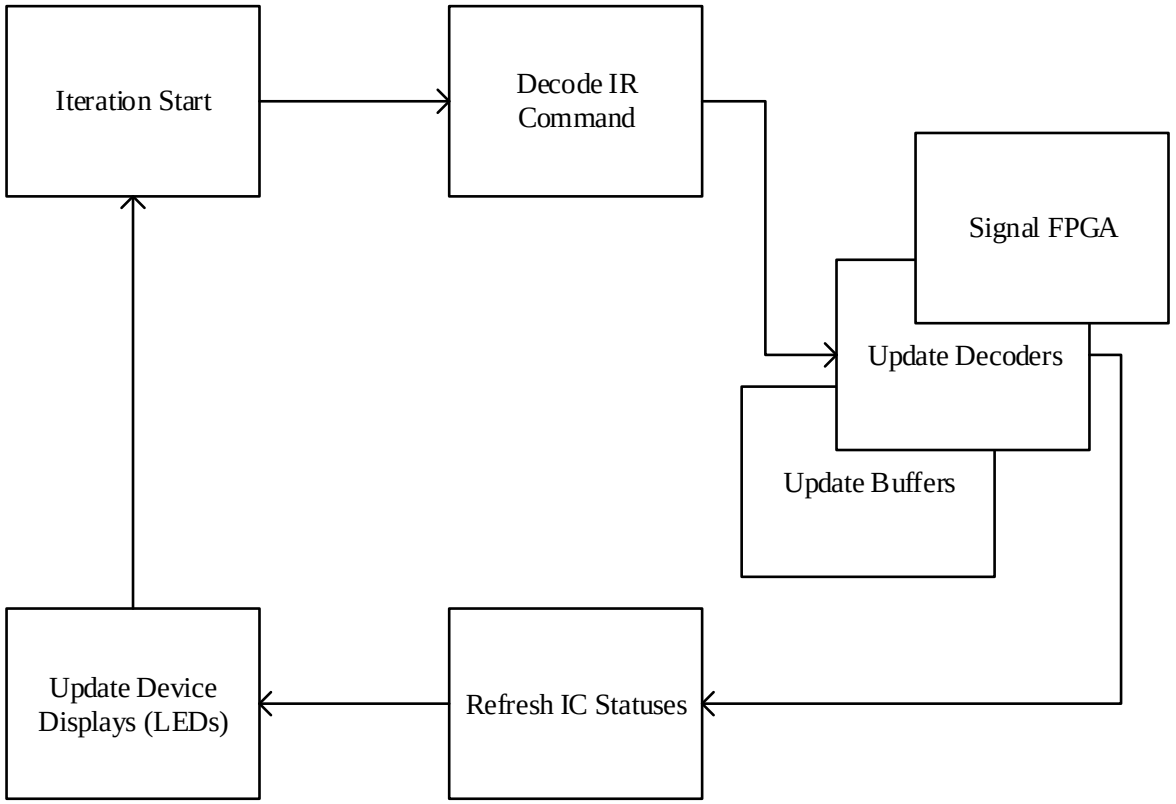
- Interrupts generated on signal transition using timers in input capture mode
- Pulse length measured and used to decode IR stream bits and build IR frame
- Poll for complete IR frame during control loop and handle appropriately

Existing implementations for RC5 and SIRC, modifications to support other protocols



Control Summary

- Basic Control Loop
  - Check for user input
  - Update devices accordingly
  - Update relevant status data from special purpose ICs
  - Update output
  - …



Library Support

STM32 Standard Peripheral Library

- Register configuration abstraction for peripherals (I2C, SPI, Timers, etc)
- Not particularly well documented, existing examples and ecosystems focus on F1 and F4 (Cortex M3 and M4 respectively) devices with different implementation

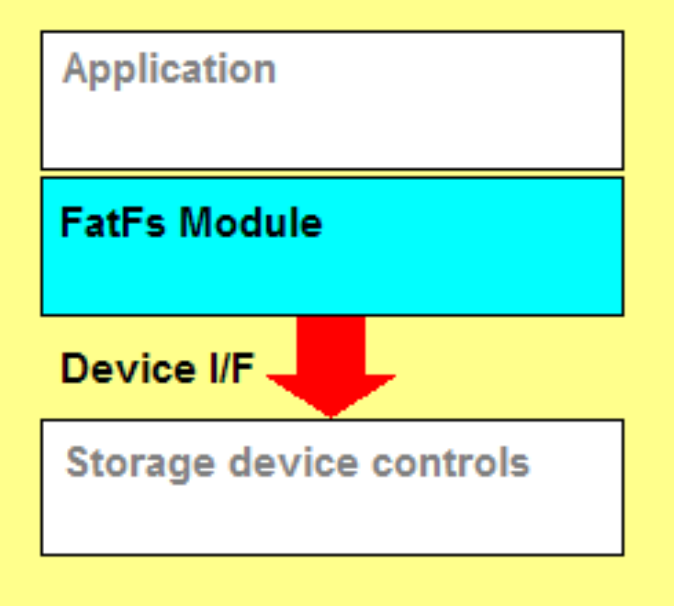
STM32 EVAL Examples

- Example implementations of extended functionality using STM32 devices
  - e.g. infrared receiver
  - Application notes/guidance on modifying for general purpose

Library Support

FatFS

- FAT implementation for embedded devices
- Provides filesystem abstraction for user application with a handful of user implemented device interface functions
  - disk_status()
  - disk_initialize()
  - disk_read()
  - disk_write()
  - disk_ioctl()
  - get_fattime()
- Interface provided to uSD via SPI interface



Power Considerations

The Super Doubler requires a well maintained DC power supply

- Digital circuits are very NOISY.
- Analog circuits are very sensitive to noise.
- Supplies and Grounds of Analog and Digital circuits will be seperated from each other.
- Physical challeges arise when providing power to devices using multiple power supplies (Board space).
- Many mixed signal IC’s require power sequencing to prevent damage to the chip.
- Switching versus linear regulation

AC-DC wall adapter

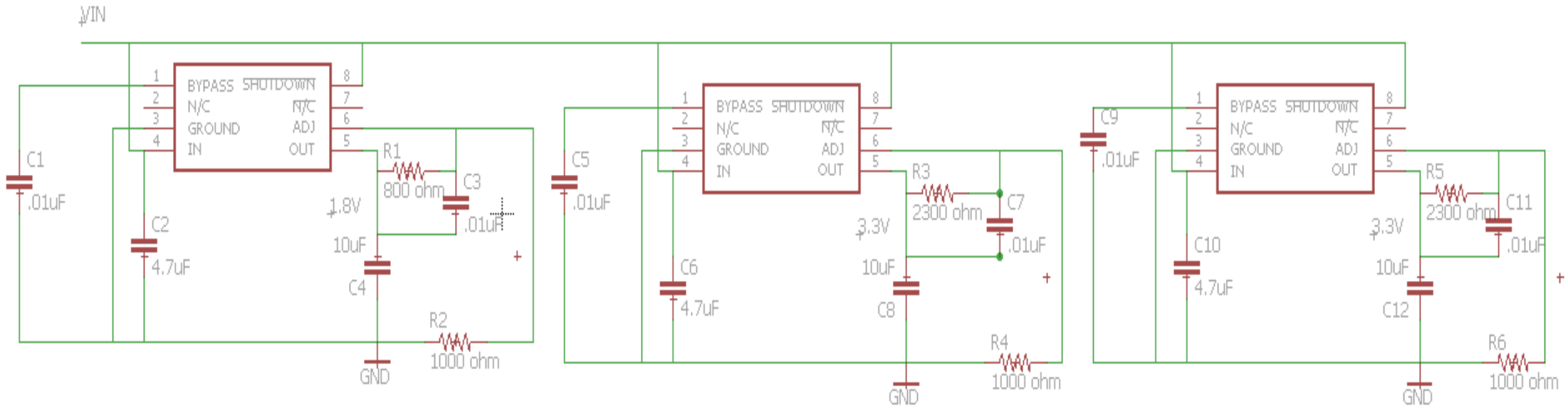
- 5 Volt 3 Amp Power Adapter.
- 2.1mm X 5.5mm plug.
- Used to power prototype PCB’s and final PCB.
- $11.96

Analog Video Input Board

- Board used for prototyping Analog Devices ADV7181 Video Decoder
- 5 Volt input
- 3.3 Volt and 1.8 Volt Analog and Digital supplies

Supply	Level
Digital Core Supply Voltage	1.8V
Digital I/O Supply Voltage	3.3V
PLL supply Voltage	1.8V
Analog supply Voltage	3.3V

Analog Video Input Board Power Schematic.

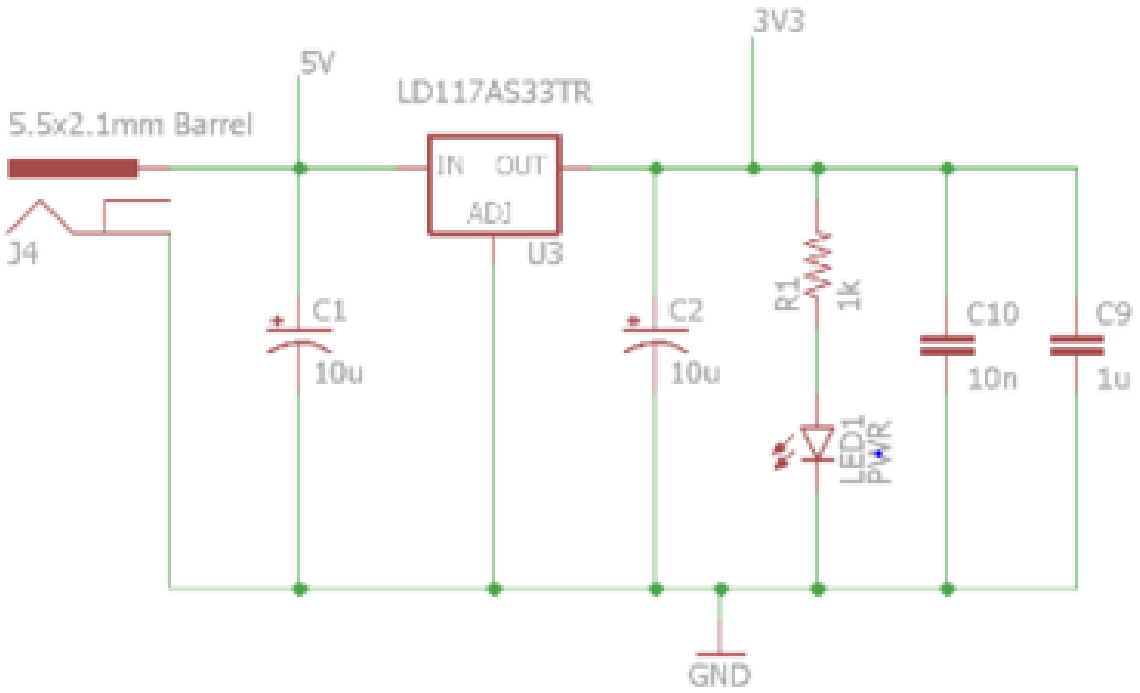


MCU Board

- Board used for prototyping
- 5 Volt input
- 5 Volt and 3.3 Volt supplies

Supply	Value
STM32F070RBT6 MCU	Analog 3.3V, Digital 3.3V
FT232RL USB <-> UART	5V
IR Receiver, MicroSD.	3.3V

MCU Board Power Schematic



Final PCB

- Prototype boards will be integrated into one final PCB.
- Appropriate systems will share power supplies.
- Appropriate supplies will be sequenced to ensure system stability and safety.

LP3878-adJ Low-Dropout Regulator

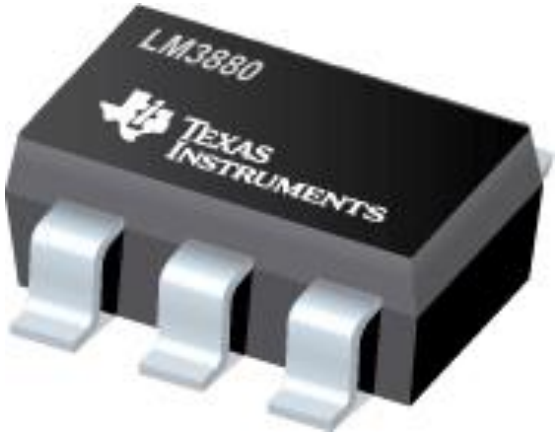
- Input Supply Voltage: 2.5 V to 16V.
- Output Voltage Range: 1 V to 5.5 V.
- 4.89mm × 3.90mm SO-PowerPad (8).
- Precise, low noise output voltage.
- Easy implementation / “Ceramic Stable”.
- $1.96

TPS54527 Synchronous Step-Down Converter

- Input voltage range: 4.5V to 18V.
- Output Voltage Range: 0.76 V to 6 V.
- Regulator to be used to power systems with substantial noise immunity (digital circuits).
- 4.5mm X 6mm DDA (8) package
- $3.25

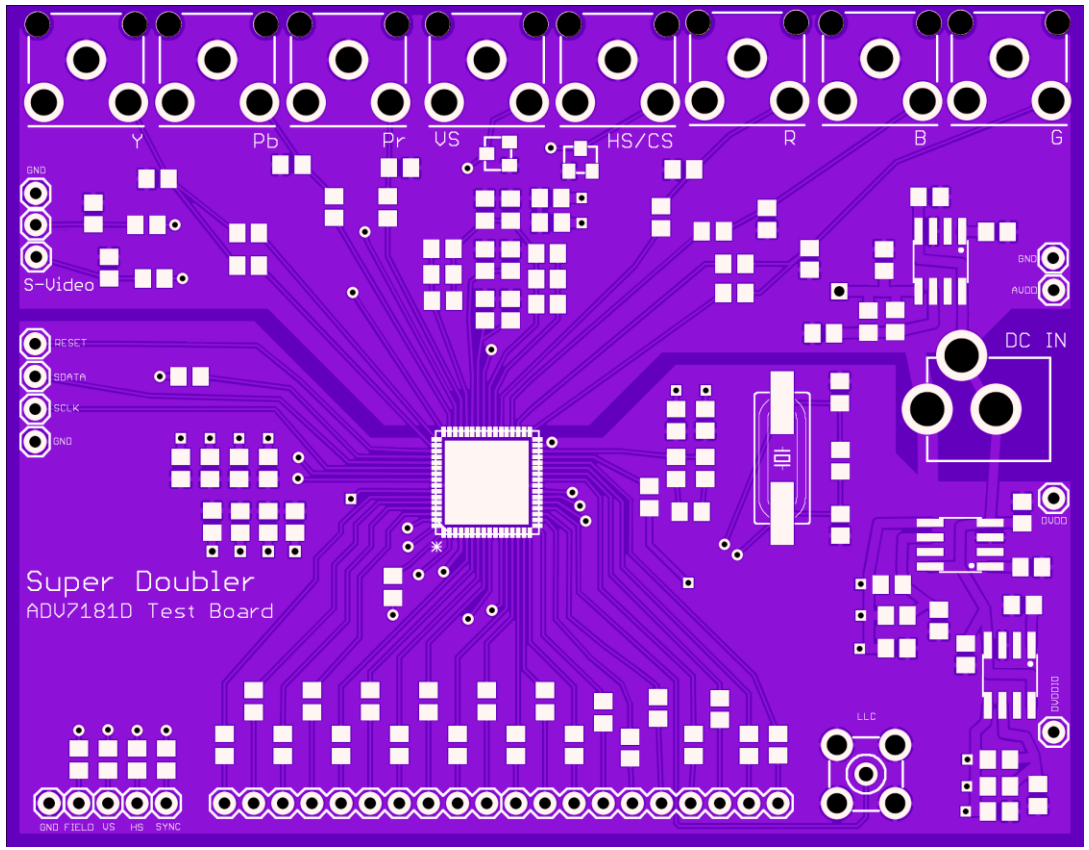
LM3880 Power Sequencer

- Input Voltage Range of 2.7 V to 5.5 V
- 3 Channel power Sequencer
- Power-Up and Power-Down Control
- Sends flags to enable inputs of regulators.
- 2.9mm X 1.6mm DDA (8) package
- $1.42

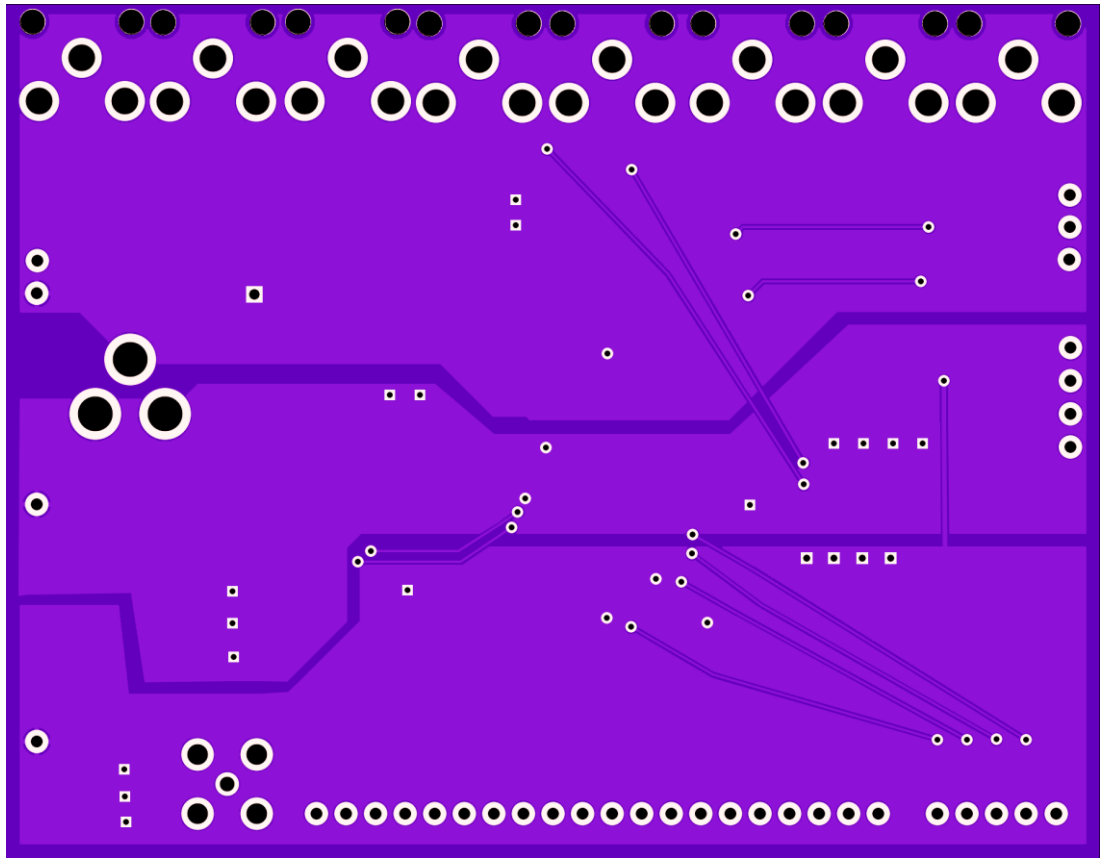


Analog Video Input PCB

- Front



- Back



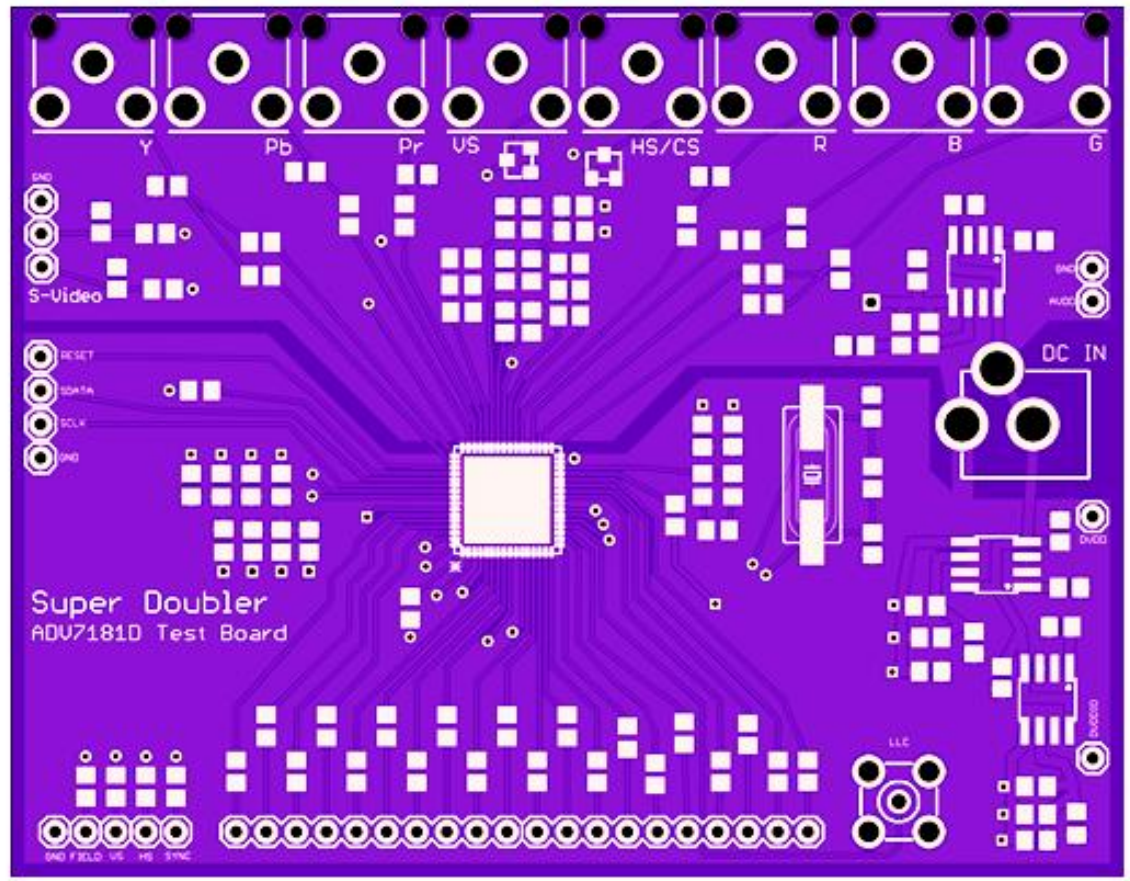
Component in

RGB in

S Video

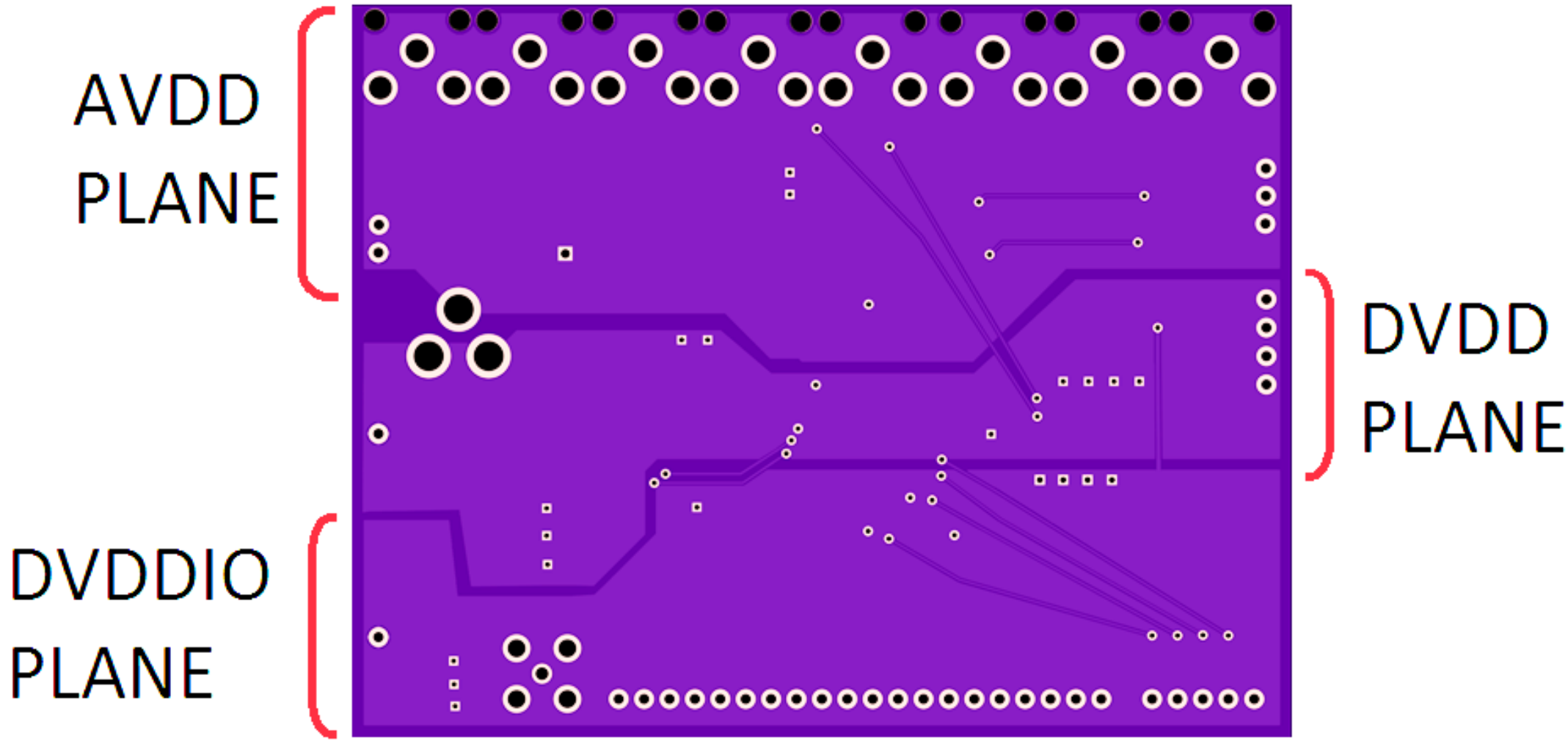
I2C

DC in

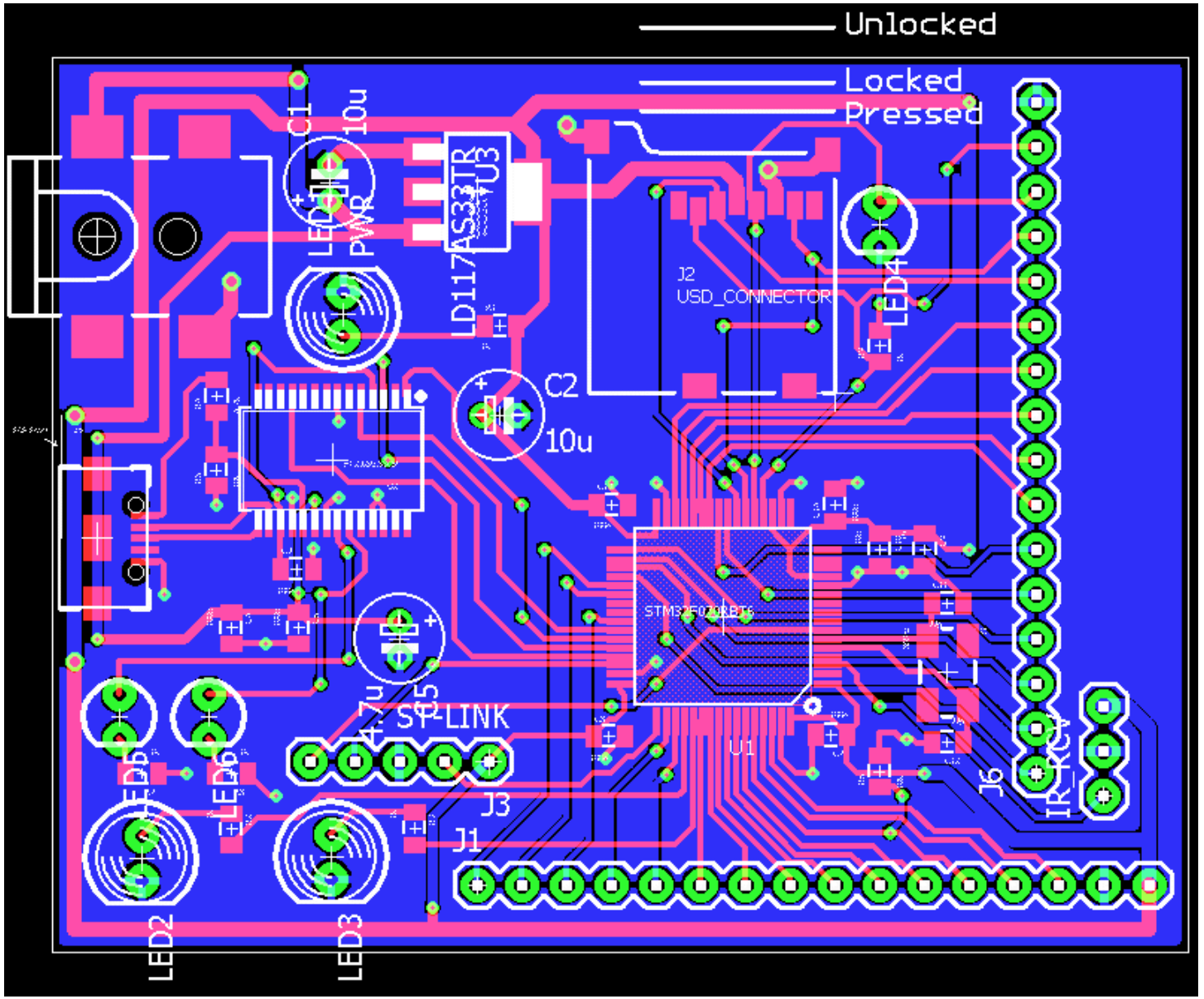


Digital Timing Signals (Synch)

Digital Video Output


AVDD
PLANE
DVDD
PLANE
DVDDIO
PLANE

MCU Peripheral Board (Layout)

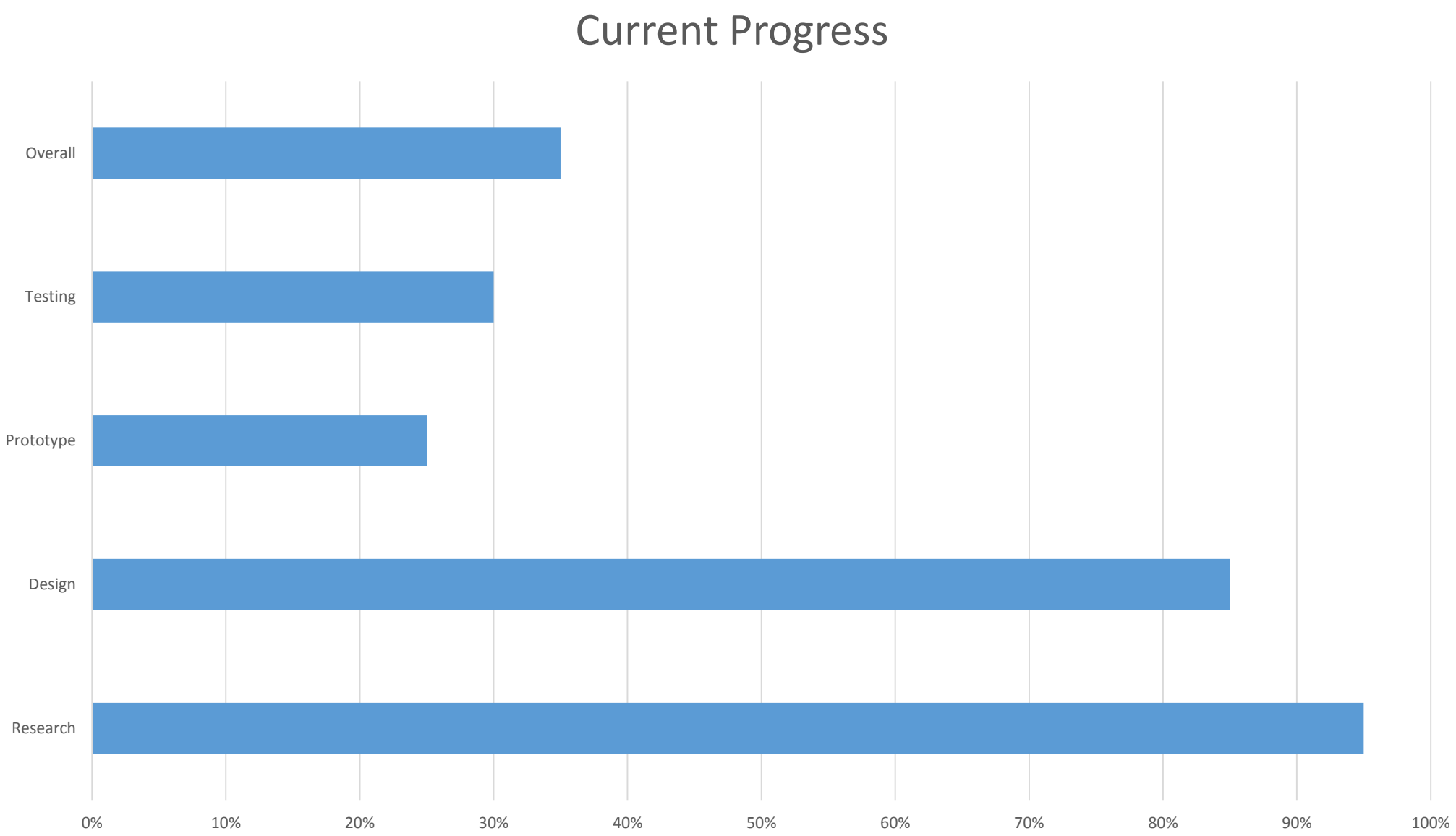


Final PCB Summary

- Protypes will be integrated
- Audio Chip will be integrated
- Final unit will connect to FPGA via FMC connector

Device enclosure

- 5.50 x 5.25 x 1.63 in.
  - Other sizes available
- $9.31 from polycase.com


Current Progress
Overall
Testing
Prototype
Design
Research
0%
10%
20%
30%
40%
50%
60%
70%
80%
90%
100%

Estimated Budget

Part Name	Unit Cost	Quantity	Total
Power System Components Set	~$30	3	$90
THS 7353 Video Buffer	$3	3	$9
AD1871 Audio Decoder	$10	3	$30
ADV7181 Video Decoder	$14	3	$42
STM32F070RBT6 MCU IC	$2	3	$6
Miscellaneous ICs	-	Varies	$50
Barrel Jacks (RCA, Power, etc)	$1	10+	$10
Miscellaneous Jacks	-	Varies	$50
Miscellaneous Components	-	Varies	$50
PCB Fab/acquisition	$50	1	$50
Enclosure	$10	1	$10
Remote/Receiver Components	$10	1	$10
SD Card	$10	1	$10
Development Boards and Tools	~$150	Varies	$150
Total			$567

Current Expenses

Part Name	Total
Power System Components Set	$10
THS 7353 Video Buffer	$9
AD1871 Audio Decoder	$30
ADV7181 Video Decoder	$36
STM32F070RBT6 MCU IC	$6
Miscellaneous ICs	$10
Barrel Jacks (RCA, Power, etc)	$10
Miscellaneous Jacks	$15
Miscellaneous Components	$50
PCB	$55
Soldering Materials	$35
Remote/Receiver Components	$10
SD Card	$10
Development Boards and Tools	$550
Total Budget	$836

Division of Labor

- Stephen: FPGA development, video processing
- Kenneth: MCU interfacing, peripherals, MCU programming
- Gilson: video filtering, video decoder, audio decoder
- Tyler: power, manufacturing, testing, administrative

Questions?