LABORATORY MANUAL

DEPARTMENT OF
ELECTRICAL & COMPUTER ENGINEERING

UNIVERSITY OF CENTRAL FLORIDA

EEL 4309
Electronics II

Revised
January 2012

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Safety Rules and Operating Procedures

1. Note the location of the Emergency Disconnect (red button near the door) to shut off power in an emergency. Note the location of the nearest telephone (map on bulletin board).

2. Students are allowed in the laboratory only when the instructor is present.

3. Open drinks and food are not allowed near the lab benches.

4. Report any broken equipment or defective parts to the lab instructor. Do not open, remove the cover, or attempt to repair any equipment.

5. When the lab exercise is over, all instruments, except computers, must be turned off. Return substitution boxes to the designated location. Your lab grade will be affected if your laboratory station is not tidy when you leave.

6. University property must not be taken from the laboratory.

7. Do not move instruments from one lab station to another lab station.

8. Do not tamper with or remove security straps, locks, or other security devices. Do not disable or attempt to defeat the security camera.

9. When touching the FPGA development boards please do not touch the solid-state parts on the board but handle the board from its edge.

10. **ANYONE VIOLATING ANY RULES OR REGULATIONS MAY BE DENIED ACCESS TO THESE FACILITIES**.

I have read and understand these rules and procedures. I agree to abide by these rules and procedures at all times while using these facilities. I understand that failure to follow these rules and procedures will result in my immediate dismissal from the laboratory and additional disciplinary action may be taken.

_____ _____

Signature Date Lab #

Laboratory Safety Information

Introduction

The danger of injury or death from electrical shock, fire, or explosion is present while conducting experiments in this laboratory. To work safely, it is important that you understand the prudent practices necessary to minimize the risks and what to do if there is an accident.

Electrical Shock

Avoid contact with conductors in energized electrical circuits. The typical cannot let-go (the current in which a person cannot let go) current is about 6-30 ma (OSHA). Muscle contractions can prevent the person from moving away the energized circuit. Possible death can occur as low 50 ma. For a person that is wet the body resistance can be as low as 1000 ohms. A voltage of 50 volts can result in death.

Do not touch someone who is being shocked while still in contact with the electrical conductor or you may also be electrocuted. Instead, press the Emergency Disconnect (red button located near the door to the laboratory). This shuts off all power, except the lights.

Make sure your hands are dry. The resistance of dry, unbroken skin is relatively high and thus reduces the risk of shock. Skin that is broken, wet, or damp with sweat has a low resistance.

When working with an energized circuit, work with only your right hand, keeping your left hand away from all conductive material. This reduces the likelihood of an accident that results in current passing through your heart.

Be cautious of rings, watches, and necklaces (which increase the conductivity and contact area). Skin beneath a ring or watch is damp, lowering the skin resistance. Shoes covering the feet are much safer than sandals.

If the victim isn't breathing, find someone certified in CPR. Be quick! Some of the staff in the Department Office are certified in CPR. If the victim is unconscious or needs an ambulance, call 911. If able, the victim should go to the Student Health Services for examination and treatment.

Fire

Transistors and other components can become extremely hot and cause severe burns if touched. If resistors or other components on your proto-board catch fire, turn off the power supply and notify the instructor. If electronic instruments catch fire, press the Emergency Disconnect (red button). These small electrical fires extinguish quickly after the power is shut off. Avoid using fire extinguishers on electronic instruments.

Explosions

When using electrolytic / tantalum capacitors, be careful to observe proper polarity and do not exceed the voltage rating. Electrolytic and tantalum capacitors can explode and cause injury. A first aid kit is located on the wall near the door. Proceed to Student Health Services, if needed.

EXPERIMENT #1

Linear Operational Amplifier Applications

Goals:

To introduce the concepts of an operational amplifier (op-amp) used as a non-inverting amplifier, inverting amplifier, unity gain buffer and a summing amplifier. Data collected during this laboratory experiment will be compared to the datasheet of the operational amplifier used.

References:

The following two links are to the Tektronix website for the user manuals for the DPO 4034B Mixed Signal oscilloscope and for the AFG3022B Arbitrary Function generator:

Oscilloscope:
http://www.tek.com/search/apachesolr_search/DPO%204034B%20user%20manual

Arbitrary Function Generator:
http://www.tek.com/search/apachesolr_search/afg3022b?filters=tid%3A1016

Please note, to download the user manual, Tektronix requires that you fill out the user information form before downloading can begin.

Equipment:

Oscilloscope: DPO 4034B Mixed Signal
Function Generator: AFG3022B
Triple Power supply
Breadboard
TL081-TL084 family of operational amplifiers
Capacitors available in the laboratory
Resistors available in the laboratory

Pre-laboratory:

Read this laboratory experiment carefully to become familiar with the background procedural steps in this experiment. Download the two user manuals for the Tektronix function generator and oscilloscope and become familiar with their use.

Using the simulation package of your choice in which you are the most familiar with: Multisim, Workbench or LTSpice IV simulate the following circuits. If you do not have access to Multisim or Workbench, LTSpice IV is a free to use spice

program available from Linear Technology Inc. and can be downloaded from the following site: http://www.linear.com/designtools/software/#LTspice
The only disadvantage is the part library is for only Linear Technology parts. They do offer a universal operational amplifier (UniversalOpamp2) that can be used for many of the simulations required for EEL4309 laboratory experiments.

The equations required for gain A_V are given in the appropriate sections for the non-inverting amplifier, inverting amplifier, unity gain buffer and the summing amplifier.

a. Design a gain Av of 3 non-inverting amplifier using a minimum of 1k-ohm resistors.
b. Simulate this non-inverting amplifier generating the time transient response for a 1.0 volt, 200 Hz sine wave input. Plot the input as well as the output voltages as a function of time.
c. Repeat steps a and b for a gain of 10.
d. Design a gain Av = -3 inverting amplifier using a minimum of 1k-ohm resistors.
e. Simulate this inverting amplifier generating the time transient response for a 1.0 volt 200 Hz sine wave input. Plot the input as well as the output voltages as a function of time.
f. Repeat step d and e for a gain of Av = -10.
g. Compare the results of steps b with e and c with f.
h. Simulate an unity gain buffer amplifier generating the time transient response for a 1.0 volt 200 Hz sine wave input. Plot the input as well as the output voltages as a function of time.
i. Design a summing amplifier such that

$$Vout = -3V1 - 2V2 \ ,$$

where V1 and V2 are input sources and Vout is the output from the summing amplifier.
j. Simulate this summing amplifier generating the time transient response for a 1.0 volt, 200 Hz sine wave input for V1 and a 2 volt DC input for V2 (V2 = a constant value of 2 volts). Plot the input as well as the output voltages as a function of time.

Discussion:

An operational amplifier (op-amp) is a multistage amplifier, where its output is proportional to the difference between the two inputs:

$$Vout = A_{od}(V^+ - V^-) \qquad (1)$$

The schematic symbol for an op-amp is a triangle with the two inputs V^+ and V^- and the one output Vout as shown in Figure 1. Most op-amps need two power supplies; one with a positive voltage +Vcc and one with a negative voltage -Vcc.

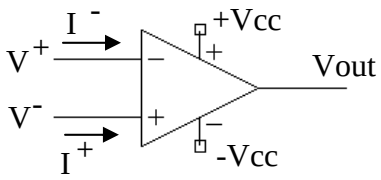


Figure 1: A Schematic diagram of a typical op-amp.

There are several important facts about op-amps. First the output Vout is bounded between the two powers supply voltages:

$$-Vcc \leq Vout \leq + Vcc \tag{2}$$

If the output voltage is allowed to go to exactly -Vcc to +Vcc this op-amp is referred to as an op-amp with a rail-to-rail output. Rewriting Equation (1) gives the following:

$$(V^+ - V^-) = \frac{Vout}{Aod} \tag{3}$$

For most common op-amps, the gain of the op-amp Aod is about 10^6. Since Vout is bound by Equation (2) to be within the power supply values which is typically less than +/- 15 volts, by Equation (3), $(V^+ - V^-)$ is limited to about +/- 15 microvolts. Essentially, $V^+ = V^-$. Finally, the last import fact is the current flowing into the positive V^+ input and the negative V^- input is very small and for most applications can be considered zero ($I^+ = I^- = 0$). Since $V^+ = V^-$ and $I^+ = I^- = 0$, this condition is called a virtual short.

Inverting Amplifier:

Figure 2 gives the schematic diagram for an inverting amplifier. A close look at Figure 2 shows that the op-amp power supply contains both +Vcc and -Vcc, which have been set to +15 and -15 volts, respectively. Also each of the power supply inputs has a capacitor. This capacitor can range in size from about 0.01 microfarad to about 10 microfarad. For this lab and the other labs for this course these two capacitors should be 10 microfarad, 35 volts, available in the lab parts cabinet. In addition, both of these capacitors should be placed as close as possible to the + and - power supply pins of the op-amp (see data sheet for actual pin numbers). These capacitors are used to prevent any noise from being coupled into

the op-amp power supply pins and to prevent any positive feedback that may make the op-amp oscillate.

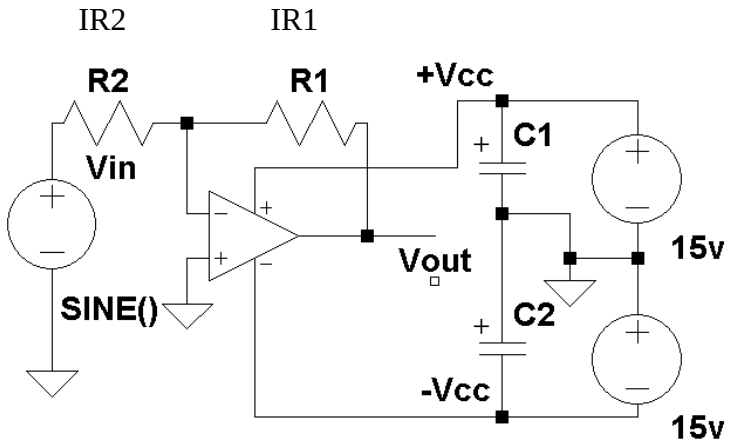


Figure 2: The schematic for an inverting amplifier.

The voltage gain for an inverting amplifier is given as:

$$Av = \frac{Vout}{Vin} = \frac{-R1}{R2} \tag{4}$$

Equation 4 includes a negative sign. This negative sign introduces a 180° phase shift in the output voltage relative to the input voltage. Assuming R1 is a 5k ohm resistor and R2 is a 1k ohm resistor, and Vin is +/- 1 volt triangle input, then Av would be -5 and Vout would be +/- 5volts triangle wave that is 180° out of phase compared to the input as shown in Figure 3. Note how the output signal is 5 times larger than the input signal. For the special case, when R2 = R1 Vout =-Vin a 180° phase shifted version of the input.

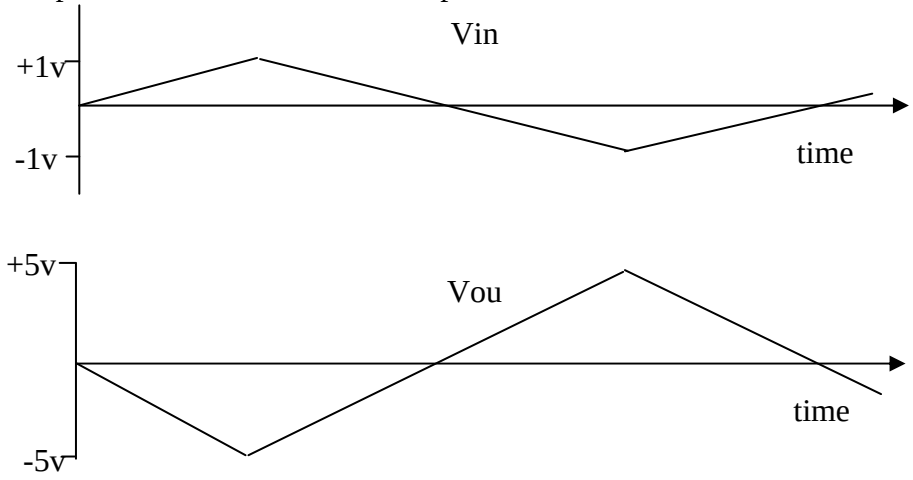


Figure 3: The output for a -5 gain, inverting amplifier with a +/- 1 volt triangle wave input.

The interesting item about the inverting amplifier is that the gain is only a function of the ratio of the two resistors of R1 and R2. Typical values of resistors used in op-amp circuits usually are in the range of 1k ohms to 10 mega ohms.

Given that there is a virtual short between the two inputs of the op-amp $V^- = V^+ = 0$ volts and the current into both input terminals is zero, the current flowing in R1 is the same as the current flowing in R2:

$$IR1 = IR2 = \frac{Vin - 0v}{R2} = \frac{Vin}{R2} = \frac{0v - Vout}{R1} = \frac{-Vout}{R1} \tag{5}$$

The bandwidth of an inverting amplifier depends on the size of the signal on Vout and broken into two categories of small signal and large signal. The two equations that give the -3dB frequency (the frequency in which the magnitude of the voltage gain is reduced by 0.707 from its value given in Equation (4)) are

$$\text{(small signal) } f\text{-}3dB = \frac{\text{Gain-Bandwidth-Product}}{\frac{R1}{R2} + 1} \tag{6}$$

$$\text{(large signal) } f\text{-}3dB = \frac{\text{Slew-Rate}}{2\pi\left(\frac{R1}{R2} + 1\right)Vin(peak)} \tag{7}$$

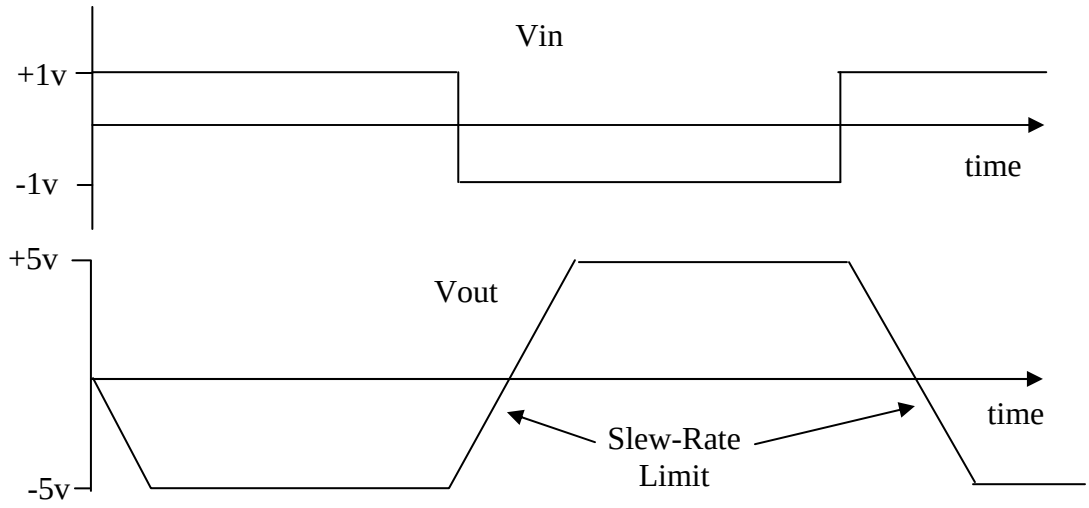


Figure 4: Vout for a square wave input showing the affect of slew-rate limit.

Actual bandwidth of the inverting amplifier is then the smaller of Equations (6) and (7). The Gain-Bandwidth-Product of an op-amp can be found in its datasheet and it's the frequency when Aod of the op-amp is equal to one. The slew-rate is the maximum rate of change of the output Vout given in volts per second and is

also given in the op-amp data sheet. Figure 4 illustrates the effect of a finite slew-rate on a square wave input for an inverting amplifier with a gain of -5. Also in Equation (7), Vin (peak) is the maximum peak input voltage.Equation (6) best describes the bandwidth of the inverting amplifier when the output voltage swing is small and Equation (7) best describes the bandwidth when the output voltage swing is large. It should be noted that in the denominator of Equation (7) that

$$\left(\frac{R1}{R2} + 1\right)\text{Vin(peak)} \tag{8}$$

is nothing more than the peak output voltage.

The last item of interest for the inverting amplifier is the maximum voltage swing that can be achieved by the op-amp. For no load on the op-amp, the op-amp maximum and minimum voltage swing is given by its datasheet. As mentioned before, if the op-amp's maximum and minimum voltage swing are equal to +Vcc to -Vcc then this op-amp is referred to as a rail-to-rail output op-amp. Another factor that limits the maximum output voltage swing is the amount of current that the op-amp output can deliver. Usually, as the load current increases, the maximum output voltage swing decreases. This again is usually given in the op-amp's datasheet. In fact, most op-amps have a maximum output current limit that is set so as to protect the op-amp should its output be accidentally shorted to ground. Most op-amps have internal projection. But what will destroy an op-amp is the accidentally applying the wrong polarity power on +Vcc and -Vcc. Care must be taken to prevent accidentally reversing the op-amp's power supply.

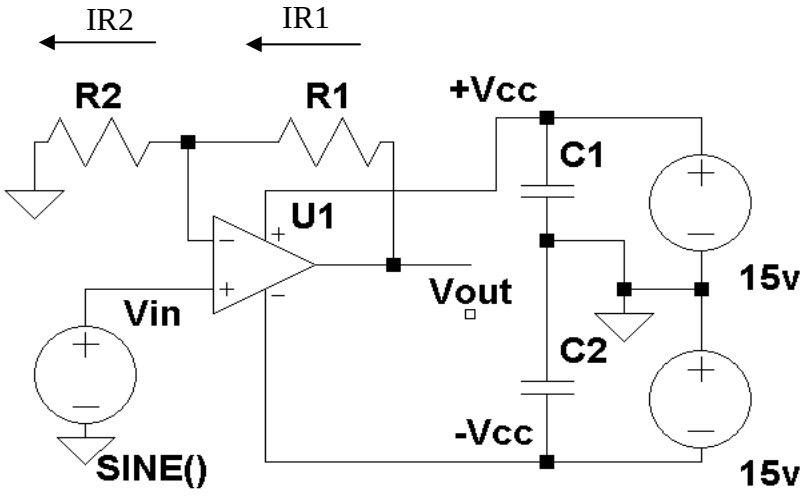


Figure 5: The schematic for a non-inverting amplifier.

Non-inverting Amplifier:

Figure 5 gives the schematic diagram for a non-inverting amplifier. Note how the input is now on the V^+ terminal of the op-amp where for the inverting amplifier

the V^+ was grounded. For the non-inverting amplifier is should be noted that ground does not get directly tied to the op-amp but is tied to one side of R2.

The gain Av for a non-inverting amplifier is given by:

$$Av = \frac{Vout}{Vin} = \frac{R1}{R2} + 1 \qquad (9)$$

In comparing Equation (9) to Equation (4), there is no minus sign indicating that the phase shift for a non-inverting amplifier is 0°. Setting R1 = 4 ·R2, gives a gain Av of 5 and is shown in Figure 6 for a triangle wave input.

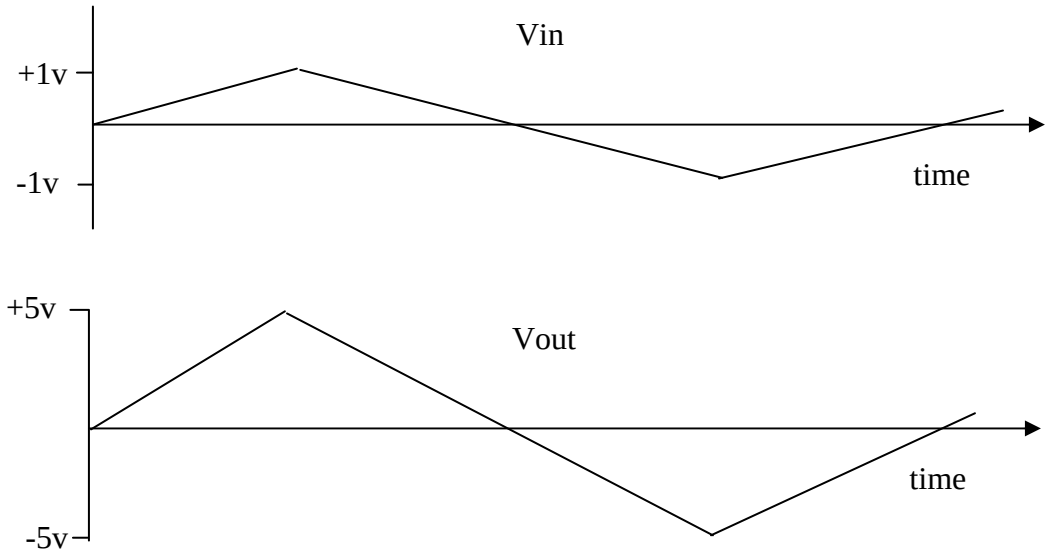


Figure 6: The output for a +5 gain non-inverting amplifier with a +/- 1 volt triangle wave input.

Given that there is a virtual short between the two inputs of the op-amp $V^- = V^+$ = Vin and the current into both input terminals is zero, the current flowing in R1 is the same as the current flowing in R2:

$$IR1 = IR2 = \frac{Vin - 0v}{R2} = \frac{Vin}{R2} = \frac{Vout - Vin}{R1} \qquad (10)$$

The bandwidth of a non-inverting amplifier depends on the size of the signal on Vout, is broken into two categories of small signal and large signal, is the same as for an inverting amplifier and is given by Equations (6) and (7). These are the two equations that give the -3dB frequency (the frequency in which the magnitude of the voltage gain is reduced by 0.707 from its value given in Equation (9)). The actual bandwidth of a non-inverting amplifier is then the smaller of Equations (6) and (7).

Figure 7 illustrates the effect of a finite slew-rate on a square wave input for a non-inverting amplifier with a gain of +5. Like the inverting amplifier, the maximum voltage swing that can be achieved at the output depends on the maximum output current that can be delivered by the op amp.

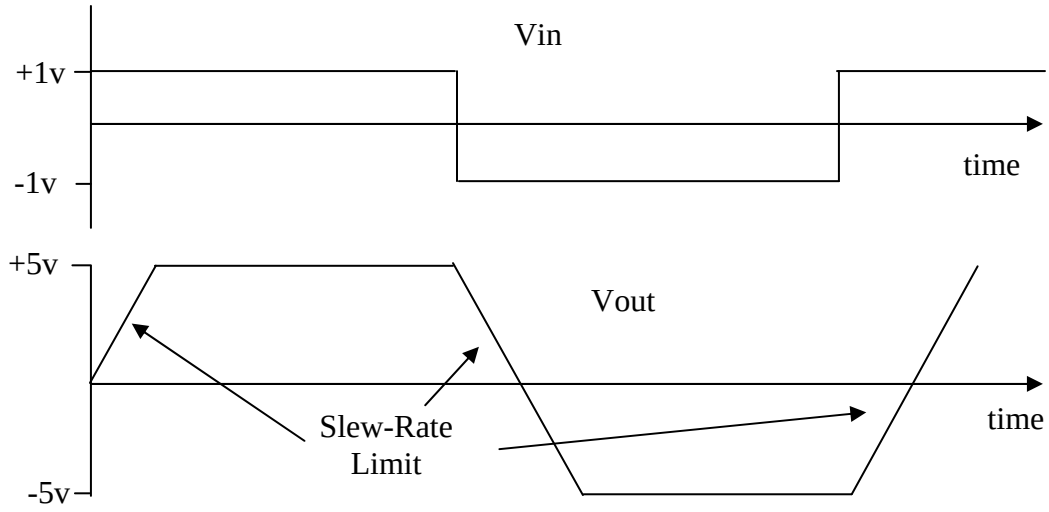


Figure 7: Vout for a square wave input showing the affect of slew-rate limit for a non-inverting amplifier with a gain of +5.

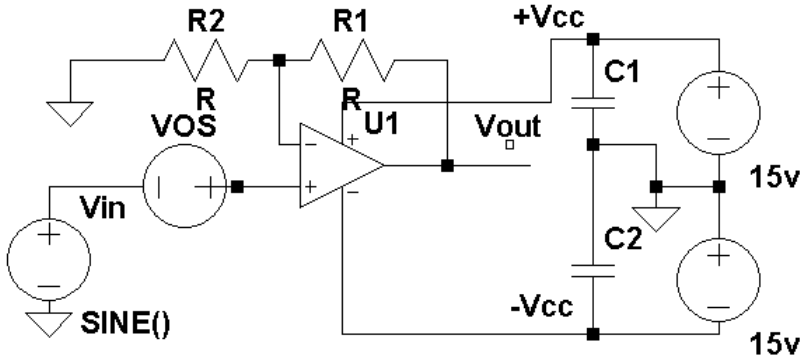


Figure 8: shows VOS place in series with the input signal Vin.

Consider the non-inverting amplifier of Figure 5. According to Equation (9), when Vin =0 volts, Vout should also be zero volts. But for a real op-amp, this is not the case; Vout is non-zero. This non-zero output voltage is the result of mis-matches in the internal amplifiers of the op-amp. Given this non-zero output voltage Vx, then it's effectively a voltage source commonly called the offset voltage (VOS) at the input given by

$$VOS = \frac{Vx}{\frac{R1}{R2}+1} \tag{11}$$

Figure 8 shows this voltage source VOS place in series with the input signal Vin.

Unity Gain Buffer or Voltage Follower

Equation (9) gives the voltage gain Av for the non-inverting amplifier. If R1 is set to 0 and R2 is set to infinity then Av reduces to 1. But R1 = 0 is the same as a wire and R2 equal to infinity is nothing more than an open. Figure 9 gives the schematic for a unity gain buffer. For this circuit Vout = Vin. Care must be taken when picking an op-amp for a unity gain buffer. Many op-amps are not stable for non-inverting gains less than 3-5. These op-amps tend to oscillate. The datasheet for a particular op-amp usually states if it's not unity gain stable.

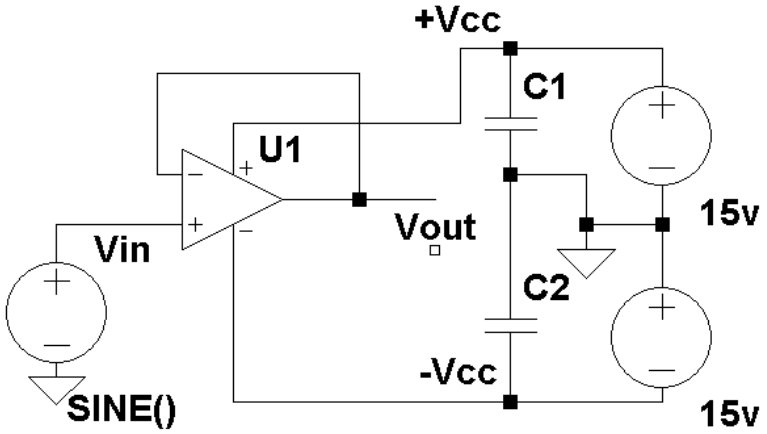


Figure 9: The schematic for a unity gain buffer amplifier.

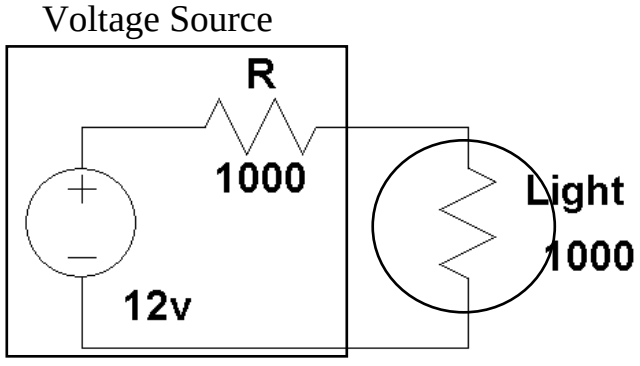


Figure 10: A 12 volt light bulb connected to a 1000 ohm 12 voltage source.

One of the interesting facts about a unit gain buffer is that its input current Iin is zero. Since the input impedance is defined as Zin = Vin / Iin and since Iin is zero then Zin is equal to infinity or is very large. An example of where a unity gain buffer is used is when a source has a high impedance value and it needs to drive a

low impedance load. Consider the following circuit of Figure 10. The voltage source has an internal resistance of 1000 ohms and is rated at 12 volts. It is desired to use this voltage source to turn on a 12-volt light bulb with an internal resistance of 1000 ohms. Using Ohm's Law the current through the light bulb is 12 volts / 2000 ohms and the voltage across the light bulb is 6 volts not 12 volts as required to light the light bulb (it's a 12 volt light bulb).

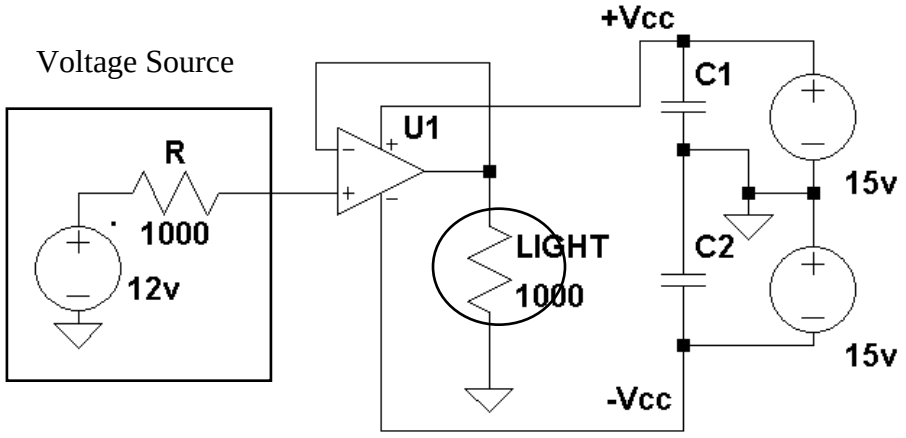


Figure 11: A 12 volt light bulb connected to a 1000 ohm 12 voltage source via a unity gain buffer.

Figure 11 shows using a unity gain buffer to light the light bulb. With this circuit, since the current into the op-amp is zero the voltage drop across the internal voltage source resistor is 0 and 12 volts appears at the input of the V+ terminal of the op-amp. Since this amplifier is a unity gain buffer Vout = Vin = 12 volts. The full 12 volts now appears across the 12 volt light bulb. As long as the maximum output current of the op-amp is not exceeded the voltage across the light bulb will remain at 12 volts. Unlike the circuit of Figure 10 where the voltage across light bulb dropped to 6 volts, the unity gain buffer circuit was able to maintain 12 volts across the light bulb.

Summing Amplifier

An application of the inverting amplifier is that of the summing amplifier shown in Figure 12. Given that plus terminal of the op-amp is at ground and the current into the op-amp terminal is zero the current flowing into R1 is equal to the sum of current due to each input.

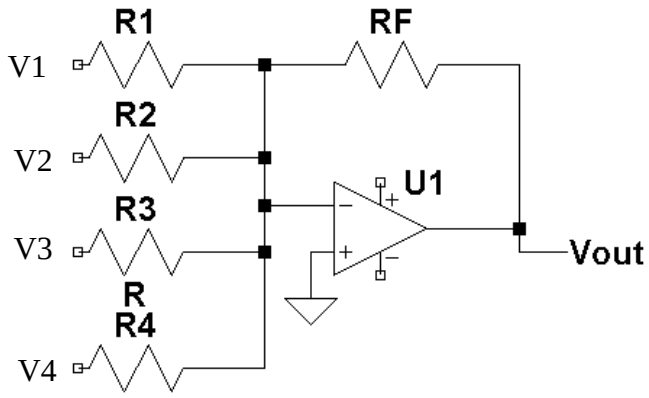


Figure 12: A schematic for a summing amplifier.

Equation (12) gives that the current through RF is equal to the sum of all of the current through R1, R2, R3, and R4.

$$IRF = IR1 + IR2 + IR3 + IR4 \tag{12}$$

Solving for each of the currents in terms of the voltage across each Resistor and substituting this into (12) gives:

$$\frac{0 - Vout}{RF} = \frac{V1-0}{R1} + \frac{V2-0}{R2} + \frac{V3-0}{R3} + \frac{V4-0}{R4} \tag{13}$$

and finally solving for Vout gives:

$$Vout = \frac{-RF}{R1} V1 + \frac{-RF}{R2} V2 + \frac{-RF}{R3} V3 + \frac{-RF}{R4} V4 \tag{14}$$

Equation (13) gives the output at op-amp as the weighted sum of the inputs V1, V2, V3 and V4. The summing amplifier of Figure 12 can be easily expanded to additional inputs by simply adding addition voltage source inputs and the appropriate resistors. For example for a two input summing amplifier with RF =3k ohms and R1 = 1K ohms and R2 = 3k ohms the following equation is implemented

$$Vout = -3\ V1 - V2 \tag{15}$$

Some comments about the schematic in Figure 12: This schematic skipped drawing the op-amp power supply that was drawn in the previous schematics of this lab. This does not mean for this circuit that the op-amp power supply is not needed. It is common to not to draw the op-amp power supply in a schematic so

as to make the schematic simpler to read, but the power supply still needs to be implemented as shown in the previous schematics including the 2 bypass capacitors. Also, the use of input voltage sources as shown in the previous schematics are drawn using a simple reference as V1, V2 etc., instead of the total symbol for a voltage source. Again this is done to make reading the schematic easier.

Op-amps driving capacitance loads

Op-amps do not like large capacitance load at the output Vout. This tends to make them unstable and having the possibility of the amplifier circuit oscillating. This typically occurs when an op-amp amplifier circuit tries to drive long cables (such as shielded cables). These cables tend to have a large capacitance per foot, which essentially connects a large capacitance directly to the output of the op-amp amplifier circuit. Figure 13 shows a slight modification of the non-inverting amplifier circuit that allows this amplifier to drive a large capacitance load. The resistor R place in series with the op-amp output Vout isolates the capacitance load of the capacitor. This resistor does not affect the voltage gain of this circuit. Since $V^+ = V^-$, the amplifier circuit will adjust its output so that the virtual short is maintained and Equations (9) and (10) are still valid. Typical values for this resistor is in the range of 50 to 1k ohms.

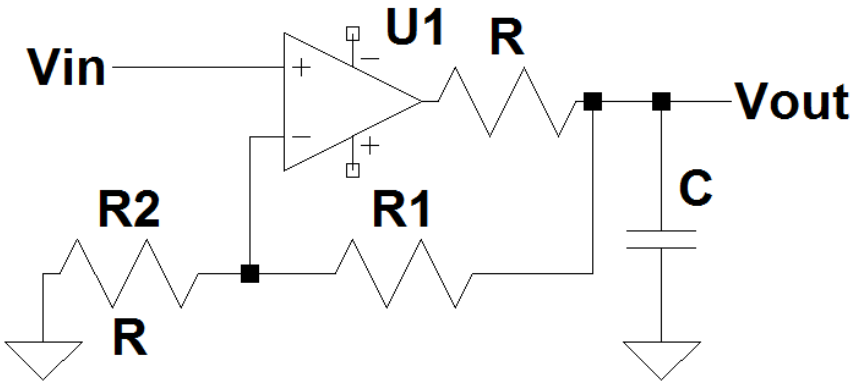


Figure 13: A schematic for a non-inverting amplifier adding a series resistor at the output of the op-amp for to drive a capacitance load.

Procedure:

General Setup:

1. Record the model and serial number of the scope, power supply, multimeter and function generator used in laboratory experiment.
2. Download the datasheet for the op-amp used. This will be needed to obtain its pin-out. When comparing datasheet data values to experimental data, use the typical values in the datasheet if given.

3. Make sure that the power supply to the op-amp is correctly wired as not to apply the incorrect polarity to the op-amp.
4. Initially set +Vcc = 15 volts and -Vcc to -15 volts
5. When measuring any values make sure to measure all inputs as well as the output of the circuit. Do not rely on the values indicated on the instruments. Always measure all signal values.
6. The output impedance of the signal generator is 50 ohms. If the generator is connected to a load other than 50 ohms, the displayed Amplitude, Offset, and High/Low values will be different than what is selected on the generator. Usually a factor of 2 larger.
7. Before turning any power on, double check the wiring to make sure that it is correct.
8. Measure all resistors that are used in the amplifier circuits using the multimeter and record these values
9. Use all measured values to determine experimental results, such as gain and current.
10. Comparing data means to calculate the percent difference between two values. For example, theoretical values versus measured values.
11. Comparing data graphically means to plot the data on the same plot to see how the data overlaps.

Inverting Amplifier:

1. Using the parts kit in the lab, build an inverting amplifier with a gain Av of -3. Use resistor values as small as possible but greater than 1k ohms.
2. Set +Vcc =15 volts and -Vcc = -15 volts
3. Measure all resistor values
4. Apply a 1-volt DC input to this circuit and measure both the input and output using the multimeter.
5. Compute the experimental gain Vout / Vin and compare it with the expected theoretical Gain for Av = -R1 / R2 using the measured values for R1 and R2.
6. Compute the current through R1 and R2 from the measured resistances and the measure voltages Vin, V^-, V^+ and Vout.
7. Compare the currents in R1 and R2 from step 5.
8. Repeat steps 4 and 5 for Vin = 0, 1.5, 2, and 3 volts and Vin = -1, -2, and -3 volts.
9. Generate a plot of Vout versus Vin from steps 4 and 8.
10. From the plot given in step 9 determine the maximum and minimum Vout obtainable.
11. Compare these two values of Step 10 to the values given in the datasheet from the Maximum Peak Output Voltage versus Supply Voltage.
12. Apply a 2-volt peak-to-peak, 200 hertz sine wave to the input and record from the oscilloscope the input and output waveforms.
13. Compare the phase between the input and output waveforms.
14. Repeat steps 12-13 for a gain Av = -10 for the inverting amplifier. Use resistor values as small as possible but greater than 1k ohms.

15. Using the same Av -10 inverting amplifier, apply a 0.05 volt peak sine wave. For various frequencies between 1000 Hz and 1 MHz obtain Vout and Vin and compute Av = Vout / Vin. Select frequencies with the value of 1X, 2X, and 5X factors for each decade of frequency.
16. Plot in dB Av (20 log(| Av |)) versus frequency.
17. Determine the frequency where the gain is down by -3dB.
18. Repeat steps 15 – 17 for a 2 volt peak-to-peak input.
19. Apply a 2-volt peak-to-peak square wave and measure the rise time of the output to determine the slew-rate of the op-amp (ΔVoltage / Δ Time = slope of the edge). Use the linear rising section to determine the slew rate. Zoom in on an edge with the oscilloscope to accurately measure the rise time.
20. Compare the measured slew-rate from step 19 to the value given in the data sheet.
21. Compare the measured value with Equations (6) and (7) for both 0.05 volt peak sine wave input and the 1 volt peak sine wave input.

Non-Inverting Amplifier:

1. Repeat steps 12 - 21 for the inverting amplifier section for the non-inverting amplifier except Av = +3 and Av = +11 instead of Av = -10.
2. Apply a 2 volt peak-to-peak, 200 Hz sine wave to the input of the, gain of 11, non-inverting amplifier with +Vcc =15 v and -Vcc = -15
3. Add a load resistor from the op-amp output Vout to ground.
4. Measure the peak output voltage from the op-amp for load resistors in the range of 100 ohms to 10k ohms. Use at least 5 different resistor values
5. Plot Vout peak-to-peak versus load resistance.
6. Compare this plot with the plot given in the data sheet (Maximum Peak Output Voltage versus Load Resistance).
7. Design and build a non-inverting amplifier with a gain of 1000. Set +Vcc = 15 volts and -Vcc = -15 volts. Use resistor values as small as possible but greater than 1k ohms.
8. Set Vin to 0 volts. The best way to do this is to disconnect Vin from the V+ terminal of the op-amp and tie the V+ terminal to ground.
9. Measure Vout. This value is the output due to VOS. Use Equation (11) to calculate VOS.
10. Compare the VOS measured in Step 9 to the value given in the datasheet.

Summing Amplifier:

1. Design and build a summing amplifier to implement Vout = -5 V1 - 2 V2. Use resistor values as small as possible but greater than 1k ohms.
2. Apply a 0.2-volt peak-to-peak, 200 Hz sine wave to V1 and a 1 volt DC input to V2.
3. Using an oscilloscope measure and record the output at Vout.
4. Repeat steps 1-3 for a DC inputs of -1 and 2 volts.

Unity Gain buffer.

1. Implement the Circuit given in Figure 10 using 1000-ohm resistors. Measure all resistors.
2. Measure the voltage across each resistor and calculate the current in each resistor.
3. What is the voltage across the 1k ohm resistor that represents the light bulb?
4. Build a unity gain buffer as given in Figure 11.
5. Measure the voltage across each resistor and calculate the current in each resistor.
6. What is the voltage across the 1k ohm resistor that represents the light bulb?
7. Build the unity gain buffer circuit given in Figure 13 with R at the output initially set to zero (a wire).
8. Connect a 0.001 microfarad capacitor to the output of the op-amp to ground.
9. Set Vin to 2.0-volt peak-to-peak, 1 KHz square wave. Using an oscilloscope measure and record the output at Vout.
10. Add a 1k ohm resistor as shown in Figure 13 for the resistor labeled R. Using an oscilloscope, measure and record the output at Vout. Record and note the change in Vout from step 12.
11. Disconnect the load 0.001 microfarad capacitor and set R back to zero ohms. Set +Vcc = +5 volts and -Vcc to -5 volts. Apply a DC input and measure the output Vout as Vin is varied from -5 Volts to + 5volts. Make sure to obtain at least 1 point at each integer voltage value. Use the signal generator as the input for this step. Set the voltage peak-to-peak to its minimum value of 20 millivolts and to change the DC value use different offset values on the generator.
12. Plot Vout versus Vin and discuss what is observed in the laboratory report.
13. Lookup the Common-Mode input Voltage range. If the inputs are allowed over the range of -Vcc to +Vcc then this operational amplifier is also referred to as a rail-to-rail input op-amp.

Report: Please follow the procedures in this laboratory manual for writing the report for this experiment. Include in your report:

1. The equipment used model and serial number.
2. Laboratory partners
3. Date and time data were taken.
4. Your laboratory report should include the goal of the laboratory experiment.
5. The procedures.
6. All calculations for each step.
7. All plots generated for each step.
8. All comparisons calculations.
9. All waveforms obtained in each step
10. For each data collection step in the procedure, there should be either data collected, a calculation performed or a waveform recorded. Please include these in the report.
11. Short summary discussing what is observed for each of the steps given in the laboratory experiment.

12. Also include what you learned.

Note: All schematics / Circuit diagrams for this laboratory experiment were generated using LTSpice IV.

EXPERIMENT #2

More Linear Operational Amplifier Applications

Goals:

To introduce the concepts of an operational amplifier (op-amp) used as a difference amplifier, an instrumentation amplifier, and a voltage-to-current converter. Data collected during this laboratory experiment will be compared to the theoretical equations for the appropriate circuits. Additionally an application for the difference amplifier will be presented.

References:

Microelectronics-Circuit Analysis and Design, D. A. Neamen, McGraw-Hill, 4th Edition, 2007, ISBN: 978-0-07-252362-1.

Equipment:

Oscilloscope: Tektronix DPO 4034B Mixed Signal
Function Generator: AFG3022B
Triple Power supply
TL081-TL084 family of operational amplifiers
2N2222A NPN transistor
Capacitors available in the laboratory
Resistors available in the laboratory

Pre-laboratory:

Read this laboratory experiment carefully to become familiar with the background and the procedural steps in this experiment. Carefully read each section and become familiar with the equations for each circuit.

Using the simulation package of your choice in which you are the most familiar with: Multisim, Workbench or LTSpice IV simulate the following circuits:

The equations required for gain A_V are given in the appropriate sections for the difference amplifier, instrumentation amplifier, and the voltage-to-current converter.

a. Design a gain Ad = 2 difference amplifier using a minimum of 1k-ohm resistors and the circuit diagram in Figure 3.
b. The difference amplifier needs two inputs V1 and V2. Simulate this difference amplifier time transient response for an input for V1 equal to a 1.0 volt 200 Hz sine wave and for V2 equal to a 1.0 volt 200 Hz sine wave but 180 degrees out of phase with the V1.

c. Plot the input voltages as well as the output voltage as a function of time.
d. Repeat steps b and c but this time set the phase difference between V1 and V2 to 0 degrees.
e. Repeat steps a, b, c, and d for a gain Ad = 4 difference amplifier.
f. Design a gain Ad = 2 instrumentation amplifier using a minimum of 1k-ohm resistors and the circuit diagram in Figure 5.
g. The instrumentation amplifier needs two inputs V1 and V2. Simulate this instrumentation amplifier time transient response for an input for V1 equal to a 1.0 volt 200 Hz sine wave and for V2 equal to a 1.0 volt 200 Hz sine wave but 180 degrees out of phase with the V1.
h. Plot the input voltages as well as the output voltage as a function of time.
i. Repeat steps g and h but this time set the phase difference between V1 and V2 to 0 degrees.
j. Repeat steps f, g, h, and i for a gain Ad = 4 instrumentation amplifier.
k. Design a voltage-to-current converter that produces an output of 1ma for every volt of input using a minimum of 1k-ohm resistors and the circuit diagram in Figure 6.
l. Simulate the voltage to converter designed in step k for V2 = 3 volts and Vin = 2 volts.
m. Vary V3 between 1 volt and 5 volts and plot Iout versus V3.

Discussion:

Consider the following design problem as shown in Figure 1. A voltage source is connected to a single ended amplifier in which a noise source is introduced onto the wire between the voltage source and the amplifier.

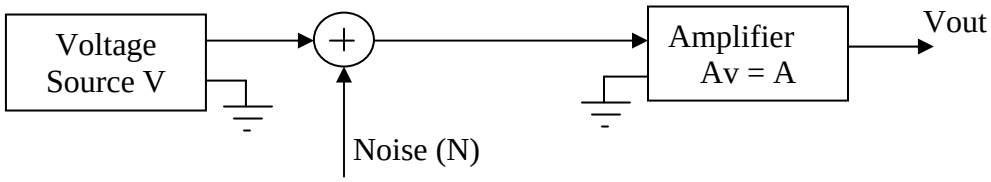


Figure 1: An example of a single ended amplifier with input noise and a gain of A.

The output voltage is then given by

$$Vout = (V + N) \cdot A = V \cdot A + N \cdot A \qquad (1)$$

The design issue is that the noise is introduced only onto the signal wire. If the layout of Figure 1 is modified, so that a second signal -V on a second wire is transmitted along with the original V in which both wires are collocated. Then any noise introduced on the wires is the same on both wires and the difference between the two signal lines produces a noise free output. Figure 2 shows the block diagram of this configuration. Since the noise is common to both wires,

taking the difference results in cancellation of the noise. This common noise of both wires is referred to as common mode noise.

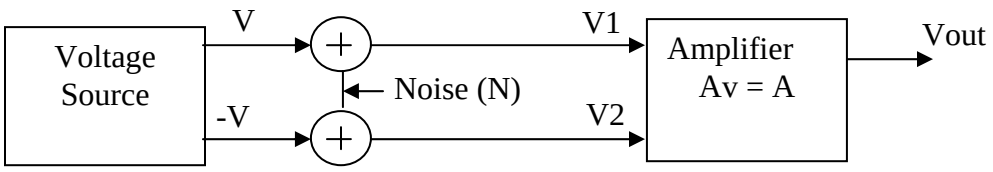


Figure 2: An example of a differential amplifier with input noise.

The amplifier used in Figure 2 is a difference amplifier with Vout defined as

$$Vout = Ad \cdot (V1 - V2) . \quad (2)$$

But V1 and V2 can be written in terms of the differential voltage sources as

$$V1 = (V + N) \quad (3)$$

And

$$V2 = (-V + N) \quad . \quad (4)$$

Substituting V1 and V2 into Equation 2 gives

$$Vout = Ad \cdot [\ (V + N\ ) - (-V + N)\ ] . \quad (5)$$

Which reduces to

$$Vout = Ad \cdot [\ 2 \cdot V + N\ -\ N\ ] = Ad \cdot 2 \cdot V \quad (6)$$

Vout contains twice the signal and no common mode noise. An example, where a difference amplifier is used is to remove 60 Hz noise for an audio system transmitted over a long cable. It is not uncommon to transmit an audio signal differentially and then use a difference amplifier at the receiving end to remove any common mode 60 Hz noise that might be injected in the cable.

Figure 3 gives the schematic of using a single op-amp to implement a difference amplifier. Vout depends on the four resistors R1 - R4:

$$Vout = V1 \ \frac{R4}{R3 + R4} \ \frac{R1 + R2}{R1} \ - \ V2 \ \frac{R2}{R1} \quad . \quad (7)$$

If the sum R1 + R2 is set equal to R3 + R4, then Equation (7) reduces to

$$\text{Vout} = \text{V1}\ \frac{\text{R4}}{\text{R1}}\ -\ \text{V2}\ \frac{\text{R2}}{\text{R1}} \quad . \tag{8}$$

Finally if R4 = R2, which implies R1 = R3, then equation simplifies to

$$\text{Vout} = \frac{\text{R2}}{\text{R1}}\ [\text{V1}\ -\ \text{V2}] \quad . \tag{9}$$

and Vout is equal to the difference of V1 and V2 with a differential gain

$$\text{Ad} = \frac{\text{R2}}{\text{R1}} \tag{10}$$

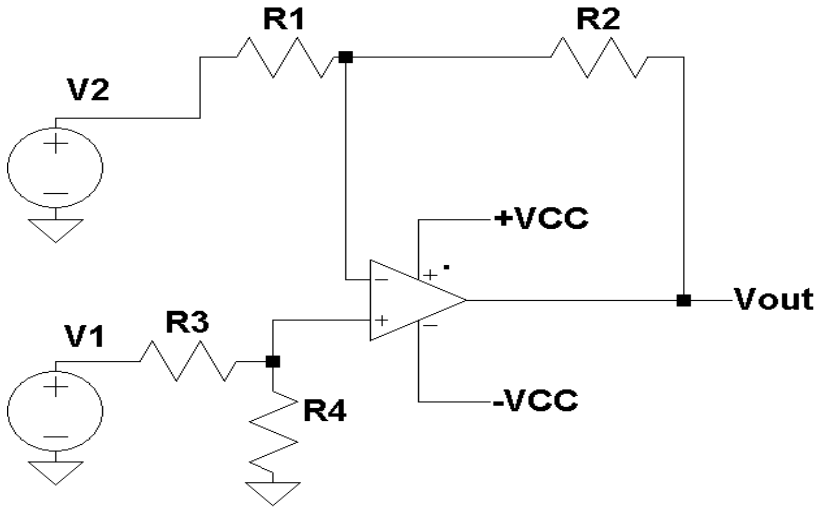


Figure 3: A single op-amp difference amplifier.

Ideally, if R1 perfectly matches R3 and R2 perfectly matches R4, when V1 equals V2 then Vout should be equal to zero. Unfortunately, this can not always be achieved with the resistor values that are selected. All resistors used have a finite tolerance value. This depends on the resistors used but the most common resistor tolerances are 1%, 5% and 10%. To verify the performance of a difference amplifier, V1 and V2 are set to a common voltage value of Vcm. The output is then measured. From Equation (7), with V1 = V2 = Vcm, Vout becomes

$$\text{Vout} = \text{Vcm}\left(\frac{\text{R4}}{\text{R3} + \text{R4}}\ \frac{\text{R1} + \text{R2}}{\text{R1}}\ -\frac{\text{R2}}{\text{R1}}\right) \quad . \tag{11}$$

Dividing both sides of Equation (11) by Vcc gives the common mode gain Acm as

$$Acm = \frac{Vout}{Vcm} = \left(\frac{R4}{R3 + R4} \frac{R1 + R2}{R1} - \frac{R2}{R1} \right) \quad . \tag{12}$$

Ideally, Acm should be zero. To find the output when V1 is not equal to V2 then V1 is set to Vd/2 and V2 is set to an equal and opposite value of -Vd/2. Substituting these values into Equation (7) gives

$$Vout = \frac{Vd}{2} \left(\frac{R4}{R3 + R4} \frac{R1 + R2}{R1} + \frac{R2}{R1} \right) \quad . \tag{13}$$

Dividing both sides by Vd, the difference mode gain Ad can be found

$$Ad = \frac{Vout}{Vd} = \left(\frac{R4}{R3 + R4} \frac{R1 + R2}{R1} + \frac{R2}{R1} \right) \quad . \tag{14}$$

Setting R1 = R3 and R2 = R4 gives a common mode gain of zero and a difference mode gain of Ad = R2 / R1. A measure of the performance of a difference amplifier is the ratio of the absolute value of difference mode gain to the absolute value of the common mode gain and commonly called the Common Mode Rejection Ratio (CMRR):

$$CMRR = 20 \log_{10} \left(\frac{|Ad|}{|Acm|} \right) \quad . \tag{15}$$

The CMRR is commonly given in Decibels and higher the value the better the performance of the difference amplifier. Since operational amplifiers are essentially difference amplifiers, the datasheet associated with the op-amp usually specifies the op-amps CMRR. One important fact of the op-amps is that the CMRR is a function of the frequency of operations and the CMRR tends to decrease in value as the frequency of operation increases as shown in Figure 4.

The main limitations of the difference amplifier given in Figure 2 is that the input impedance is not very high and the input impedance of the two inputs is not the same. The input impedance for the V1 input is

$$Z(V1) = R3 + R4 \tag{16}$$

and for the V2 is

$$Z(V2) = R1 \quad . \tag{17}$$

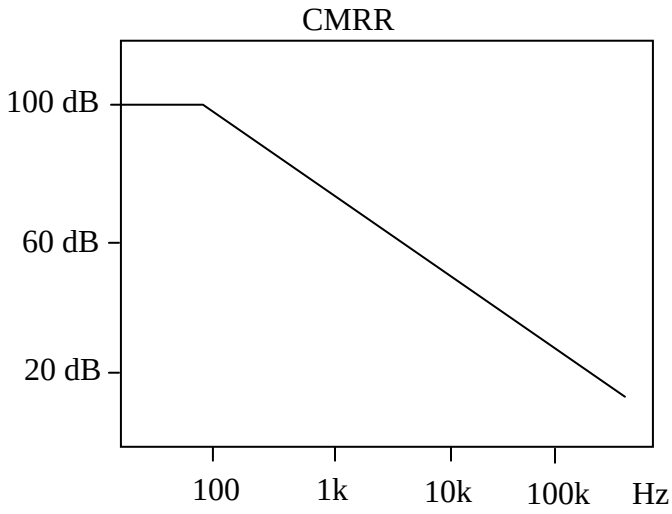


Figure 4: A typical plot of the CMRR of an op-amp as a function of frequency.

Another version of a difference amplifier where both inputs have high impedance is given in Figure (5). This amplifier is commonly referred to as an instrumentation amplifier. This amplifier contains the difference amplifier of Figure 3 and two additional op-amp stages. A closer look at the circuits shows that both V1 and V2 are tied directly to the non-inverting input of these two op-amps. Since the input impedance is very high, the current into an op-amp is approximately zero.

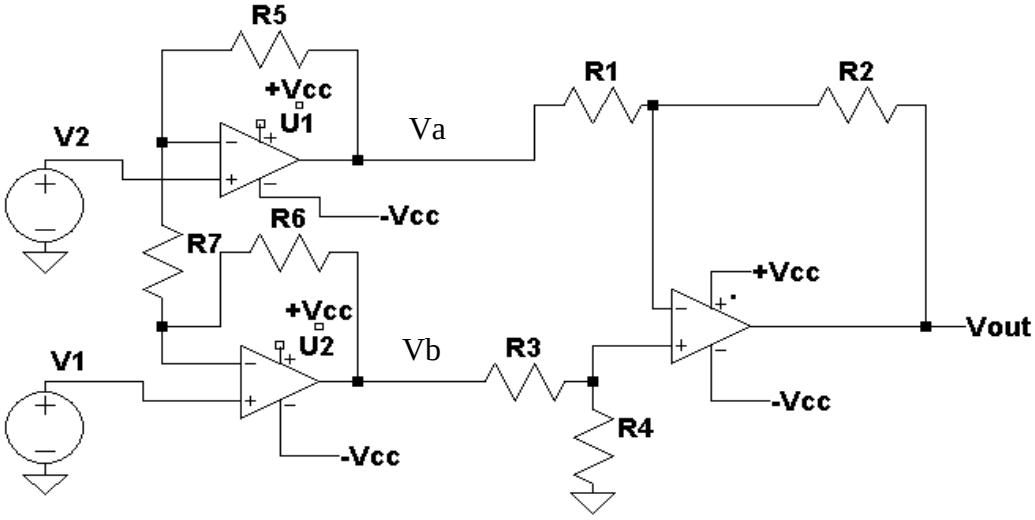


Figure 5: An instrumentation amplifier designed using three op-amps.

The voltage Va for this amplifier is given as

$$Va = V2\left(\frac{R5}{R7} + 1\right) - V1\frac{R5}{R7} \quad . \tag{18}$$

and for Vb as

$$Vb = V1\left(\frac{R6}{R7} + 1\right) - V2\frac{R6}{R7} \quad . \tag{19}$$

Since the right most stage of Figure 5 is a difference amplifier, Vout is found by substituting Va for V2 and Vb for V1 into Equation (7)

$$Vout = \left(V1\left(\frac{R6}{R7} + 1\right) - V2\frac{R6}{R7}\right) \cdot \left(\frac{R4}{R3 + R4}\ \frac{R1 + R2}{R1}\right) -$$

$$\left(V2\ \left(\frac{R5}{R7} + 1\right) - V1\frac{R5}{R7}\right)\ \frac{R2}{R1} \quad . \tag{20}$$

Rearranging and combining V1 and V2 gives

$$Vout = V1\left(\left(\frac{R6}{R7} + 1\right) \cdot \left(\frac{R4}{R3 + R4}\ \frac{R1 + R2}{R1}\right) + \frac{R5}{R7}\frac{R2}{R1}\right) -$$

$$V2\ \left(\frac{R6}{R7}\left(\frac{R4}{R3 + R4}\ \frac{R1 + R2}{R1}\right) + \frac{R2}{R1}\left(\frac{R5}{R7} + 1\right)\right) \quad . \tag{21}$$

Using a similar approach to find Equation (11), the common mode gain is given by

$$Acm = \frac{Vout}{Vcm} = \left(\frac{R6}{R7} + 1\right) \cdot \left(\frac{R4}{R3 + R4}\ \frac{R1 + R2}{R1}\right) + \frac{R5}{R7}\frac{R2}{R1} -$$

$$\frac{R6}{R7}\left(\frac{R4}{R3 + R4}\ \frac{R1 + R2}{R1}\right) + \frac{R2}{R1}\left(\frac{R5}{R7} + 1\right) \quad . \tag{22}$$

Ideally, Acm should be zero. To find the output when V1 is not equal to V2 then V1 is set to Vd/2 and V2 is set to and equal and opposite value of -Vd/2. Substituting these values into Equation (21) gives

$$Ad = \frac{Vout}{Vd} = \frac{1}{2}\left(\left(\frac{R6}{R7} + 1\right) \cdot \left(\frac{R4}{R3 + R4}\ \frac{R1 + R2}{R1}\right) + \frac{R5}{R7}\frac{R2}{R1}\right) +$$

$$\frac{1}{2}\left(\frac{R6}{R7}\left(\frac{R4}{R3 + R4}\ \frac{R1 + R2}{R1}\right) + \frac{R2}{R1}\left(\frac{R5}{R7} + 1\right)\right) \quad . \tag{23}$$

Once the common mode gain Acm and the difference mode gain are known, the

common mode rejection ratio becomes Common Mode Rejection Ratio is found using the same equation that was used for the difference amplifier

$$\text{CMRR} = 20 \log_{10}\left(\frac{|\text{Ad}|}{|\text{Acm}|}\right) \quad . \tag{24}$$

For the special case when R6 = R5 and R1 = R3 and R2 = R4, Vout can then be written from Equation (21) as

$$\text{Vout} = \text{V1}\left(\left(\frac{\text{R6}}{\text{R7}} + 1\right)\cdot\left(\frac{\text{R2}}{\text{R1}}\right) + \frac{\text{R6}}{\text{R7}}\frac{\text{R2}}{\text{R1}}\right) -$$

$$\text{V2}\left(\frac{\text{R6}}{\text{R7}}\left(\frac{\text{R2}}{\text{R1}}\right) + \frac{\text{R2}}{\text{R1}}\left(\frac{\text{R6}}{\text{R7}} + 1\right)\right) \quad . \tag{25}$$

Combining terms gives

$$\text{Vout} = \text{V1}\left(\frac{2\cdot\text{R6}}{\text{R7}} + 1\right)\cdot\frac{\text{R2}}{\text{R1}} - \text{V2}\left(\frac{2\cdot\text{R6}}{\text{R7}} + 1\right)\cdot\frac{\text{R2}}{\text{R1}} \tag{26}$$

or

$$\text{Vout} = \frac{\text{R2}}{\text{R1}}\left(\frac{2\cdot\text{R6}}{\text{R7}} + 1\right)\cdot[\text{V1} - \text{V2}] \tag{27}$$

Equation (27) illustrates that Vout is simply the difference between V1 -V2 with a difference gain of

$$\text{Ad} = \frac{\text{R2}}{\text{R1}}\left(\frac{2\cdot\text{R6}}{\text{R7}} + 1\right) \tag{28}$$

The last linear op-amp circuit that will be discussed in this laboratory experiment is that of the voltage- to-current converter. The input to this circuit is voltage and the output is current. Figure 6 gives the schematic diagram for this circuit. Given the fact that there is a virtual short between the plus and minus inputs of the op-amp and with V+ = Vin, the voltage on across R2 is simply Vin (V+ = V- = Vin).

The current through R2 is then Vin / R2. The current, I2, through R2 is also the emitter current flowing in the transistor. The relationship of the current flowing in a transistor between the base, emitter, and collector are

$$\text{Ic} = \beta\,\text{Ib} \tag{29}$$

$$\text{Ie} = \text{Ic} + \text{Ib} = (\beta + 1)\,\text{Ib} \tag{30}$$

and

$$Ic = \frac{\beta}{\beta+1} Ie \quad , \tag{31}$$

where β is the current gain of the transistor.

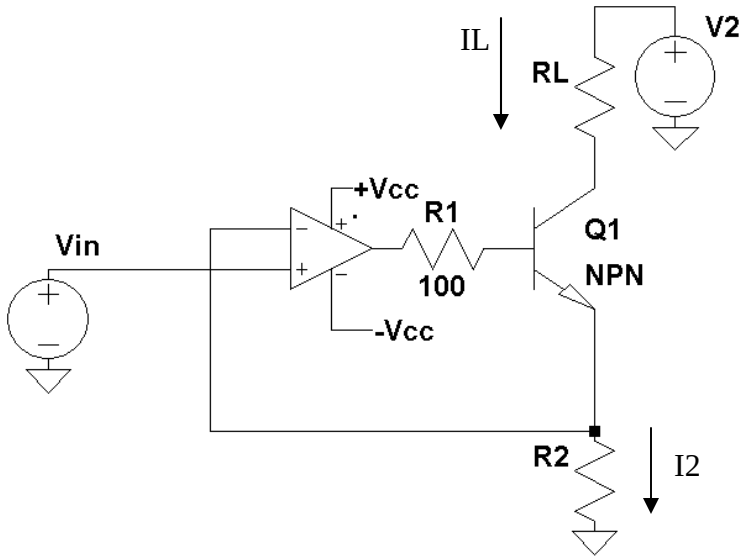


Figure 6: The schematic diagram for a voltage to current converter.

Since Ie = I2 in Figure 6, then Ic is given by

$$Ic = \frac{\beta}{\beta+1} I2 \quad , \tag{32}$$

but I2 = Vin / R2

$$Ic = \frac{\beta}{\beta+1} \frac{Vin}{R2} \quad , \tag{33}$$

The collector current is equal to the input voltage Vin divided by R2. If β is large, on the order of 100, then

$$\frac{\beta}{\beta+1} \approx 1 \tag{34}$$

and Equation 33 then reduces to

$$Ic = \frac{Vin}{R2} = IL \quad . \tag{35}$$

The output IL is simply Ic the collector current. The output current depends only on the input voltage and R2 provided that the voltage across the resistor is less V2 - VCE(SAT)) (the saturation voltage VCE(SAT) is the minimum voltage that exist across the collector to the emitter). The second criteria is that voltage across R2 must be less than the maximum output voltage of the op-amp Vout(MAX) - Vbe - Ib *100. Typically Ib (typically about 100x smaller than Ic) is very small and the maximum voltage across R2 must be less than Vout(MAX)- Vbe. The 100 ohm resistor R1 between the base and the output of the op-amp is used to isolate the base to emitter capacitance from appear right at the output of the op-amp (See Laboratory experiment #1).

Procedure:

General Setup:

1. Record the model and serial number of the scope, power supply, multimeter and function generator used in laboratory experiment.
2. Download the datasheet for the op-amp used. This will be needed to obtain the pin-out of the op-amp used. When comparing datasheet data values to experimental data use the typical values in the datasheet if given.
3. Make sure that the power supply to the op-amp is correctly wired as not to apply the incorrect polarity to the op-amp.
4. Initially set +Vcc = 15 volts and -Vcc to -15 volts
5. When measuring any values make sure to measure all inputs as well as the output of the circuit. Do not rely on the values indicated on the instruments. Always measure all signal values.
6. The output impedance of the signal generator is 50 ohms. If the generator is connected to a load other than 50 ohms, the displayed Amplitude, Offset, and High/Low values will be different than what is selected on the generator. Usually a factor of 2 larger.
7. Before turning any power on double check the wiring to make sure that it is correct.
8. Measure all resistors that are used in the amplifier circuits using the multimeter and record these values.
9. Use all measured values to determine experimental results such as gain and current.
10. Comparing data means to calculate the percent difference between two values. For example, theoretical values versus measured values.
11. Comparing data graphically means to plot the data on the same plot to see how the data overlaps.
12. Obtain the pin out for the 2N2222 transistor

Difference Amplifier:

1. Using the parts kit in the lab, design the difference amplifier of Figure 3 with a gain of Ad = 2 using 1k ohm resistors for R1 and R3.
2. Measure with the multimeter the actual resistance values.
3. Compute Acm and Ad using Equations (12) and (14).
4. Also calculate the CMMR using Equation (15).
5. Build the gain of Ad = 2 difference amplifier.

6. Setting V1 = V2 = 20 volt peak-to-peak 200 Hz sine wave measure Vout.
7. Calculate from step 6 Acm = Vout / V1.
8. Varying the frequency of the function generator from 100 Hz to 100 kHz repeat steps 6, and 7. Use measured values at frequencies of 1X, 2X and 5X for each decade.
9. Setting V1 = 1 volt peak-to-peak 200 Hz sine wave and V2 = -V1. To generate V2 = -V1, build an inverting amplifier[1] with a gain equal to –1. Apply the function generator to V1 input to the difference amplifier and to the inverting amplifier. The output of the inverter is now equal to -V1 and can be applied to V2 input to the difference amplifier.
10. Measure Vout from step 9.
11. Calculate Ad from step 9 (Ad = Vout / (2 · V1).
12. Using Equation (15) calculate the CMRR from Acm from Step 7 and Ad from Step 10.
13. Compare step 12 to step 4.
14. Discuss in the laboratory report the result of step 13.
15. Varying the frequency of the function generator from 100 Hz to 100 kHz repeat steps 9, 10, and 11. Use measured values at frequencies of 1X, 2X and 5X for each decade.
16. From steps 14, 15 calculate CMRR as a function of frequency.
17. From steps 14, 15 and 16 plot Acm, Ad, CMRR as a function of Frequency.
18. Decrease the value of R4 by 15 % to 20 %. Add a 10K ohm variable resistor in series with this new value of R4. One side of the variable resistor to R4 and the middle connection to ground. See Figure 7.
19. Setting V1 = V2 = 20 volt peak-to-peak 200 Hz sine wave measure Vout. Adjust this variable resistor (potentiometer) to yield the smallest value for Vout. Adjust R4 to best match R2 (This is the optimum setting).
20. Repeat steps 6,7, 9, 10, and 11 with this optimum setting for the potentiometer.
21. Build a gain of Ad = 4 difference amplifier.
22. Repeat steps 6, 7, 9, 10, and 11 for the difference amplifier of step 21.
23. Build the test circuit shown in Figure 8 with a gain of Ad = 4 for the difference amplifier. This allows for two voltage sources to be applied to V1 and V2 of the difference amplifier. The op-amp circuit of U2 inverts V1 adding 180 degree phase shift. U1 and U3 are unity gain summers, summing V2 and V1 to produce two signals into the difference amplifier:

$$\text{Vout(U1)} = - \text{V1} - \text{V2} \tag{36}$$

$$\text{Vout(U3)} = + \text{V1} - \text{V2} \tag{37}$$

24. Set V1 to a 0.5 volt peak-to-peak 200 Hz sine wave. Also set V2 to a 0.5 volt peak-to-peak 20 Hz sine wave.
25. Measure and record with oscilloscope the outputs U1 and U2 op-amp stages.

[1] You can also use Channel B of the function generator and change the phase to 180°. Remember to phase-lock ("track phase") the two channels prior to setting the phase angle, otherwise, the two channels' phases won't be aligned. Check with the o-scope.

26. Measure and record Vout with the Oscilloscope.
27. Discuss in the laboratory report the results of steps 25 and 26.

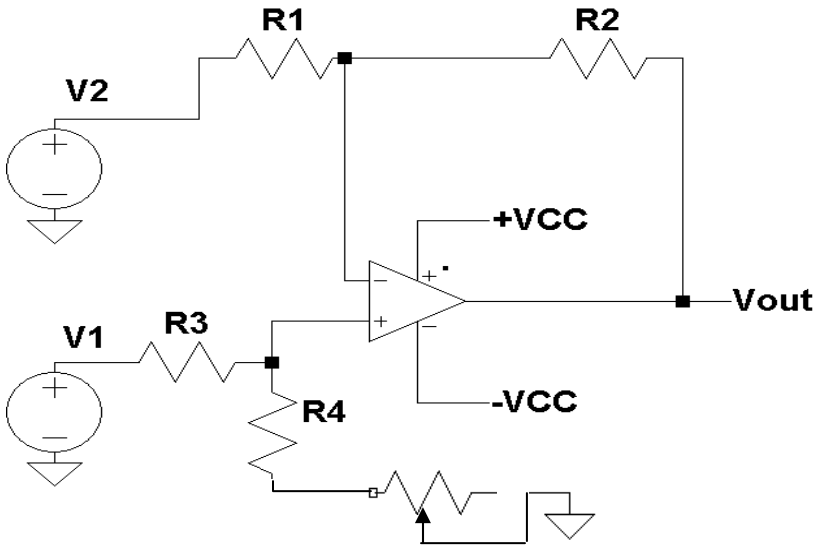


Figure 7. A difference amplifier with a variable resistor to optimize the resistors used.

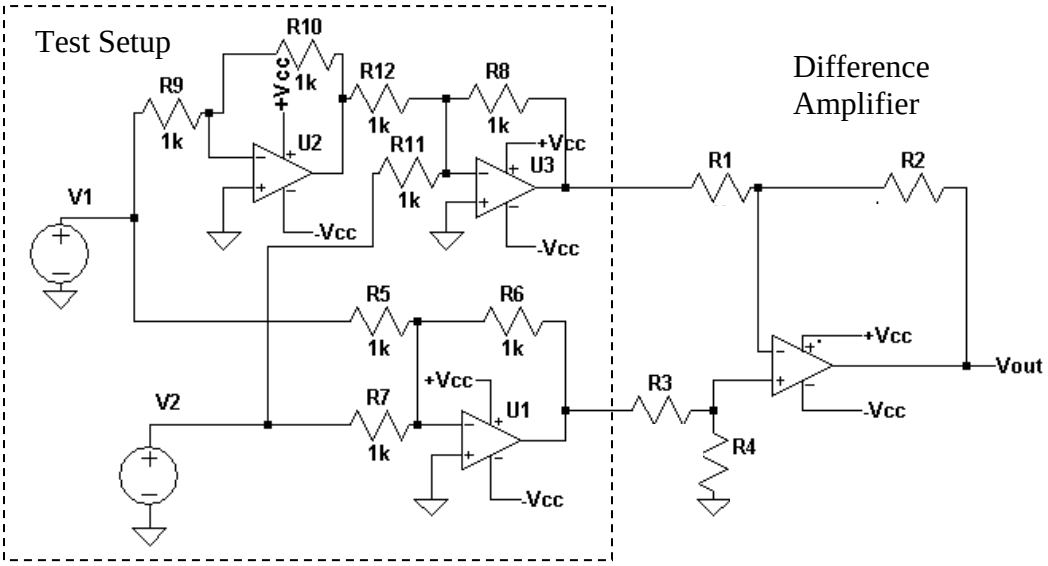


Figure 8: The schematic diagram to test a one op-amp difference amplifier.

Instrumentation Amplifier:

1. Using the parts kit in the lab, build the instrumentation amplifier of Figure 5 with a gain of Ad = 2 using 1k ohm resistors for R21, R3, and R7.
2. Measure with the multimeter the actual resistance values.

3. Compute Acm and Ad using Equations (22) and (23).
4. Also calculate the CMMR using Equation (15).
5. Setting V1 = V2 = 20 volt peak-to-peak 200 Hz sine wave measure Vout.
6. Calculate from step 5 Acm = Vout / V1.
7. Setting V1 = 1 volt peak-to-peak 200 Hz sine wave and V2 = -V1. To generate V2 = -V1, build an inverting amplifier[2] with a gain equal to -1. Apply the function generator to V1 input to the difference amplifier and to the inverting amplifier. The output of the inverter is now equal to -V1 and can be applied to V2 input to the difference amplifier.
8. Measure Vout from step 7.
9. Calculate Ad from step 8 (Ad = Vout / (2 · V1).
10. Using Equation (24) calculate the CMRR from Acm from Step 6 and Ad from Step 9.
11. Compare step 10 to step 4.
12. Discuss in the laboratory report the result of step 11.
13. Varying the frequency of the function generator from 100 Hz to 100 kHz repeat steps 5, and 6. Use measured values at frequencies of 1X, 2X and 5X for each decade.
14. Varying the frequency of the function generator from 100 Hz to 100 kHz repeat steps 7, 8, and 9. Use measured values at frequencies of 1X, 2X and 5X for each decade.
15. From steps 13 and 14 calculate CMRR as a function of frequency.
16. From steps 13, 14, and 15 plot Acm, Ad, CMRR as a function of Frequency.

Voltage to Current Converter:

1. Design and build the voltage to current converter given in Figure 6 for a conversion factor of 1milliamp of out for one volt of input.
2. Using a load resistance of RL = 1k ohms and V2 = 15 volts measure the voltage across R2 and RL for Vin = 1 volt
3. Compute the current in RL and R2 from step 2.
4. Varying the input from 0 to 5 volts, repeat steps 2 and 3. Make sure there is at least 5 points measured per integer voltage value.
5. Plot IL versus Vin from step 4. Is the curve linear?
6. Setting Vin to 2 volts measure IL as a function of V2 with V2 varying from 1 volt to 5 volts.
7. Plot IL versus V2.
8. Setting Vin to 2 volts and V2 to 5 volts measure Vin with RL varying from 100 ohms to 2k ohms. Use at least 5 different resistor values for RL.
9. Plot IL versus RL.

Report: Please follow the procedures in this laboratory manual for writing the report for this experiment.

1. The equipment used model and serial number.

[2] You can also use Channel B of the function generator to generate V2 – see Footnote 1.

2. Laboratory partners
3. Date and time data was taken.
4. Your laboratory report should include the goal of the laboratory experiment.
5. The procedures.
6. All calculations for each step.
7. All plots generated for each step.
8. All comparisons calculations.
9. All waveforms obtained in each step
10. For each data collection step in the procedure, there should be either data collected, a calculation performed, a waveform recorded. Please include these in the report.
11. Short summary discussing what is observed for each of the steps given in the laboratory experiment..
12. Also include what you learned.
13. For the difference amplifier compare the theoretical CMMR versus the measured CMRR.
14. Discuss the frequency plots of CMMR versus frequency for the difference amplifier.
15. Look up for the op-amp used in this laboratory experiment the CMRR.
16. Discuss in this laboratory report the results of steps 25 and 26 for the difference amplifier.
17. For the instrumentation amplifier compare the theoretical CMMR versus the measured CMRR
18. Discuss the frequency plots of CMMR versus frequency for the instrumentation amplifier
19. Is the curve linear for IL versus Vin?

Note: All schematics / Circuit diagrams for this laboratory experiment was generated using LTSpice IV.

EXPERIMENT #3

Linear Voltage Regulators

Goals:

To introduce the concepts of a linear voltage regulator and their use to maintain a regulated voltage output. Data collected during this laboratory experiment will be compared to the datasheet for the parts used.

References:

Microelectronics-Circuit Analysis and Design, D. A. Neamen, McGraw-Hill, 4th Edition, 2007, ISBN: 978-0-07-252362-1.

Equipment:

Triple Power supply
TL081-TL084 family of operational amplifiers
2N2222A NPN transistor
Capacitors available in the laboratory
Resistors available in the laboratory
Multimeter
7805 and 7812 linear three terminal regulators

Pre-laboratory:

Read this laboratory experiment carefully to become familiar with the background and the procedural steps in this experiment. Carefully read each section and become familiar with the equations for each circuit.

Using the simulation package of your choice in which you are the most familiar with: Mulitsim, Workbench or LTSpice IV simulate the linear regulator of Figure 2.

a. Pick R1 and R2 such that Vout is 3 volts. The minimum values for R1 and R2 should be 1000 ohms.
b. Set RL = 100 ohms and Vin = 6 volts. Measure with the simulator Vout.
c. Measure IL and Iin. Calculate Pin, Pout and Preg.
d. Calculate the Efficiency = Pout / Pin · 100%.
e. Vary RL from 50 to 10k ohms and measure Vout and IL.
f. Plot Vout versus IL
g. Setting RL to 1k ohms vary Vin from 0 to 6 volts.
h. Plot Vout versus Vin
i. What is the dropout voltage for this regulator.
j. Lookup the data sheet for the 7805 and 7812 (LM340) voltage regulators

k. Find the typical output voltages.
l. Find the dropout voltage and calculate the minimum allowed input voltage Vin for the 7805 and 7812 voltage regulators.
m. Find the peak output current.
n. Find the maximum allowed power dissipation of the regulator at room temperature and with no heatsink (assume a TO220 case).
o. Find the load regulation.
p. Find the thermal resistance of the voltage regulator.

Discussion:

Consider the following circuit given in Figure 1. With R1 equal to 100 ohms Vout is equal to 10.9 volts. If R1 is changed to 10 ohms, then Vout is equal to 6 volts. Vout depends on the load resistor R1. In other words, the output voltage decreases as the load current (the current through R1) increases. In many applications it is desirable to have a constant voltage source that is independent of load current. For example, the +Vcc and -Vcc input to a typical op-amp circuit should remain constant independent of the op-amp current.

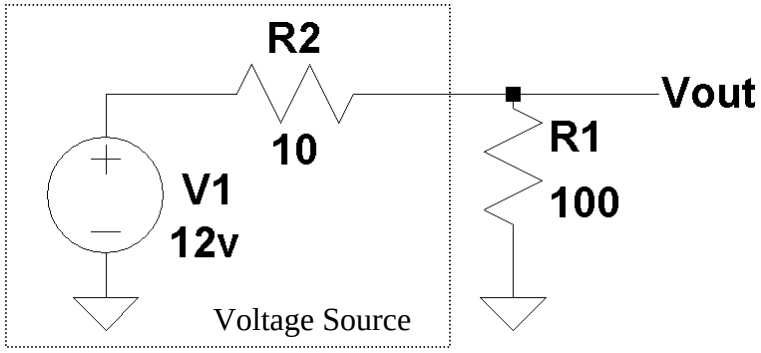


Figure 1: An example of a 12-volt voltage source with an internal resistance of 10 ohms.

A circuit that maintains a constant output voltage is called a regulator. There are two types of voltage regulators that are available. Those that work at a DC or constant operation point (known as linear regulators) and those that are based. upon varying a duty cycle of a pulse (known as a switching regulator). This laboratory experiment will focus on linear regulators. Switching regulators will be discussed in a later laboratory experiment.

Figure 2 gives the circuit diagram for a linear regulator. This regulator uses a 2N2222 transistor and an op-amp to perform the output regulation. It is based upon the requirement that the op-amp will try to adjust its output so as to keep its inputs, V^+ and V^-, equal. The voltage at the V^+ terminal is

$$V^+ = Vcc \frac{R4}{R3 + R4} \quad (1)$$

Assuming +Vcc =15v and -Vcc = -15v, then V^+ = 1.485 volts. The op-amp will adjusts its output voltage so that V^- terminal is the same as V^+. Since the output from the regulator Vout is equal to voltage output of the opamp -Vbe, the output of the regulator also changes. Given that the V^- terminal is related to Vout as

$$V^- = Vout \frac{R2}{R1 + R2} \tag{2}$$

then setting $V^+ = V^-$ gives

$$V^- = Vout \frac{R2}{R1 + R2} = Vcc \frac{R4}{R3 + R4} \tag{3}$$

Solving for Vout

$$Vout = Vcc \frac{R1 + R2}{R2} \frac{R4}{R3 + R4} \tag{4}$$

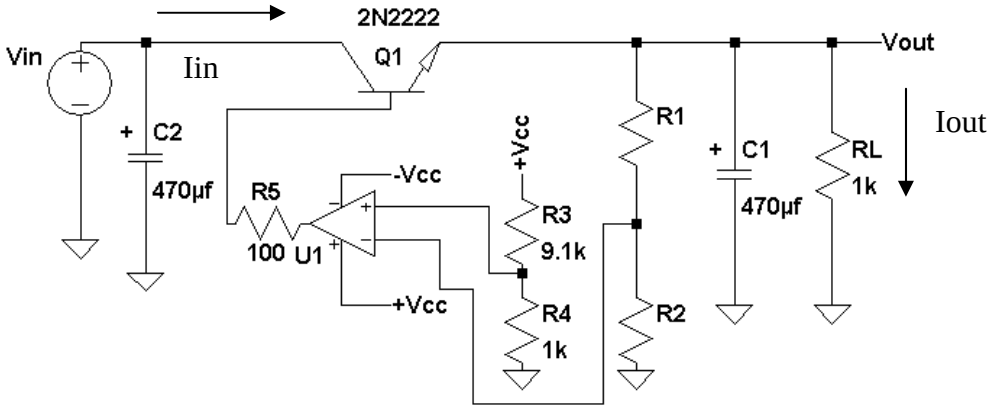


Figure 2: An example of a linear regulator.

For +Vcc = 15 volts, R3 = 9.1K, and R4 = 1k Vout becomes

$$Vout = 1.485v \frac{R1 + R2}{R2} \tag{5}$$

From Equation (5) Vout does not depend on the load current, as was the case for the circuit given in Figure 1.

Here's how the regulator in Figure 2 maintains a constant voltage at Vout. Assume Vout drops below its regulated voltage given by Equation (4) or (5). Then the V^- terminal voltage will be less then the V^+. Since the voltage output of the op-amp is Aod (V^+ - V^-), the voltage output from the op-amp will increase in

the positive direction ($V^+ > V^-$). This increasing voltage will raise the voltage on the base of the transistor. Since Vbe is a constant (about .7 volts), Vout will increase. Vout increases until $V^+ = V^-$. Now consider that Vout increases in voltage beyond regulated voltage given in Equation (4). For this case V^+ will be less than V^-. Since the voltage output of the op-amp is Aod ($V^+ - V^-$), the voltage output from the op-amp will tend to decrease in value. This lowers the voltage on the base of the transistor, which lowers the transistor's emitter voltage and lowers Vout.

As a final note, R5 is used to limit the current out of the op-amp and capacitors C1 and C2 are bypass capacitors used to maintain low AC impedance path to ground from Vin and Vout. These capacitors are used to eliminate any AC signals from appearing on Vin and Vout so the output of the regulator is a constant DC value.

The regulator of Figure 2 is a simple regulator with no short circuit or thermal protection. The linear regulator of Figure 2 is available in a three terminal part with both thermal and short circuit protection. Figure 3 gives the circuit diagram for this regulator. One set of linear regulators that are commonly used is the 78XX three terminal linear regulator family, where XX gives the output voltage of the regulator. Both the input and output voltages of these regulators are positive. For example, a 7805 voltage regulator produces an output voltage +5 volts. For negative output voltages, the 79XX regulators are available.

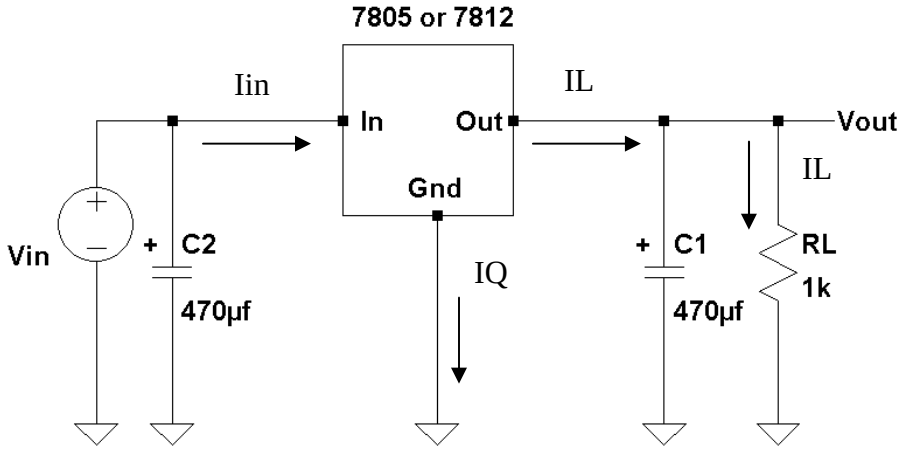


Figure 3: An example of a three terminal linear voltage regulator.

There are several parameters that are important when dealing with a linear regulator:

$$Iin = IL + IQ \qquad (6)$$

IQ is the regulator quiescent current and typically is milliamps. If the load current is much larger than IQ then Iin ≈ IL and IQ can be ignored in the following equations.

$$Pin = Vin \cdot Iin = Vin \cdot (IL + IQ) \quad (7)$$

$$Pout = Vout \cdot IL \quad (8)$$

$$Preg = Pin - Pout = (Vin - Vout)\, IL + IQ\, Vin \quad (9)$$

Where Pin is the input power, Pout is the output power, and Preg is the power dissipated in the regulator. The efficiency of a voltage regulator defines the percentage of power that is delivered to the load and is given by

$$Efficiency = \frac{Pout}{Pin} 100\% \quad . \quad (10)$$

The main objective of a voltage regulator is to maintain a constant voltage over various load currents. One parameter of importance is the load regulation parameter. This parameter gives the change in Vout as the regulator's output current, IL, is varied from a minimum to a maximum current. From Equation (9), the power dissipated in the regulator is proportional to the voltage across the regulator. To minimize the power dissipated in the regulator, the goal is to use as minimum a voltage across it as possible. Another parameter of importance is the minimum allowable voltage across the regulator for the regulator to maintain a constant output voltage. In other words the regulator is still in regulation. This minimum voltage across the regulator is known as the dropout voltage Vdo.

As with any electronic parts, there are maximum ratings that must be adhered to, such as the maximum input voltage, the maximum allowable load current, the maximum power dissipation allowed and the maximum operating temperature. Finally, since these parts are short circuit protected, the maximum short circuit current is also given. As long as the maximum power dissipation and maximum operating temperature are not exceeded the part will operate indefinitely with its output shorted to ground.

There are several items that will destroy one of these three-terminal regulators even if these parts are correctly installed in the circuit diagram of Figure 3 and the maximum rating are adhere to. The first is applying the wrong polarity voltage at the input. The second is having Vout be greater than Vin. This can occur if C1 > C2 and the energy storage in the output is greater than the energy storage in the input. This commonly occurs during power off if C1 > C2. The input to regulator will discharge toward zero volts faster than the output. Figure 4 shows a solution to protecting the regulator should Vout become greater than Vin. Under normal use, Vin > Vout, and the diode is reversed biased. Should Vout become greater than Vin, the diode is forward biased preventing any current flowing into the regulators from its output.

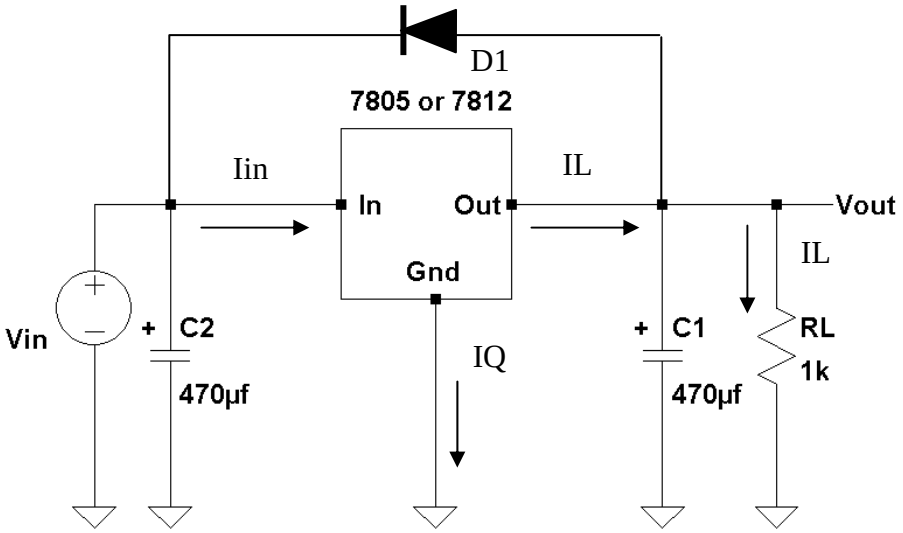


Figure 4: An example of a linear voltage regulator with protection.

The three terminal regulators can also be made to be adjustable so any desired regulated output voltage can be obtained. The only requirement is that the minimum voltage is that of the part itself. For example, a 7805 regulator can be made adjustable, but its minimum output voltage is 5 volts. Figure 5 gives the circuit required to make a three-terminal linear regulator adjustable. For this discussion, assume the regulator output voltage is Vreg (the voltage between the output and the ground pins of the regulator). Then IR1 is then given by

$$IR1 = \frac{Vreg}{R1} \quad . \tag{11}$$

and the voltage across R2 (VR2) is

$$VR2 = R2\,(IQ + IR1) = R2\left(IQ + \frac{Vreg}{R1}\right) \quad . \tag{12}$$

The output voltage from the regulator Vout is the sum of VR1 + VR2. But VR1 is equal to Vreg

$$Vout = R2\left(IQ + \frac{Vreg}{R1}\right) + Vreg \quad . \tag{13}$$

or

$$Vout = R2 \cdot IQ + Vreg\left(\frac{R2}{R1} + 1\right) \quad . \tag{14}$$

If the current IR1 >> IQ then the quiescent current IQ can be ignored in Equation (14) and Vout is given by

$$\text{Vout} = \text{Vreg}\left(\frac{\text{R2}}{\text{R1}} + 1\right) . \qquad (15)$$

Since for the 78XX regulators, IQ is about 6 milliamps. IR1 should be about at least 30 milliamps. The goal is not to make IR1 too large, as this will reduce the efficiency of the regulator circuit.

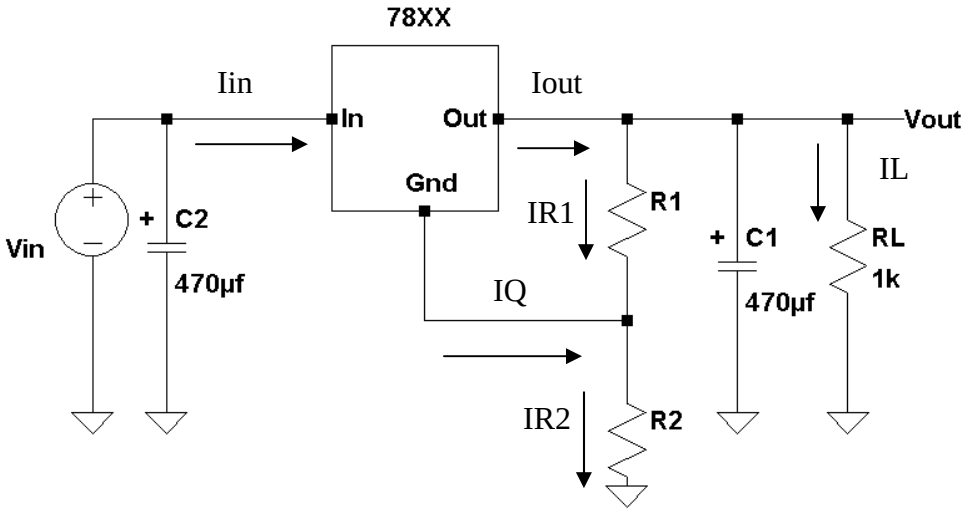


Figure 5: A circuit diagram to make linear voltage regulator adjustable.

Procedure:

General Setup:

1. Record the model and serial number of the scope, power supply, multimeter and function generator used in laboratory experiment.
2. Download the datasheet for the 78XX regulators. This will be needed to obtain the pin-out of the regulator. When comparing datasheet data values to experimental data use the typical values in the datasheet if given.
3. Obtain the pin-out for the 2N2222 transistor
4. Make sure that the power supply to the op-amp is correctly wired so as not to apply the incorrect polarity to the op-amp.
5. When measuring any values, make sure to measure all inputs as well as the output of the circuit. Do not rely on the values indicated on the instruments. Always measure all signal values.
6. Before turning any power on, double check the wiring to make sure that it is correct.
7. Measure all resistors that are used in the amplifier circuits using the multimeter and record these values.
8. Use all measured values to determine experimental results such as gain and current.
9. Comparing data means to calculate the percent difference between two values. For example, theoretical values versus measured values.
10. Comparing data graphically means to plot the data on the same plot to see how the data overlaps.

Discrete linear regulator:

1. Build the linear regulator of Figure 2.
2. Calculate the resistors R1 and R2 required to produce an output voltage of 3 volts for the circuit of Part 1. The minimum values for R1 and R2 should be 1000 ohms.
3. Set +Vcc = 15 volts and -Vcc to -15 volts.
4. Build this linear circuit (Part 1) using a 1000 ohm resistor for RL. Take note of the polarity of the two electrolytic capacitors. Double check your wiring.
5. Vary the input voltage Vin, between 0 and 6 volts and measure Vout, Iout and Iin.
6. Plot the output voltage Vout as a function of Vin.
7. What is the dropout voltage for this regulator?
8. Plot the output current Iout as a function of Vin.
9. Plot the input current Iin as a function of Vin.
10. Calculate Pin and Pout from steps 6, 7, 8 and 9.
11. For step 5, plot the output efficiency Pout / Pin as a function of Vin once the output voltage becomes constant.
12. Keeping Vin at 6 volts and varying the RL between 100 and 10000 ohms and measure Vout, Iout, and Iin as a function of Vin. Use 5 different load resistor values.
13. Calculate the load regulation.
14. For step 12, plot the output efficiency Pout / Pin as a function of RL.

78XX Three terminal linear regulator

1. Build this linear regulator circuit of Figure 3 using the 7805 regulator and a 1000 ohm resistor for RL. Take note of the polarity of the two electrolytic capacitors. Double check your wiring.
2. Vary the input voltage between 0 and 20 volts and measure Vout, Iout and Iin.
3. Plot Vout as a function of Vin.
4. What is the dropout voltage for this regulator and compare this measured value to the value given in the datasheet.
5. Plot Iout and Iin as a function of Vin in Step 2.
6. Compute Pin and Pout as a function Vin.
7. From step 6, plot the output efficiency Pout / Pin as a function of Vin once the output voltage becomes constant.
8. Keeping Vin at 15 volts and varying the RL between 100 and 10000 ohms, measure Vout, Iout and Iin as a function of RL. Use 5 different load resistor values.
9. Compute Pin and Pout as a function RL
10. For step 9, plot the output efficiency Pout / Pin as a function of RL.
11. Repeat steps 1 – 7 for the 7812 voltage regulator.

78XX A three terminal linear regulator as an adjustable regulator

1. Calculate the resistors R1 and R2 required to produce an output voltage of 7 volts for the linear regulator circuit of Figure 5. The minimum values for R1 and R2 should be 1000 ohms.

2. Build the linear regulator circuit of Figure 5 using a 7805 regulator and a 1000 ohm resistor for RL. Take note of the polarity of the two electrolytic capacitors. Double check your wiring.
3. Vary the input voltage between 0 volts and 15 volts and measure Vout, Iout and Iin.
4. Plot Vout as a function of Vin.
5. Determine the dropout voltage for this regulator and compare this measured value to the value given in the datasheet.
6. Plot Iout and Iin as a function of Vin in Step 3.
7. Compute Pin and Pout as a function Vin.
8. From step 7, plot the output efficiency Pout / Pin as a function of Vin once the output voltage becomes constant.

Report: Please follow the procedures in this laboratory manual for writing the report for this experiment. Include in your report:

1. The equipment used model and serial number.
2. Laboratory partners
3. Date and time data were taken.
4. The goal of the laboratory experiment.
5. The procedures.
6. The pre-laboratory results.
7. All calculations for each step.
8. All plots generated for each step.
9. All comparisons calculations.
10. For each data collection step in the procedure, there should be either data collected, a calculation performed or a waveform recorded. Please include these in the report.
11. Short summary discussing what is observed for each of the steps given in the laboratory experiment.
12. Also include what you learned.
13. Make sure to include the measured dropout voltages as well as the dropout voltages from the datasheet.
14. Discuss the efficiency of this linear regulator and why is efficiency an important parameter.
15. Where does the regulator power go to?
16. Is the curve linear for IL versus Vin?

EXPERIMENT #4

Switching Voltage Regulators

Goals:
To introduce the concepts of using a switching regulator as a voltage regulator. The theory of a switching regulator will be presented along with its a design. Data collected during this laboratory experiment will be compared to the datasheet for the switching regulator used.

References:

Microelectronics-Circuit Analysis and Design, D. A. Neamen, McGraw-Hill, 4th Edition, 2007, ISBN: 978-0-07-252362-1.

The following two links are to the Tektronix website for the user manual for the TDS2014B oscilloscope and for the AFG3022B Function generator:
Oscilloscope:
http://www2.tek.com/cmswpt/madetails.lotr?ct=MA&cs=mur&ci=16272&lc=EN

Equipment:

Oscilloscope: DPO 4034B
Triple Power supply
Capacitors available in the laboratory
Resistors available in the laboratory
Multimeter
Inductor (100 μH)
Electrolytic Capacitors (470 μF at 15 volts)
LM 2576-ADJ switching regulator
Fast recovery diode MBR 1060

Pre-laboratory:

Read this laboratory experiment carefully to become familiar with the background and the procedural steps in this experiment. Carefully read each section and become familiar with the equations for each circuit.

Using the simulation package of your choice in which you are the most familiar with: Multisim, Workbench or LTSpice IV simulate the linear regulator of Figure 2.

a. Download the National Semiconductor LM 2576-ADJ Datasheet and become familiar with this part.
b. Design a 5 volt DC output switching regulator with 10 volts DC of input.

c. Pick the ratio for R1 and R2 that sets the output to 5 volts DC (Figure 2 of datasheet). The minimum values for R1 and R2 should be 1000 ohms.
d. Compute E*T given on page 14 of datasheet.
e. Assuming a maximum current of 1 to 1.5 amps find the optimum inductance L given in Figure 7 of datasheet.
f. Compute the minimum output capacitance (page 14 of datasheet).
g. Assuming a 3 amp maximum load, calculate the efficiency of the switching regulator (Performance Figures).
h. Assuming a maximum load current of 3 amps, find the power dissipation of the output and the regulator.
i. What is the expected dropout voltage at 3 amps (Vin - Vout)?
j. What is the expected current limit for the LM2576 regulator?
k. Approximately how much does the output voltage change if the input voltage goes from 10 volts to 15 volts (assume a junction temperature of 25 Degrees C)?

Discussion:

Switching regulators are based upon using a pulse where its duty cycle is varied to maintain a constant voltage at its output. Consider the periodic pulse waveform given in Figure 1. The average or DC for time varying signal is by

$$Vavg = \frac{1}{T}\int_0^T v(t)\,dt \quad . \tag{1}$$

But for the periodic pulse signal v(t) is equal to zero for the time period of T - T1 and takes on a value of A from 0 to T. Substituting these values is Equation (1) gives

$$Vavg = \frac{1}{T}\int_0^{T1} A\,dt \quad . \tag{2}$$

Integration Equation yields an average voltage or DC voltage (Vavg) of

$$Vavg = A\,\frac{T1}{T} \tag{3}$$

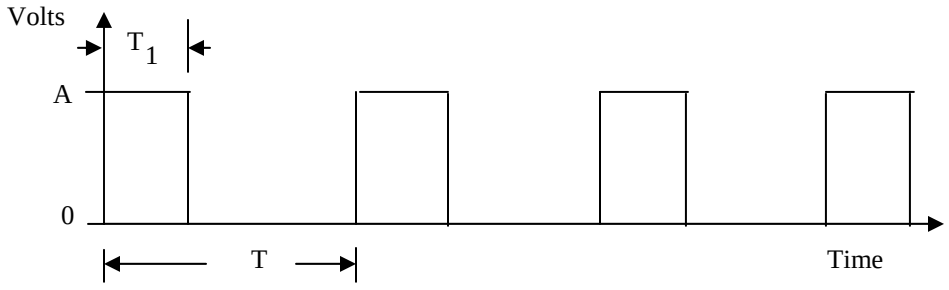


Figure 1: An example of a periodic pulse waveform.

The average voltage Vavg depends on the ratio of T1 to T. As T1 decreases, Vavg decreases, and as T1 increases, Vavg increases. The ratio of T1 to T is nothing more than the *duty-cycle*, D, of the periodic waveform

$$Vavg = A \cdot D \quad . \tag{4}$$

A circuit that produces a varying duty cycle periodic waveform is called a *pulse width modulator*. Consider the block diagram shown in Figure 2. This circuit uses a comparator and a sawtooth waveform to generate a varying duty cycle periodic waveform. The output of the comparator is A volts if V1 > V2 otherwise the output of the comparator is 0 volts. For a fixed input Vin, if Vin > V2, then the output of the comparator is A volts. As the input V2 increases in value due to the sawtooth waveform increasing in value, there is a point in time when V2 becomes greater than Vin and the output of the comparator goes to zero. Figure 1 gives the output of the pulse width modulator with T1 equal to Vin and T equal to K.

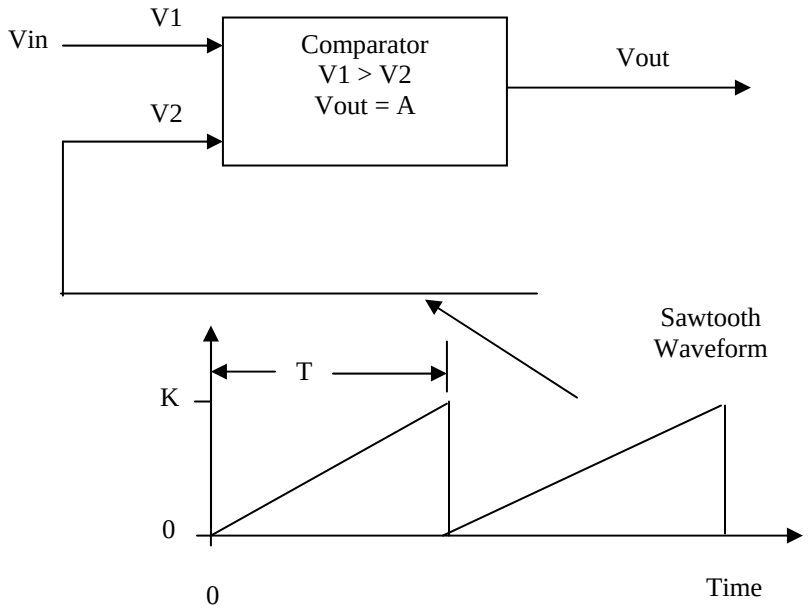


Figure 2: A block diagram of a pulse width modulator.

The average voltage output from Figure 2 is then given by Equation (3) as

$$Vavg = A \frac{Vin}{K} \quad , \tag{5}$$

where T = K (the amplitude of the sawtooth wave at time T) and T1 = Vin (the time when the sawtooth amplitude is equal to Vin). The pulse width modulator

provides a means of varying the pulse width of a periodic pulse waveform, which allows the average voltage to be varied.

Figure 3 gives a simple switching voltage regulator using an N-channel MOSFET and a pulse width modulator. The input to the pulse width modulator is a sampled version of Vout generated by the voltage divider composed of R1 and R2. The capacitor C is used to filter the sampled output voltage to obtain its average or DC value. As the output voltage increases, the pulse width modulator decreases its pulse width and decreases the time that the MOSFET is on. This decreases the time that Vin is connected to the output. As Vin decreases, the pulse width modulator increases its pulse width. This increases the time that Vin is connected to Vout.

The output waveform is the periodic pulse given in Figure 1 with A equal to Vin. Typical switching regulators use periodic frequencies in the range of a few kilohertz to a few megahertz (1 / T).

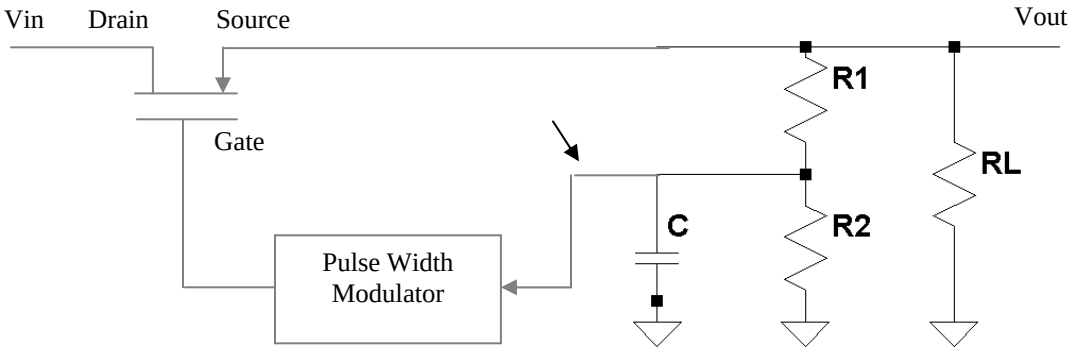


Figure 3: A simple switching regulator.

The main limitation of the simple regulator given in Figure 1 is that Vout is a periodic pulse, not a constant DC voltage. The problem is that, when the MOSFET turns off, Vout goes to zero and the current to the load, RL, goes to zero. What needs to be added to this simple switching regulator is a means of storing energy when the MOSFET is on and delivering this energy to the load, RL, when the MOSFET is off. One device that stores energy in a magnetic field is an inductor.

Figure 4 shows the modification of the simple switching regulator with the addition of an inductor and a diode. This allows current to continue to follow in RL when the MOSFET is OFF. When the MOSFET is on, Vin appears at the source pin, the diode is reversed biased and off, and VL appears on the left side of the inductor L1. Ignoring the current flowing in R1 and R2 since this current is usually much smaller than current flowing in RL, the effective circuit, when the MOSFET is on, is an RL circuit as shown in Figure 5. Since the current in an

inductor can not change instantaneously, the current through the inductor starts to increase at rate of

$$IL = \frac{Vin}{RL}\left(1 - e^{-\frac{t\,L}{R}}\right) \qquad (6)$$

and reaching a final value IL = Vin / RL. At the point that MOSFET turns off, the diode becomes forward biased allowing current to continue to flow in the inductor in the same direction as when the MOSFET was on. The model of the switching regulator when the MOSFET is off is shown in Figure 6. The diode turns on allowing current to flow through the inductor L1 and through the load RL.

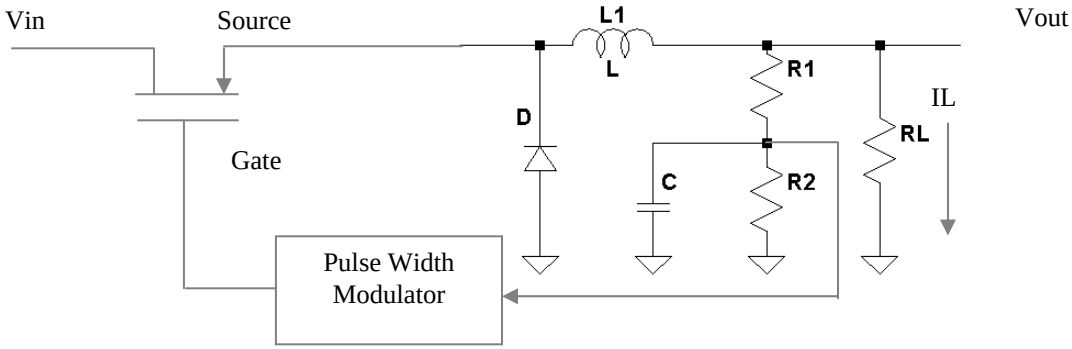


Figure 4: A switching regulator with energy storage.

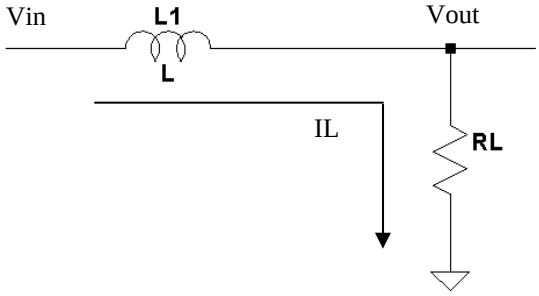


Figure 5: The model of the switching regulator when the MOSFET is on.

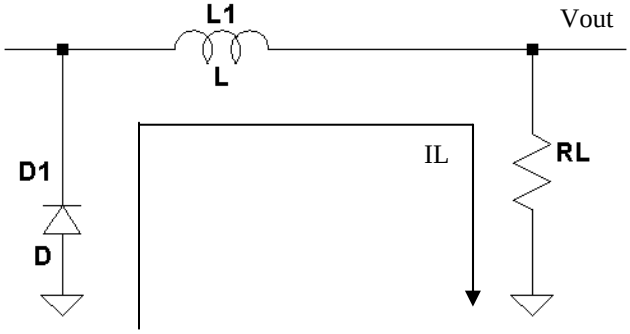


Figure 6: The model of the switching regulator when the MOSFET is off.

Since there is no longer an applied source the current through the inductor L and the load RL decreases at the rate of

$$IL = K \cdot e^{-\frac{t\,L}{R}} \tag{7}$$

where K is the current flowing in the inductor and the load RL when the MSOFET turns off. Figure 7 shows the current flowing in the load RL and the inductor L1 as a function of time.

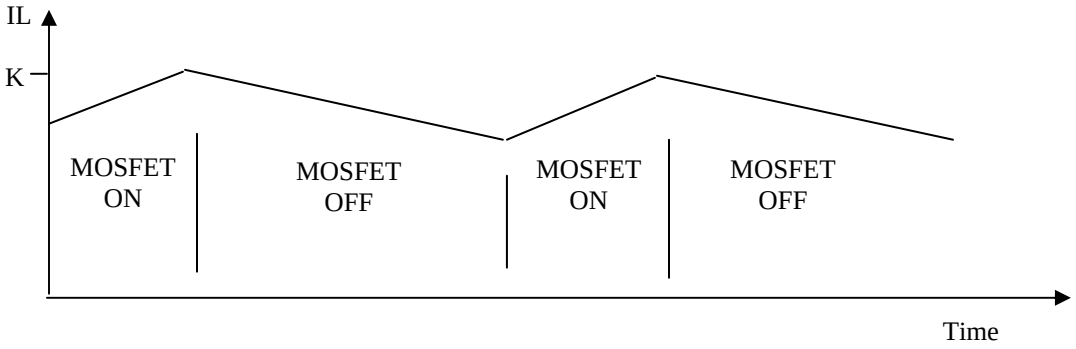


Figure 7: A plot of load current as a function of time.

Since the voltage across a resistor is equal to its current times its resistance, Vout = IL · RL. Vout is simply the same waveform that is given in Figure 7, but scaled by RL. The magnetic energy stored in the inductor when the MOSFET is on is delivered to the load when the MOSFET is off essentially providing for continuous current flow when the MOSFET is on and off. To maintain a constant Vout, an additional energy storage element, a capacitor, is placed across the load RL. The final switching regulator is given in Figure 8.

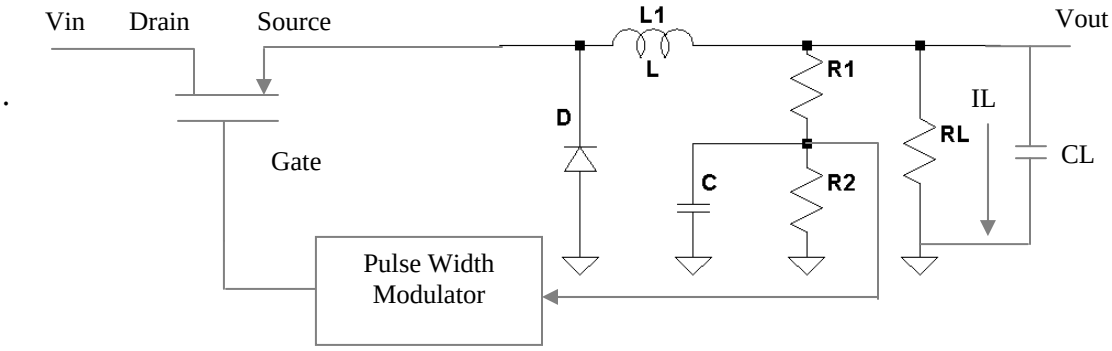


Figure 8: The final switching regulator circuit diagram.

When designing this regulator, several parameters must be adhered to. First, the maximum currents for the MOSFET, the inductor and the diode must be observed. The polarity and maximum voltage of the capacitors that are used must

be followed. And finally the maximum power dissipation allowed for the MOSFET and its maximum temperature rating must be included in the design.

The switching regulator presented here, as shown in Figure 8, is available from many semiconductor manufacturers in a single integrated circuit (IC). Typically the IC includes the MOSFET as well as the pulse width modulator. The external parts that must be included are the inductor, diode, and the capacitor. R1 and R2 are usually also included in the IC. The switching regulator presented in Figure 8 is known as a *BUCK regulator,* since Vout < Vin. There are other switching regulator topologies that allow for generating an output voltage that is greater than the input voltage. These switching regulators are known as *BOOST regulators*. Another common topology is the single-ended primary-inductor converter (SEPIC) switching regulator. This regulator uses two inductors and allows for both Vout < Vin and Vout > Vin conditions to be achieved in one design topology.

The main advantage that a switching regulator has over a linear regulator is power efficiency. From the linear regulator laboratory experiment, the power dissipation across a linear regulator is

$$Preg = Iin * Vreg \tag{8}$$

But

$$Iin = IL + IQ \quad , \tag{9}$$

where IQ is the quiescent current of the regulator. This is the current needed by the regulator to power its internal electronics. Under most conditions, IQ << IL and

$$Iin \approx IL \tag{10}$$

The power dissipated in the regulator is

$$Preg = Iin \cdot Vreg \tag{11}$$

and the total input power

$$Pin = Vin \cdot Iin = Vin \cdot IL \tag{12}$$

Pout is simply

$$Pout = Vout \cdot IL \tag{13}$$

The efficiency is defined as

$$\text{Efficiency} = \text{Pout} \ / \ \text{Pin} \cdot 100\% \quad (14)$$

Substituting Equations (12) and (13) in Equation (14) gives

$$\text{Efficiency} = \text{Vout} \ / \ \text{Vin} \cdot 100\% \quad (15)$$

Just having Vin > Vout, The efficiency of the linear regulator circuit is less than 100%. Typical efficiencies for linear regulator are bellow 50%. For switching regulators, the main loss of power is the power dissipated in the MOSFET. But the MOSFET is either full on or full off. When the MOSFET is off there is no power dissipated in the MOSFET, but when the MOSFET is on the power dissipated in the MOSFET is

$$P_{MOSFET} = IL^2 \cdot Rds \quad , \quad (16)$$

where Rds is the drain to source on resistance of the MOSFET. For a power MOSFET Rds on is on the order of a few milliohms. Such a small value produces very small power dissipation in the MOSFET allowing for very high efficiencies for the switching regulator. Efficiencies of 80% to 90% are very common in switching regulators. To reiterate, the frequency of switching regulators runs anywhere from a few kilohertz to a few megahertz. This allows for reasonably-sized inductors and capacitors to be used.

Procedure:

General Setup:

1. Record the model and serial number of the scope, power supply, multimeter and function generator used in laboratory experiment.
2. Download the datasheet LM 2576-ADJ switching regulator. This will be needed to obtain the pin-out of the regulator. When comparing datasheet data values to experimental data use the typical values in the datasheet if given.
3. When measuring any values make sure to measure all inputs as well as the output of the circuit. Do not rely on the values indicated on the instruments. Always measure all signal values.
4. Before turning any power on double check the wiring to make sure that it is correct.
5. Measure all resistors that are used in the amplifier circuits using the multimeter and record these values.
6. Use all measured values to determine experimental results such as gain and current.
7. Comparing data means to calculate the percent difference between two values. For example, theoretical values versus measured values.
8. Comparing data graphically means to plot the data on the same plot to see how the data overlaps.

Switching Regulator:

1. Have the lab assistant approve your design using a 100 μH inductor and two

470μF, 15 volts capacitors.

2. Build your design making sure to correctly wire the LM2576, the polarity of the diode, and the electrolytic capacitors.
3. Triple check your wiring before applying any power.
4. Select RL to be 500 ohms.
5. Vary the input voltage Vin between 0 and 15 volts and measure Vout, Iout and Iin.
6. Plot the output voltage Vout as a function of Vin.
7. What is the dropout voltage for this regulator?
8. Compare the dropout value in step 7 to the expected value from the datasheet.
9. Plot the output current Iout as a function of Vin.
10. Plot the input current Iin as a function of Vin.
11. Calculate Pin and Pout from steps 6, 9, and 10.
12. For step 11, plot the output efficiency Pout / Pin as a function of Vin once the output voltage becomes constant. How does this value compare to the expected value.
13. Setting Vin to 10 volts and varying the RL between 100 and 10000 ohms measure Vout, Iout, and Iin as a function of RL. Use at least 5 different resistor values. Do not forget to measure the actual resistance of these resistors.
14. Plot Vout as a function of RL.
15. Plot the output current Iout as a function of RL.
16. Plot the input current Iin as a function of RL.
17. Calculate Pin and Pout from steps 14, 15, and 16.
18. For step 17, plot the output efficiency Pout / Pin as a function of RL.
19. For step 14 calculate the load regulation.
20. Measure with a scope the voltage on both sides of the inductor for Vin = 10v and RL = 500 ohms. Discuss your findings in the lab report.

Report: Please follow the procedures in this laboratory manual for writing the report for this experiment. Include in your report:

1. The equipment used model and serial number.
2. Laboratory partners
3. Date and time data were taken.
4. Your laboratory report should include the goal of the laboratory experiment.
5. The procedures.
6. The pre-laboratory results.
7. All calculations for each step.
8. All plots generated for each step.
9. All comparisons calculations.
10. For each data collection step in the procedure, there should be either data collected, a calculation performed, a waveform recorded. Please include these in the report.
11. Short summary discussing what is observed for each of the steps given in the laboratory experiment.
12. Also include what you learned.

13. Make sure to include the measured dropout voltage as well as the dropout voltage from the datasheet.
14. Discuss the efficiency of this switching regulator and why is efficiency an important parameter.
15. Is the curve linear for IL versus Vin?
16. Where does the power dissipated in the regulator go?

EXPERIMENT #5

Precision Diodes and Applications

Goals:
To introduce the concepts of using diodes as rectifiers and limiters. The concepts of the ideal diode designed from diodes and op-amps circuits will also be discussed. Finally, diode limiter circuits will be presented. Data collected during this laboratory experiment will be compared to the theoretical Equations presented in this laboratory experiment.

References:

Microelectronics-Circuit Analysis and Design, D. A. Neamen, McGraw-Hill, 4th Edition, 2007, ISBN: 978-0-07-252362-1.

The following link is to the Tektronix website for the user manual for the DPO 4034B oscilloscope and for the AFG3022B Function generator:
Oscilloscope:
http://www2.tek.com/cmswpt/madetails.lotr?ct=MA&cs=mur&ci=16272&lc=EN

Equipment:

Oscilloscope: DPO 4034B
Triple Power supply
Capacitors available in the laboratory
Resistors available in the laboratory
Multimeter
1N4148 diodes
Electrolytic Capacitors (470 uf at 15 volts)
LM 285 precision voltage reference.

Pre-laboratory:

Read this laboratory experiment carefully to become familiar with the background and the procedural steps in this experiment. Carefully read each section and become familiar with the equations for each circuit.

Use the simulation package of your choice in which you are the most familiar with: Mulitsim, Workbench or LTSpice IV.

a. Download the National Semiconductor LM285 Datasheet and become familiar with this part.
b. Simulate the half wave rectifier circuit given in Figure 3 with R = 1K and the diodes equal to 1N4148s. Set Vin equal to a 200 Hz +5 volt peak sine wave with no DC offset. Obtain a plot of Vin and Vout versus time.
c. Repeat Step b for Vin equal to a 200 Hz +10 volt peak sine wave with no DC offset.

d. Simulate the full wave rectifier circuit given in Figure 5 with R = 1K and the diodes equal to 1N4148s. Set Vin to a 200 Hz +5 volt peak sine wave with no DC offset. Obtain a plot of Vin and Vout versus time.
e. Repeat Step d for Vin equal to a 200 Hz +10 volt peak sine wave with no DC offset.
f. Repeat Step b for Figure 7a for R =1K and C = 470 μf. Obtain the peak-to-peak ripple voltage. How does this value compare to Equation (11)? What is the DC voltage at the output Vout? How does this value compare to Equation (13).
g. Repeat Step d for Figure 7b for R =1K and C = 470 μf. Obtain the peak-to-peak ripple voltage. How does this value compare to Equation (12)? What is the DC voltage at the output Vout? How does this value compare to Equation (14).
h. Simulate the ideal half wave rectifier given in Figure 9 for R = 1k. Set Vin to a 200 Hz +5 volt peak sine wave with no DC offset. Also set +Vcc = 15 volts and -Vcc = -15 volts. Use this same value for all steps unless otherwise directed. Obtain a plot of Vin and Vout versus time.
i. Change the diode orientation in Figure 9 and repeat Step h.
j. Change the input frequency of the sine wave to 2000 Hz, 20kHz and 200 kHz and repeat Step h.
k. Simulate the ideal half wave rectifier given in Figure 11 for R = 1k. Set Vin to a 200 Hz +5 volt peak sine wave with no DC offset. Obtain a plot of Vin and Vout versus time.
l. Change the diode orientations in Figure 11 and repeat Step k.
m. Simulate the ideal full wave rectifier given in Figure 13 for R1 and R2 = 1k. Set Vin to a 200 Hz +5 volt peak sine wave with no DC offset. Obtain a plot of Vin, V2 and Vout versus time.
n. Change the diode orientations in Figure 13 and repeat Step m.
o. Simulate the limiter circuit given in Figure 17a for RF = RA = 100k, R1 = 20k, R2 = 15k, R3 = 10K, and R4 = 20K. Set VR1 = +Vcc and VR2= -Vcc . Vary Vin from -Vcc to +Vcc and obtain Vout. Compare this result to the plot given in Figure 16. Use at least 10 points to perform the comparison.
p. Repeat Step o with but remove RF.

Discussion:

Diode Model

The diode model used in the laboratory experiment is shown in Figures 1 and 2. When the diode is forward biased so that Vd > Vx, (the forward turn on voltage) the diode is on and the current Id flowing in the diode is non-zero (Figure 2b). When Vd < Vx, the diode current Id is zero and the diode is reversed biased (Figure 2c). Under this condition no current is flowing in the diode and the diode can be considered an open circuit. Figure 1 gives a plot of the diode current as a function of the diode voltage showing the forward biased and reverse biased region. Typical values of the forward biased voltage Vx depends on the semiconductor material used for the diode but typically is in the range of 0.2 volts to 0.7 volts.

Half Wave Rectifier

Diodes can be used to convert an average voltage AC signal to a DC voltage using the process of rectification. Figure 3(a) shows a diode connected to a resistor R with a Vin of

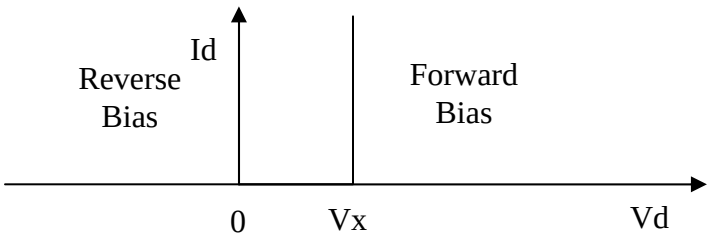


Figure 1: Id versus Vd for the simplified diode model.

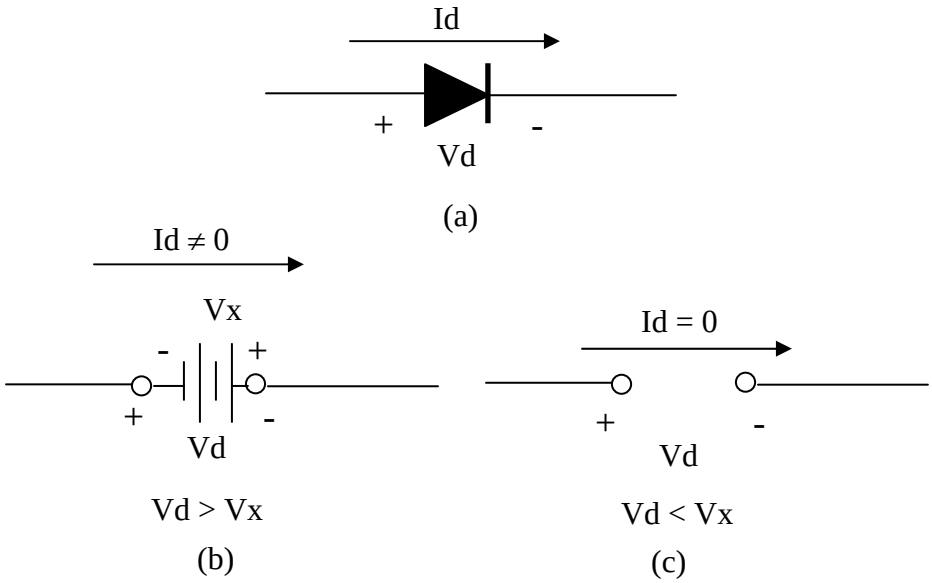


Figure 2: The simplified model for the diode. (a) Its symbol, (b) the forward biased model, and (c) the reversed biased model.

$$Vin(t) = A \cdot \sin(\omega t) \quad , \qquad (1)$$

where ω is the frequency in rad/sec and $\omega = 2\pi f$ (f is the frequency in hertz). This circuit is commonly called a half wave rectifier.

When Vin < Vx the diode is off (reversed bias) and the diode model of Figure 2(c) applies, the diode current Id = 0 and Vout = 0 (Vout = R · Id). Under the condition Vin > Vx, the diode is on (forward bias) and the model of Figure 2(b) applies and current Id flows through the diode and the resistor R. Vout is then given by

$$Vout = Vin - Vx \quad . \tag{2}$$

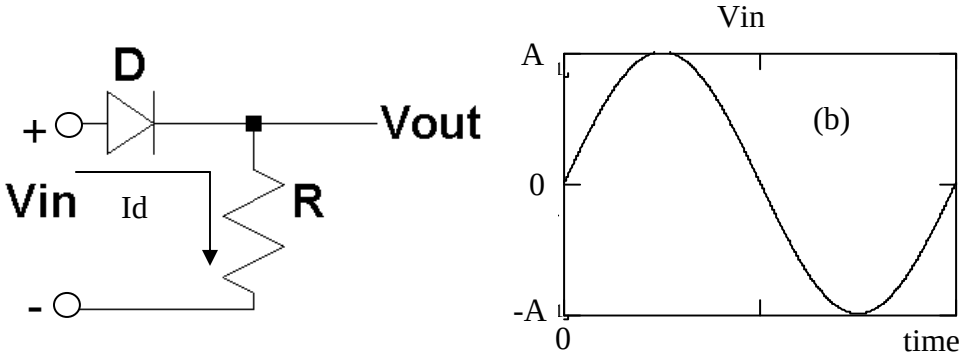


Figure 3: (a) Half wave rectifier circuit diagram and (b) Vin as a function of time.

The output is the same as the input Vin but smaller in voltage by Vx (Assuming Vin peak >> Vx). Figure 4 gives Vout as a function time.

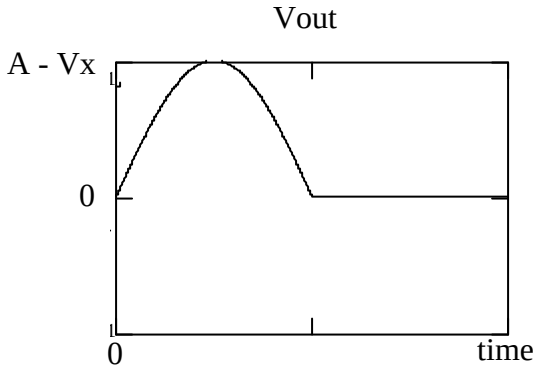


Figure 4: Vout as a function of time for the half wave rectifier circuit.

As shown in Figure 4, half of the sine wave waveform has been set to zero. The average or DC value for Vout is now non-zero. The average is defined

$$Vavg = \frac{1}{T}\int_0^T v(t)\,dt \quad . \tag{3}$$

Substituting $Vin(t) = A \cdot \sin(\omega t)$ for v(t)

$$Vavg = \frac{1}{T}\int_0^T A \cdot \sin(\omega t)\,dt \quad . \tag{4}$$

and integrating over its period T = 1 / f produces a zero average value. Repeating the process for Vout gives

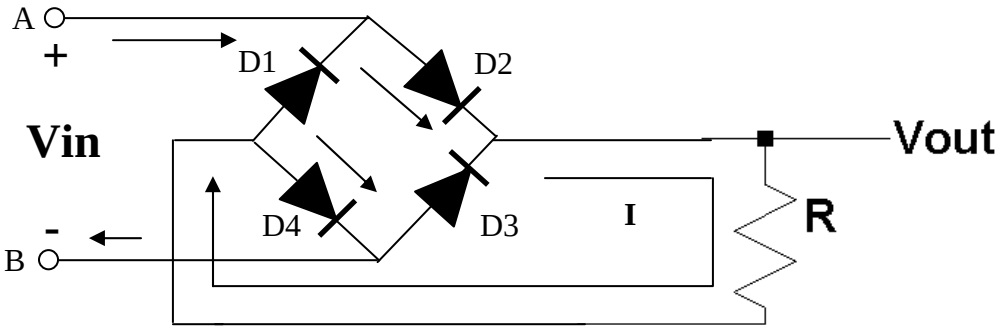
$$Vavg = \frac{1}{T}\int_{0}^{\frac{T}{2}} (A - Vx) \cdot \sin(\omega t)\, dt \quad . \tag{5}$$

The integration is now over half the period since Vout is zero for half the period. Performing the integration in given in Equation (5) yields

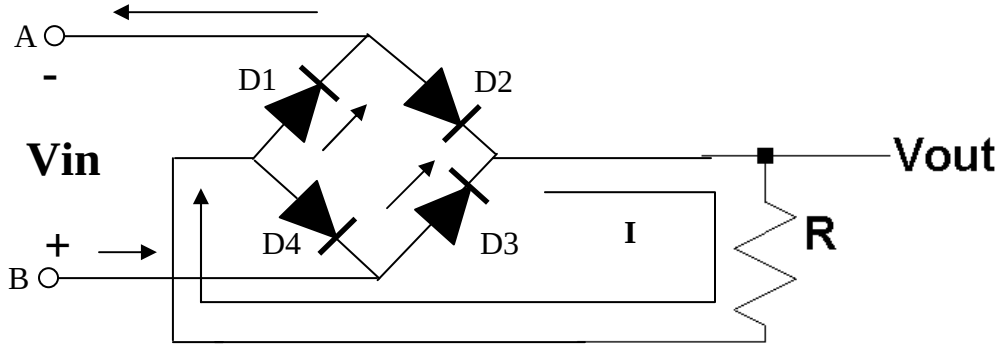
$$Vavg = \frac{A - Vx}{\pi} \quad . \tag{6}$$

Full Wave Rectifier

The main limitation of the half wave rectifier is that its output is zero for half of the period. Figures 5(a) and (b) give circuit diagram of a full wave rectifier using a bridge configuration. A full wave rectifier allows current to flow during both parts of the input sine wave input.



(a)



(b)

Figure 5: A full wave rectifier circuit diagram (a) For Vin > 2 · Vx and (b) Vin < - 2 · Vx..

Assuming Vx is the same for all of the diodes, when Vin > 2 · Vx, D2 and D4 are forward biased and D1 and D3 are reverse biased. Current then flows from Vin (A) through D2 through R and then through D4 and back to Vin (B) (Figure 5(a)). Again, when Vin < -2 · Vx, but in the opposite polarity, D1 and D3 are forward biased and D2 and D4 are reverse biased. Under this condition, current flows from Vin (B) through D3 and then through R and D1 and back to Vin (A) (Figure 5(b)).

Under both conditions for Vin > 2 · Vx and Vin < - 2 · Vx, the current flowing through the resistor R is in the same direction. Even though Vin changes polarity, the voltage across R (Vout = I · R) remained the same. Figure 6 gives Vin and Vout as a function of time. Vout is the same as Vin when Vin > 2 · Vx except it has been reduced in amplitude by 2 two diode drops of Vx (Vout = Vin - 2 · Vx and assuming Vin peak >> 2 ·Vx). When Vin < -2 · Vx, then Vout is the inverted version of Vin Vx except it also has been reduced in amplitude by two diode drops of Vx (Vout = 2 · Vx - Vin). In other words

$$\text{Vout} = | \text{Vin} - 2 \cdot \text{Vx}) | \quad , \tag{7}$$

where | | is the absolute value.

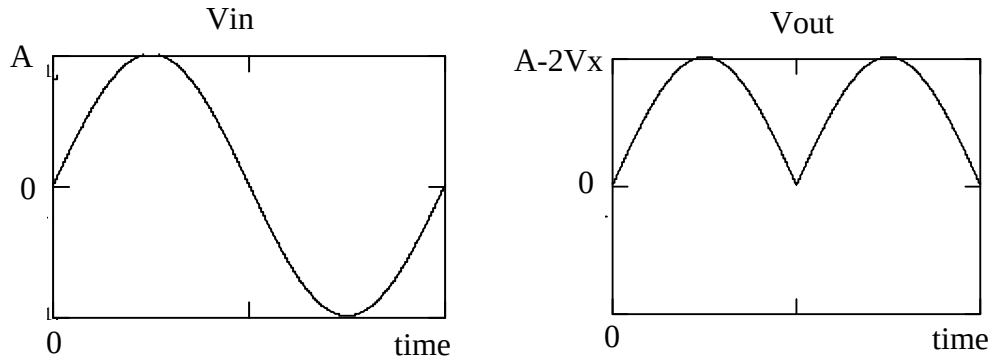


Figure 6: Vin and Vout as a function of time for a full wave rectifier.

The average or DC value for Vout is also non-zero. For the full wave rectifier, the average is given by

$$\text{Vavg} = \frac{1}{T} \int_0^T | \left(\text{A} - 2 \cdot \text{Vx}\right) \cdot \sin(\omega t) | \, dt \quad . \tag{8}$$

Since Vout is the same for $0 \le t < T/2$ and $T/2 \le t < T$, the integral is twice the integral over $0 \le t < T/2$

$$Vavg = \frac{2}{T} \int_0^{T/2} \left| \left(A - 2 \cdot Vx\right) \cdot \sin(\omega t) \right| dt \qquad (9)$$

Performing the integration gives

$$Vavg = \frac{2 \cdot (A - 2 \cdot Vx)}{\pi} \qquad (10)$$

The average or DC value is twice the average value of the half wave rectifier given in Equation (6).

Rectifier Filtering

In many applications, it is desired to convert the output of rectification (either half or full wave) to a constant DC output. This can be accomplished by adding a capacitor C in parallel with the resistor R in Figures 3(a) and 5 as shown in Figure 7.

Figure 8 shows the output of the filtered half wave rectifier circuit. The curve highlighted in X is when the diode is delivering power to the load R and charging the capacitor C. Once the peak is reached, the capacitor is charged to its maximum value of A - Vx. As Vin decreases below its peak value of A the diode turns off. At this point the energy stored in the capacitor C is delivered to the resistor R and the capacitor starts to discharge as highlighted in the curve Y. The voltage difference between the peak value of A - Vx and the minimum voltage is known as the ripple voltage, Vr, and is given by

$$Vr = \frac{A - Vx}{f\,R\,C} \quad , \qquad (11)$$

where f is the frequency in Hertz of Vin as defined in Equation (1). For a full wave rectifier, the period is half that of a half wave rectifier or the frequency is twice that of a half wave rectifier

$$Vr = \frac{A - Vx}{2\,f\,R\,C} \quad , \qquad (12)$$

The average output voltage Vout for the half wave rectifier is the given as

$$Vout(average) = (A - Vx) \cdot \left(1 + \frac{1}{\pi}\sqrt{\frac{2\,Vr}{A - Vx}}\right) \qquad (13)$$

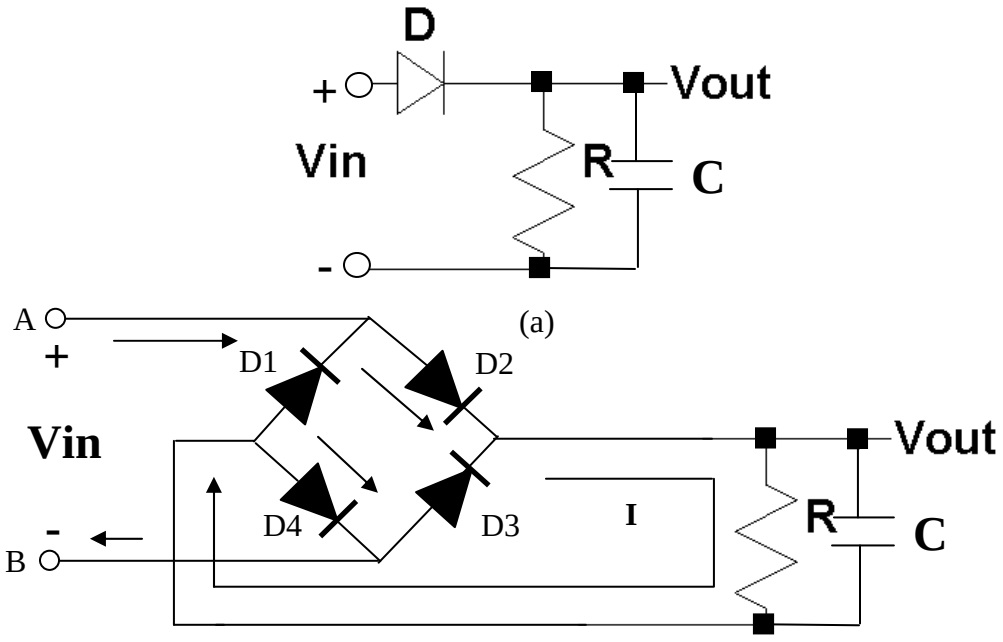


Figure 7: Filtering the output of a (a) half-wave and (b) full-wave rectifier circuit.

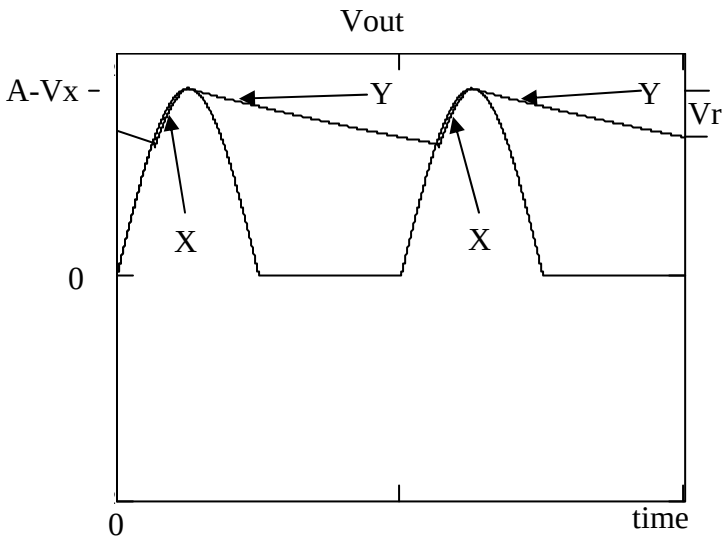


Figure 8: Filtered half wave rectifier output using a capacitor of Value C.

and for a full wave rectifier

$$\text{Vout(average)} = (A - 2 \cdot Vx) \cdot \left(1 + \frac{1}{\pi}\sqrt{\frac{2\,Vr}{A - 2 \cdot Vx}}\right) \qquad (14)$$

with Vr defined by Equations (11) and (12), respectively. For Vr << A - Vx or Vr << A - 2 · Vx, the average voltage output reduces to Vout(average) = A - Vx for the half wave rectifier and Vout(average) = A - 2 · Vx for the full wave rectifier.

The Ideal Half Wave Rectifier

The major limitation with the full wave and half wave rectifiers presented above is the forward biased voltage drop of the diodes that must be achieved before the diodes conduct. For the half wave rectifier Vin must exceed Vx and for the full wave rectifier must exceed 2 · Vx before the diodes start conducting. The ideal rectifier circuits use the open loop gain of the op-amp to remove the effects of the forward biased voltage diode Vx. Consider the ideal half wave rectifier shown in Figure 9. Assuming initially Vin = 0, and op-amp output is zero. Then since

$$\text{op-amp output} = Ad\,(V^+ - V^-) = Ad\,(Vin - V^-)\ , \qquad (15)$$

(where Ad is the open loop gain of the op-amp) V^- must also be initially zero. Since V^- and op-amp's output are both zero, the voltage across the diode Vd = op-amp output - V^- is zero and the diode is off. If Vin is now allowed to go negative (Vin < 0) then by Equation (15), the op-amp's output goes negative and the diode voltage Vd becomes negative and remains off. Since the diode is off and no current flows through the diode, the current flowing in the resistor I = 0. This results in zero voltage across the resistor and Vout = 0. Under this condition the feedback loop is open and the output of the op-amp is at maximum allowed negative voltage (negative rail). Next, consider Vin positive (Vin > 0). Under this condition, from Equation (15) the op-amp's output heads toward a positive voltage turning on the diode. The current flowing through the diode also flows through the resistor producing a non zero voltage at Vout. The op-amp will try to make $V^+ = V^-$ (virtual short) maintaining a closed loop configuration. Since V^+ = Vin and $V^+ = V^-$, V^- = Vout = Vin. The output Vout is nothing more than the input for Vin > 0. Equation 16 give the output Vout

$$\begin{array}{ll} Vout = Vin & \text{for } Vin > 0 \\ Vout = 0 & \text{for } Vin < 0 \end{array} \qquad (16)$$

If Vin is a sine wave as given by Equation (1), then Vout is the same as Figure 6 except the peak output voltage is equal to A not A - Vx. The forward bias diode voltage has been eliminated. To maintain a closed loop condition and to maintain that the diode is on, the op-amp's output = V^- + Vx or the op-amp's output = Vin + Vx.

Changing the diode direction changes the polarity of the output producing an output when Vin is negative

$$\begin{aligned} \text{Vout} &= 0 && \text{for Vin} > 0 \\ \text{Vout} &= \text{Vin} && \text{for Vin} < 0 \end{aligned} \qquad (17)$$

Figure 10 gives an inverting ideal half wave rectifier configuration. To maintain $V^- = V^+ = 0$, the diode must be forward-biased, and this occurs when the op-amp's output is greater than zero. For the op-amp's output to be greater than zero, Vin must be less than zero. If the feedback loop is closed since the diode is on, the Vout is

$$\text{Vout} = \frac{-\text{R2}}{\text{R1}}\text{Vin} \qquad \text{for Vin} < 0\ . \qquad (18)$$

Equation (18) is nothing more than the output equation for an inverting amplifier given an input Vin. For Vin > 0, the op-amp's output is negative (at its most negative value) and the diode is reversed biased and off. Since the diode is off (I2 = 0) and since no current flows into the V^- terminal of the op-amp, then the current I1 flowing in the resistor R1 is zero. Since I2 = 0 then

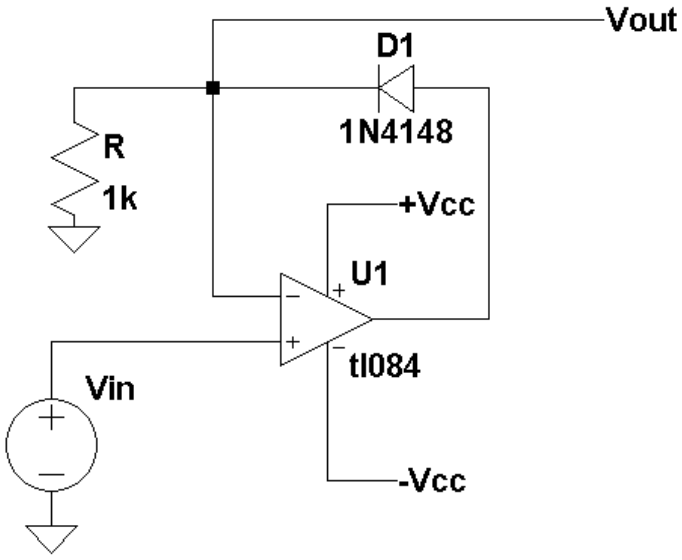


Figure 9: The ideal half wave rectifier.

$$\text{Vout} = 0 \qquad \text{for Vin} > 0 \qquad (19).$$

Equations (18) and (19) describe an inverting half wave rectifier output as described by Figure 6 without the effects of Vx. Changing the direction changes the polarity of Equation (18) and (19) and inverts the output polarity of the half wave rectifier of Figure 10.

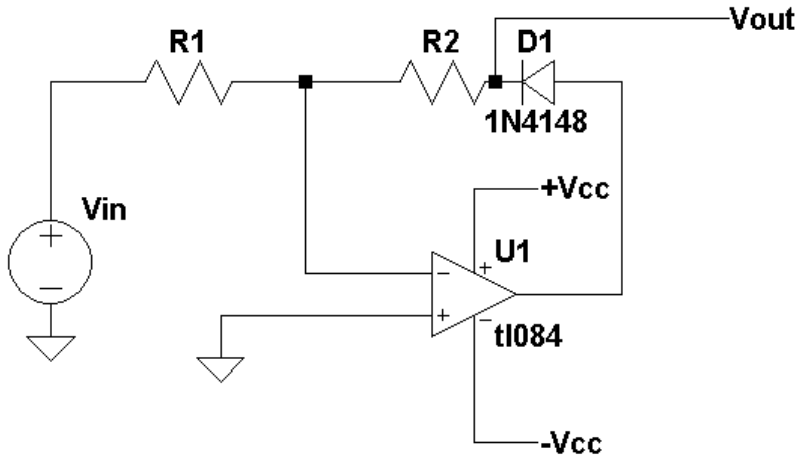


Figure 10: Inverting configuration ideal half wave rectifier.

.

The main limitation of the half wave rectifier circuits presented in Figures 9 and 10 is that for half the time period the output of the op-amp is in saturation either near the positive or negative rails. Care must be taken when an op-amp's output is at its rails and if the input common mode voltage is exceeded. When the op-amp is running open loop with no feedback ($V^+ \neq V^-$), Vout will not be zero when the diode D1 is off. In addition, for an op-amp to come out of saturation, it takes time and slows the response of the half wave rectifier circuits given in Figures 9 and 10. Adding a diode D2 as shown in Figure 11 prevents the op-amp from going into saturation and increases the overall response time of the half wave rectifier. For Vin <0, the op-amp output is positive and D1 is forward biased on and D2 is reversed biased off. Under this condition the output Vout is the same as described by Equation (18). But when Vin > 0 the op-amp's output is negative, D1 is off and D2 is forward biased on. D2 forward biased on keeps the feedback loop closed so that $V^- = V^+ = 0$. The current flowing in diode D2 is equal to the current flowing in R1 (Vin/R1). With diode D2 forward biased on and V- equal to zero, the op-amp's output is equal to -Vx and the op-amp output is kept from going to its most negative value (negative saturation). What makes the circuit of Figure 11 faster than the circuit of Figure 10 is that turning off the diodes is usually faster than an op-amp coming out of saturation.

The Ideal Full Wave Rectifier

Consider a sine wave input Vin as described in Equation (1) as input to the half wave rectifier given in Figure 11 with diodes the direction of diodes D1 and D2 swapped. This produces a negative going half wave rectifier output V2 as shown in Figures 12(a) and (b). Next, consider

$$V3 = Vin + 2 \cdot V2 \qquad (20)$$

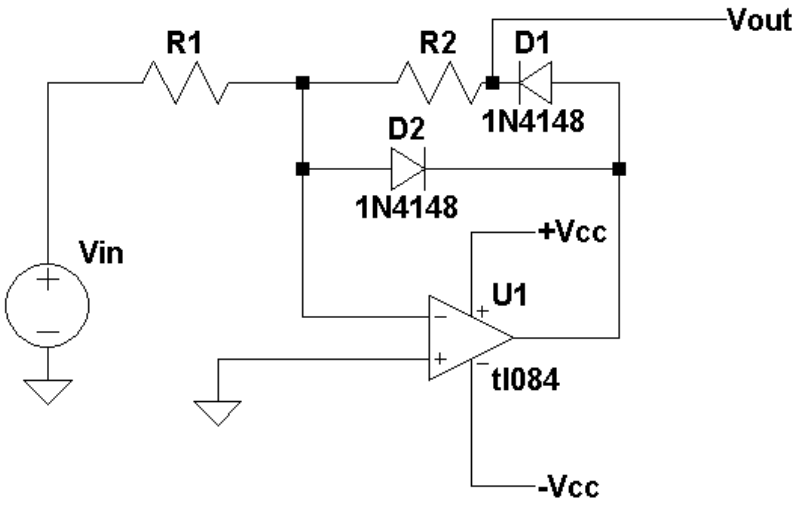


Figure 11: Half wave rectifier without op-amp saturation.

The best way to analyze Equation (20) is to determine V3 when Vin > 0 and when Vin is < 0. When Vin < 0, the output V2 of the inverted have wave rectifier output (Figure 12(b) is zero and Equation (20) reduces to

$$V3 = Vin + 2 \cdot 0 = Vin \text{ for } Vin < 0 \qquad (21)$$

For Vin > 0, V2 is simply equal to the inverted version of Vin (V2 = -Vin) and Equation (20) reduces to

$$V3 = Vin + 2 \cdot (-Vin) = -Vin \text{ for } Vin > 0 \quad . \qquad (22)$$

Equations (21) and (22) can be combined and be written as

$$V3 = -|\, Vin \,| \qquad (23)$$

Equation (23) is nothing more the inverted version of the full wave rectifier equation in Equation (7) for the ideal rectifier case of Vx = 0 (Figure 12(c)). Inverting Equation (23) gives

$$Vout = |\, Vin \,| \qquad (24)$$

and is shown in Figure 12(d). Inverting Equation (20) gives Vout directly as

$$V3 = -Vin - 2 \cdot V2 \qquad (25)$$

A closer look at Equation (25) shows that this equation is nothing more than a summing amplifier with gains of -1 and -2, respectively. Figure 13 shows the circuit diagram for a full wave rectifier using the ideal half wave rectifier and a two-input summing amplifier with gains of -1 and 2, respectively.

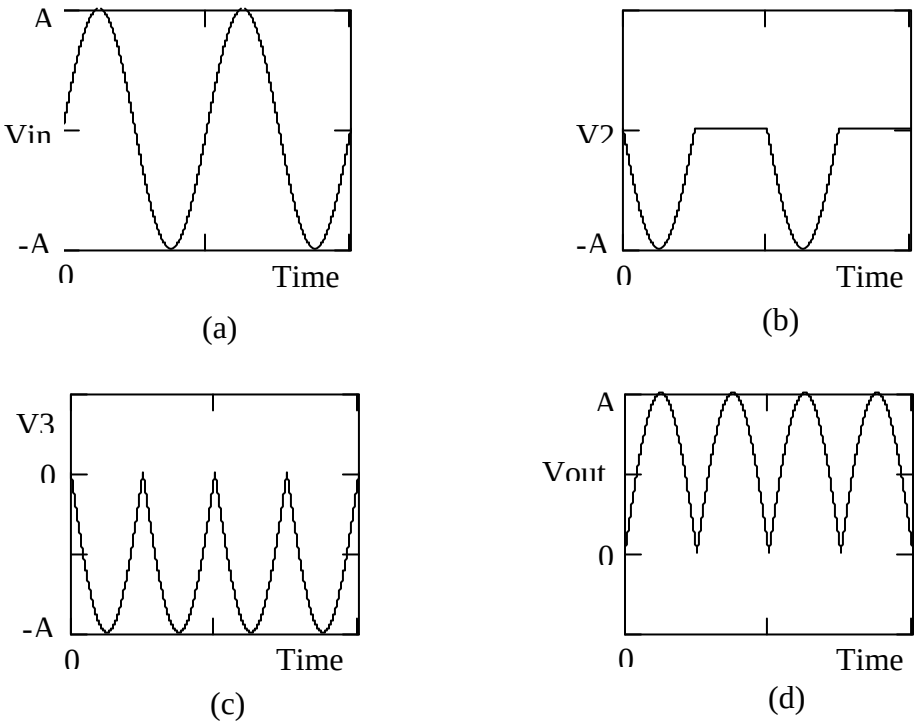


Figure 12: (a) The input signal, (b) the inverted half wave rectified signal, (c) the signal due to Equation (20), and the final output Vout.

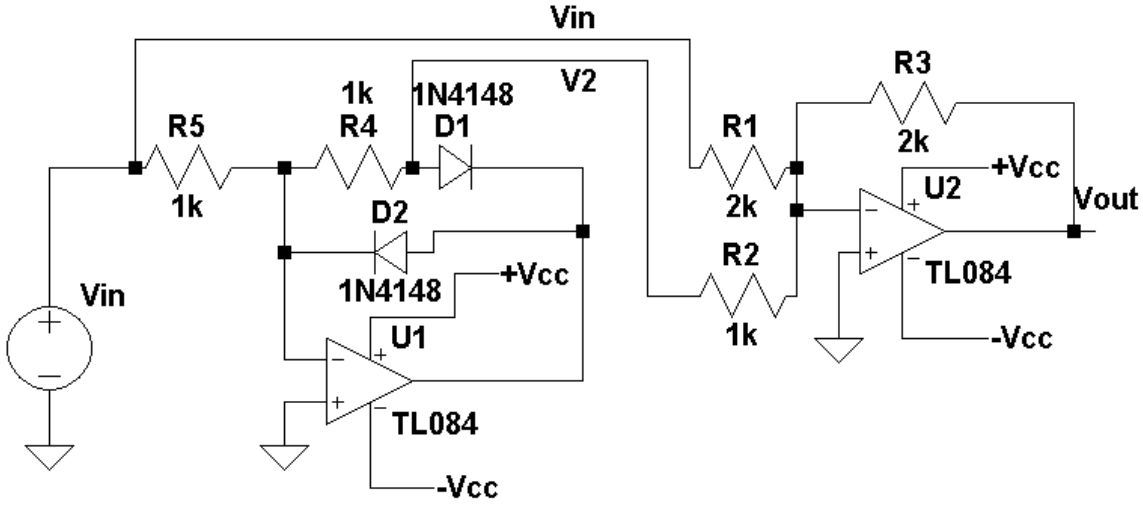


Figure 13: An ideal full wave rectifier.

The Precision Voltage Reference

Many applications require a precision constant DC voltage that does not vary with temperature and is very accurate. Figure 14 shows a schematic diagram for a LM285 a precision voltage reference. The schematic diagram is the same as that used for a zener diode. In addition, using and biasing a precision diode is the same as a zener diode. The only difference between a precision voltage reference and a zener diode is the voltage across the diode remains fairly constant over a large range of bias current, where for a zener diode there is a significant change in voltage across the part as the bias current changes. For the LM285 precision voltage reference, the voltage across the device has a constant voltage of 1.235 volts and has a typical change of voltage of only 7 millivolts over the current range of 10 microamps to 20 milliamps. It has a temperature stability of a typical value of less than 6 millivolt change in voltage over the temperature range of -40 °C to 85 °C.

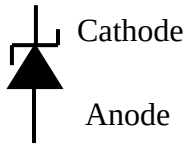


Figure 14: A schematic diagram for a precision voltage reference.

Figure 15 shows how to bias a precision voltage reference. Assuming the current I1 flowing out of the output Vo is zero then I is gvien as

$$I = (Vcc - Vo) / R \quad , \tag{26}$$

where Vo = 1.235 volts. To bias the LM285 a bias current in the range of 0.5 milliamps to 20 milliamps is chosen.

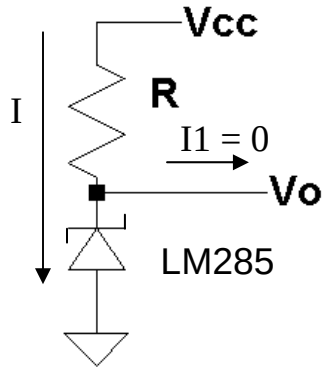


Figure 15: A schematic diagram shown how to bias a precision voltage reference.

Since it was assumed that the current I = 0, typically Vout is connected to an op-amp buffer to produce a gain so the desired voltage reference can be obtained.

Figure 16 gives the circuit diagram for a precision voltage reference using the LM285. The final output is then

$$\text{Vout} = \text{Vo}\left(\frac{\text{R2}}{\text{R1}} + 1\right) \quad . \tag{27}$$

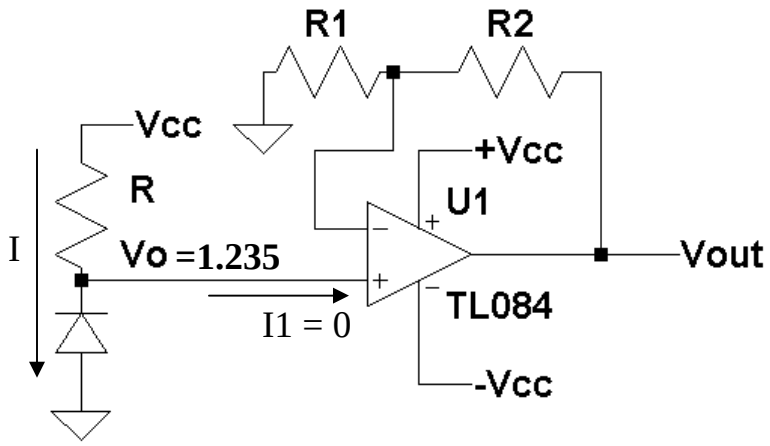


Figure 16: A schematic diagram for precision voltage reference.

But, Vo = 1.235 volts

$$\text{Vout} = 1.235\left(\frac{\text{R2}}{\text{R1}} + 1\right) \quad . \tag{28}$$

To design a precision voltage reference, for a desired output Vout, Equation (28) is used and the ratio of R2 / R1 is found

$$\frac{\text{R2}}{\text{R1}} = \frac{\text{Vout}}{1.235} - 1 \quad . \tag{29}$$

Either R1 or R2 is chosen and the other resistor is calculated from Equation (29). The final step is to solve Equation (26) for R and to calculate R based on the value for Vcc and the desired current I between 10 microamps and 20 milliamps.

The Ideal Diode Limiter

There are many types of limiter circuits that limit the output to a fixed value. Many of these circuits are based upon using ether standard or zener diodes to perform the limiting function. Figure 18a gives the two diode limiter where the voltage limit can be set using resistors. For this derivation and discussion it is assumed that V1 and V2 are much greater than the forward biased voltage Vx of the diodes used so that Vx can be ignored in the derivation. Under this assumption, ideal diodes will be assumed where Vx is assumed to be zero.

Analyzing Figure 18(a) further shows that if V1 > 0 and V2 < 0, both diodes will be off and the output is the simply the circuit shown in Figure 18(b). To satisfy the V1 > 0 and V2 <0, Vout can be found by relating Vout to VR1 and VR2.

The current through R1 and R2 is given as the voltage across R1 and R2 divided by the total resistance R1 and R2

$$I = \frac{VR1 - Vout}{R1 + R2} \tag{30}$$

The voltage across R2 is then found as

$$V(R2) = I \cdot R2 = \frac{VR1 - Vout}{R1 + R2} \tag{31}$$

V1 is sum of V(R2) + Vout or

$$V1 = Vout + R2 \frac{VR1 - Vout}{R1 + R2} \tag{32}$$

Rearranging Equation (32) and combining terms gives

$$V1 = \frac{R2 \cdot VR1 - R1 \cdot Vout}{R1 + R2} \tag{33}$$

For the diode D1 to be off, V1 > 0 as stated earlier. Substituting this fact into Equation (33)

$$0 > \frac{R2 \cdot VR1 - R1 \cdot Vout}{R1 + R2} \tag{34}$$

and solving for Vout yields

$$Vout > -\frac{VR1 \cdot R2}{R1} \tag{35}$$

Using a similar approach in solving for V2 and with the requirement that V2 < 0 for D2 to be off, gives

$$Vout < -\frac{VR2 \cdot R3}{R4} \tag{36}$$

As long as

$$-\frac{VR1 \cdot R1}{R2} < Vout < -\frac{VR2 \cdot R3}{R4} \quad , \tag{37}$$

both diodes will be off and the circuit of Figure 18(b) applies. Figure 18(b) is a circuit for an inverting amplifier with

$$Vout = -\frac{RF}{RA} Vin \tag{38}$$

Figure 17 shows the transfer function of Vout versus Vin. The center curve is represented by Equation (38).

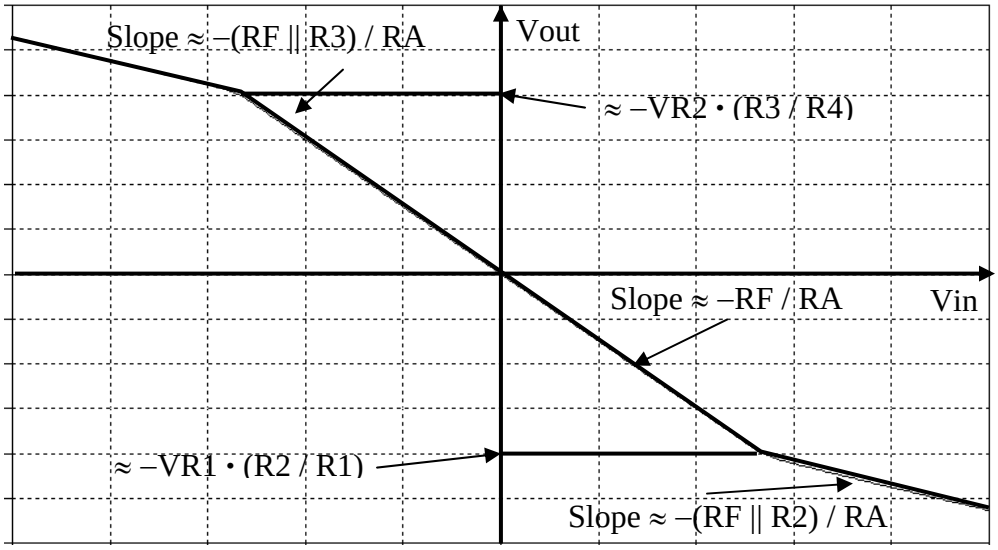


Figure 17: Vout versus Vin for the limiter circuit given in Figure 18.

For the case then V2 > 0, then

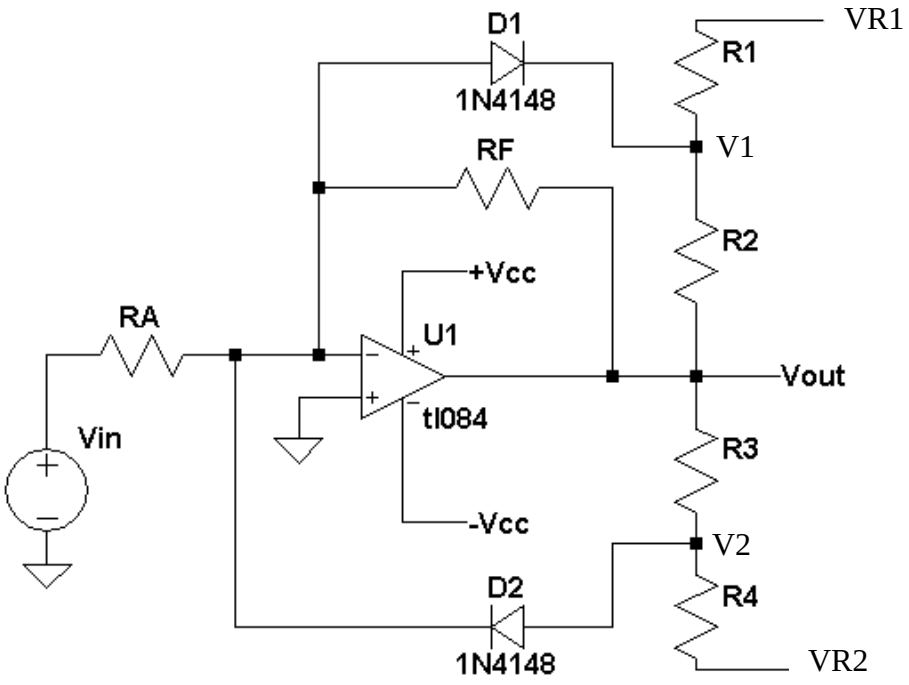
$$Vout > -\frac{VR2 \cdot R3}{R4} \tag{39}$$

and the diode D2 is on and diode D1 is off. With Diode D2 on, the resistor R3 is placed parallel with RF. Vout for this case is then given by

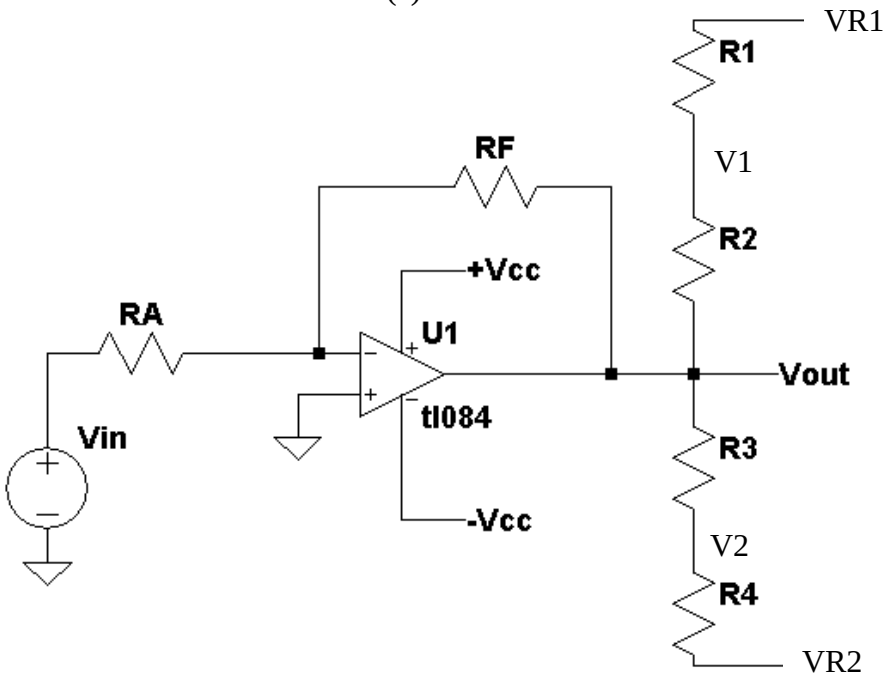
$$Vout = -\frac{R3 \parallel RF}{RA} Vin \tag{40}$$

This is the top left curve in Figure 17. Similarly for the case when V1 < 0, then

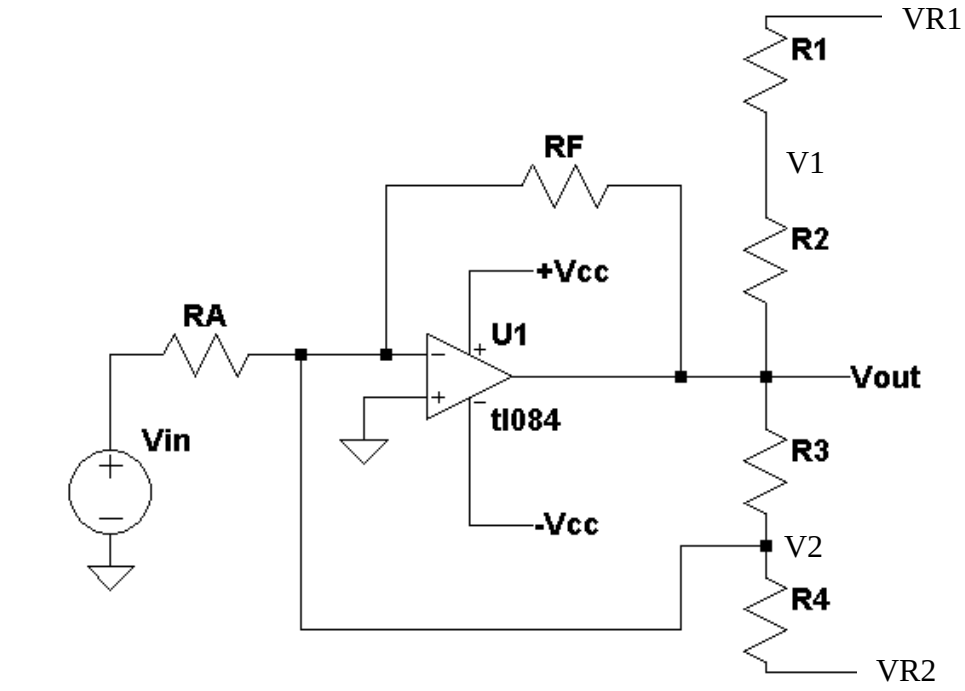
$$Vout < -\frac{VR1 \cdot R2}{R1} \quad , \tag{41}$$


D1
1N4148
VR1
R1
V1
RF
R2
+Vcc
RA
U1
Vout
tl084
Vin
R3
-Vcc
V2
D2
R4
1N4148
VR2

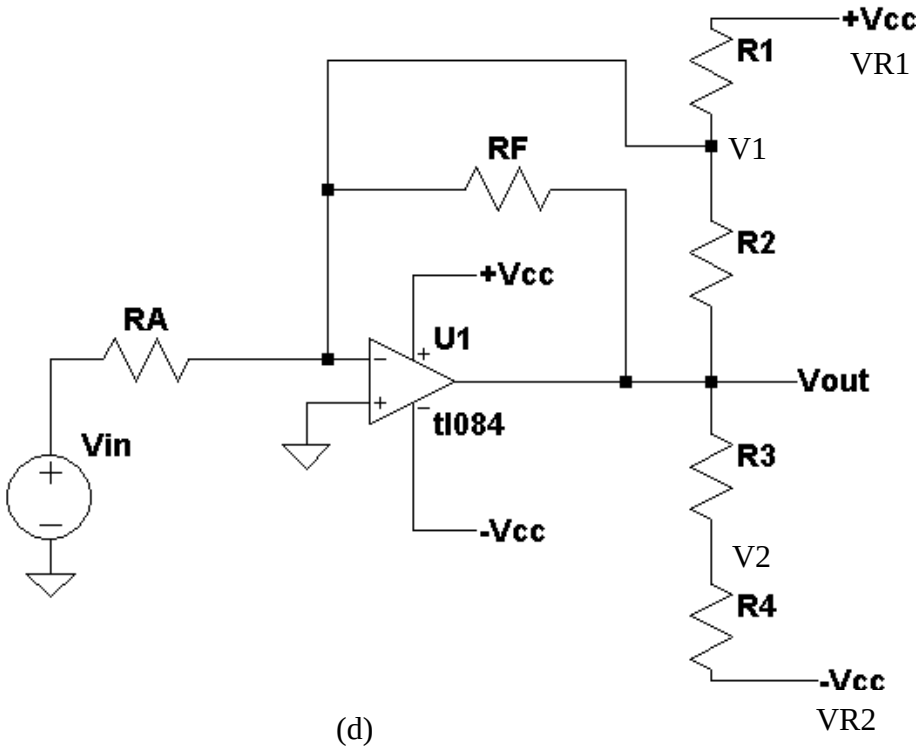
(a)


VR1
R1
RF
V1
R2
+Vcc
RA
U1
Vout
tl084
Vin
R3
-Vcc
V2
R4
VR2

(b)



(c)



(d)

Figure 18: A two diode limiter circuit diagram (a) the actual circuit, (b) the model for when D1 and D2 are both off, (c) the model for when D1 is off and D2 is on, (d) the model for when for D1 is on and D2 is off.

When V1 < 0, diode D1 is on and diode D2 is off as shown in Figure 18(d). Diode D1 on places R2 is parallel with RF and Vout becomes

$$\text{Vout} = -\frac{\text{R2} \parallel \text{RF}}{\text{RA}} \text{Vin} \tag{42}$$

This is the bottom right curve in Figure 16.

Procedure:

General Setup:

1. Record the model and serial number of the scope, power supply, multimeter and function generator used in laboratory experiment.
2. Download the datasheet LM 285 precision voltage reference.
3. When comparing datasheet data values to experimental data use the typical values in the datasheet if given.
4. When measuring any values make sure to measure all inputs as well as the output of the circuit. Do not rely on the values indicated on the instruments. Always measure all signal values.
5. Before turning any power on, double check the wiring to make sure that it is correct.
6. Measure all resistors that are used in the amplifier circuits using the multimeter and record these values.
7. Use all measured values to determine experimental results such as gain and current.
8. Comparing data means to calculate the percent difference between two values. For example, theoretical values versus measured values.
9. Comparing data graphically means to plot the data on the same plot to see how the data overlaps.

Experimental Data

1. Build and design the half wave rectifier circuit given in Figure 3 with R = 1K and the diodes equal to 1N4148s. Set Vin equal to a 200 Hz +10 volt peak-to-peak sine wave with no DC offset. Obtain a plot of Vin and Vout versus time using the oscilloscope.
2. Measure the DC voltage with a multimeter and compare this result to Equation (3).
3. Repeat Step 1 for Figure 7a for R =1K and C = 470 μf. Obtain the peak-to-peak ripple voltage. How does this value compare to Equation (11)? What is the DC voltage at the output Vout? How does this value compare to Equation (13).
4. Build and design the full wave rectifier circuit given in Figure 5 with R = 1K and the diodes equal to 1N4148s. Set Vin to a 200 Hz +10 volt peak-to-peak sine wave with no DC offset. Obtain a plot of Vin and Vout versus time the oscilloscope. Since the output of the full-wave rectifier is not isolated from the input, special care must be taken. Both the ground of the signal generator and the oscilloscope are tied together through electrical ground. So attaching the

signal generator at the input and attaching the oscilloscope at the output shorts the input and output together. To measure the output using the oscilloscope, one of the output leads is tied to one channel of the oscilloscope and the other is tied to an additional channel. Then the math function of the oscilloscope is used to take the difference between the two leads. The ground of the scope is tied to the ground lead of the signal generator

5. Measure the DC voltage with the multimeter and compare the results to Equation (6).
6. Repeat Step 4 for Figure 7b for R =1K and C = 470 μf. Obtain the peak-to-peak ripple voltage. How does this value compare to Equation (12)? What is the DC voltage at the output Vout? How does this value compare to Equation (14).
7. Build and design the ideal half wave rectifier given in Figure 9 for R = 1k. Set Vin to a 200 Hz +10 volt peak-to-peak sine wave with no DC offset. Also set +Vcc = 15 volts and -Vcc = -15 volts. Use this same value for all steps unless otherwise directed. Obtain a plot of Vin and Vout versus time using the oscilloscope.
8. Change the diode orientation in Figure 9 and repeat Step 7.
9. Change the input frequency of the sine wave to 2000 Hz, 20kHz, and 200 kHz and repeat Step 7.
10. Build and design the ideal half wave rectifier given in Figure 11 for R1 = R2 = 1k. Set Vin to a 200 Hz +10 volt peak-to-peak sine wave with no DC offset. Obtain a plot of Vin and Vout versus time using the oscilloscope.
11. Change the diode orientations in Figure 11 and repeat Step 10.
12. Build and design the ideal full wave rectifier given in Figure 13 for R1 = R3 = 2k and R2 = R4 = R5 = 1k. Set Vin to a 200 Hz +10 volt peak-to-peak sine wave with no DC offset. Obtain a plot of Vin and Vout versus time using the oscilloscope.
13. Change the diode orientations in Figure 13 and repeat Step 12.
14. Build and design the precision voltage reference given in Figure 16 for Vout = 5 volts. Set R1 equal to 1K and set the current to the precision voltage reference diode to 1 ma. Measure Vout and V+ and compare this result to the datasheet for the LM285 and the expected Vout.
15. Build and design the limiter circuit given in Figure 18a for RF = RA = 100k, R1 = 20k, R2 = 15k, R3 = 10K, and R4 = 20K. Set Vcc = 10V. Set VR1 = +Vcc and VR2= -Vcc . Using the signal generator, input a sawtooth or triangle wave on Vin that varies from -Vcc to +Vcc and obtain Vout. Compare this result to the plot given in Figure 17.
16. Repeat Step 15 with but remove RF.

Report: Please follow the procedures in this laboratory manual for writing the report for this experiment. Include in your report:

1. The equipment used model and serial number.
2. Laboratory partners
3. Date and time data were taken.

4. Your laboratory report should include the goal of the laboratory experiment.
5. The procedures.
6. The pre-laboratory results.
7. All calculations for each step.
8. All plots generated for each step.
9. All comparisons calculations.
10. For each data collection step in the procedure, there should be either data collected, a calculation performed, a waveform recorded. Please include these in the report.
11. Short summary discussing what is observed for each of the steps given in the laboratory experiment.
12. Also include what you learned.
13. Make sure to include a discussion on how the frequency of the input affects the output of the ideal half wave rectifiers.
14. Discuss the difference between the ideal half wave and full wave rectifiers and the non-ideal half wave and full wave rectifiers.
15. Discuss the effect of filtering the output of a half and full wave rectifier.

EXPERIMENT #6

Active Filters

Goals:
To introduce the concepts of using an operational amplifier to perform filtering of electrical signals. Both the lowpass and highpass filters will be investigated. The equations for first order and second order filters will also be given. The frequency response of the various filters will be measured and compared with expected results.

References:

Microelectronics-Circuit Analysis and Design, D. A. Neamen, McGraw-Hill, 4th Edition, 2007, ISBN: 978-0-07-252362-1.

The following link is to the Tektronix website for the user manual for the DPO 4034B oscilloscope:
http://www2.tek.com/cmswpt/madetails.lotr?ct=MA&cs=mur&ci=16272&lc=EN

Equipment:

Oscilloscope: DPO4034B
Triple Power supply
Signal generator
Capacitors available in the laboratory
Resistors available in the laboratory (minimum filter resistor should be 10kΩ)

Pre-laboratory:

Read this laboratory experiment carefully to become familiar with the background and the procedural steps in this experiment. Carefully read each section and become familiar with the equations for each circuit.

Using the simulation package of your choice in which you are the most familiar with: Mulitsim, Workbench or LTSpice IV simulate the following filters.
Simulate using a pulse input of 0 to 1 volt to the filter and compare one cycle to the equations below.

First order Filters:

a. Simulate a first order lowpass filter using the circuit given in Figure 4 with ωo = 10,000 rad / sec.
b. Using the AC simulation mode of the simulator obtain the lowpass filter magnitude spectrum from 10 Hz to 10,000 Hz.
c. Determine the attenuation factor in dB / Decade from Step b.
d. Apply a 1 volt peak square input with a frequency of 500 Hz. Simulate and plot the time response of this filter. Use 1 μsec rise and fall times, or less, for

the pulse generator.

e. Simulate a first order highpass filter using the circuit given in Figure 7 with ωo = 10,000 rad / sec.
f. Using the AC simulation mode of the simulator obtain the highpass filter magnitude spectrum from 10 Hz to 10,000 Hz.
g. Determine the attenuation factor in dB / Decade from Step f.
h. Apply a 1-volt peak square input with a frequency of 500 Hz. Simulate and plot the time response of this filter. Use 1 μsec rise and fall times, or less, for the pulse generator.

Second order Filters

i. Simulate a second order lowpass filter using the circuit given in Figure 10 with ωo = 10,000 rad / sec with Q = 2.
j. Using the AC simulation mode of the simulator, obtain the lowpass filter magnitude spectrum from 10 Hz to 10,000 Hz.
k. From Step j, measure Vout at $\omega = \omega o$ and compare this result to $K \cdot Q$.
l. Apply a 1 volt peak square input with a frequency of 500 Hz. Simulate and plot the time response of this filter. Use 1 μsec rise and fall times, or less, for the pulse generator.
m. Measure the peak overshoot and compute the percent overshoot using Equation (31)
n. Repeat Steps l and m for Q = 0.5, 1, and 5. How do these simulations compare to Figure 12?
o. Compare the measured % overshoot to the calculated value from Equation (31).
p. Simulate a second order highpass filter using the circuit given in Figure 13 with ωo = 10,000 rad / sec with Q = 2.
q. Using the AC simulation mode of the simulator, obtain the highpass filter magnitude spectrum from 10 Hz to 10,000 Hz.
r. From Step q, measure Vout at $\omega = \omega o$ and compare this result to $K \cdot Q$.
s. Apply a 1 volt peak square input with a frequency of 500 Hz. Simulate and plot the time response of this filter. Use 1 μsec rise and fall times, or less, for the pulse generator.
t. Repeat Step s for Q = 0.5, 1, and 5. How does these simulations compare to Figure 15?

Butterworth Filter

u. Simulate a fifth order lowpass Butterworth filter using the steps described in the laboratory experiment with ωo = 10,000 rad / sec and Kd = 5. The attenuation factor should be -100 dB / Decade.
v. Using the AC simulation mode of the simulator obtain the lowpass filter magnitude spectrum from 10 Hz to 10,000 Hz.
w. From Step v, measure Vout at $\omega = \omega o$.
x. Apply a 1 volt peak square input with a frequency of 200 Hz. Simulate and plot the time response of this filter. Use 1 μsec rise and fall times, or less, for the pulse generator.

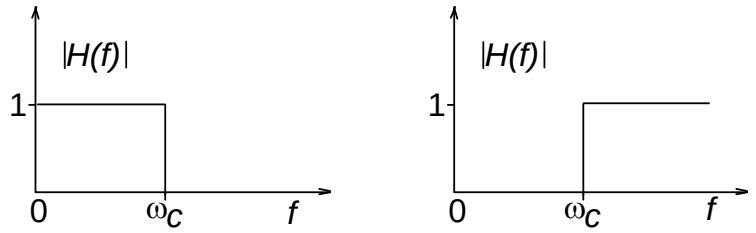
Discussion:

Filtering of a signal is an important aspect of electronic signal processing. It provides a means of reducing the noise present in a signal and means of removing unwanted interference. Filtering of a signal is easily implemented using resistor, inductor and capacitor circuits or resistor, capacitor and op-amp circuits. The classification of a filter is based upon which frequency components have been attenuated.

There are four major types of filters. An ideal lowpass filter is defined as one that contains no transition set of frequencies in which the filter goes from passing frequency components to the attenuation of frequency components:

$$H(\omega) = \begin{cases} 1 \text{for } \omega \le \omega_C \\ 0 \text{for } \omega > \omega_C \end{cases} . \qquad (1)$$

Figure 1(a) shows a plot of its magnitude spectrum. This filter has a finite discontinuity at the cutoff frequency ω_C.



(a) (b)

Figure 1: The magnitude spectrums for (a) the ideal lowpass filter and (b) the ideal highpass filter.

In a similar way, the ideal highpass filter is defined as

$$H(\omega) = \begin{cases} 1 \text{for } \omega \ge \omega_C \\ 0 \text{for } \omega < \omega_C \end{cases} . \qquad (2)$$

This ideal filter also has a finite discontinuity. Figure 1(b) gives the highpass filter magnitude spectrum. The ideal lowpass and highpass filters presented above cannot be built using electronic components as these filters would need an infinite number of storage elements such as capacitors and inductors.

Realistic filters do not have a sharp or zero transition band of passing frequency components to attenuate frequency components. Figure 2 shows the three bands associated with a typical filter. The pass band is the band where frequency components of the input to the filter essentially remain unchanged. The attenuation band is where the frequency components of the input are attenuated

and the transition band is the band where the filter transitions from passing frequency components to attenuating frequency components.

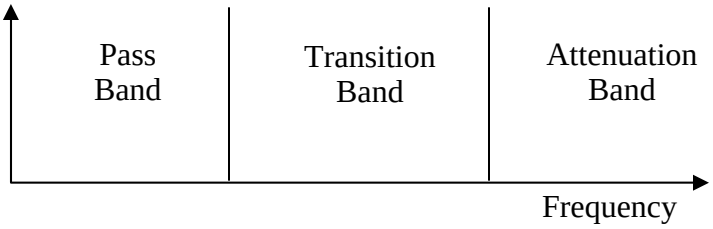


Figure 2: The three regions of a filter.

Figure 3(a) gives the magnitude spectrum for a typical lowpass filter. This filter passes the frequencies below the cutoff frequency ω_c and attenuates the frequency components above the cutoff frequency. As shown in Figure 3(a), there is a gradual transition from passing frequency components to attenuating frequency components. Figure 3(b) gives a typical highpass filter. This filter passes the high frequency components above the cutoff frequency ω_c and attenuates the low frequency components.

Figure 3(c) gives the magnitude spectrum for a bandpass filter. This filter passes frequency components in the range of frequencies ω_1 to ω_2, with the center frequency of the pass band given by ω_0. The final filter is the band-reject filter, given in Figure 3(d). This filter attenuates the frequency components in the range of ω_1 to ω_2.

There are many types of electronic filters that are available. Many of these filters come directly from electronic circuit designs that have existed for many decades. Some of the most common ones are the *Butterworth*, *elliptical*, *Chebyshev*, and *Bessel* filters as well as the simple first order resistor and capacitor network and the second order resistor, capacitor, and inductor network. In this laboratory experiment, the buffered version of the lowpass and highpass resistor-capacitor filter circuits will be investigated along with the lowpass and highpass second order resistor, capacitor, and op-amp filter circuits known as active filters.

First Order Filters

Figure 4 shows the circuit used to implement a buffered version of a first order lowpass filter. The op-amp is nothing more than a unity gain buffer isolating the output of the R-C filter. The transfer function of this filter is given as

$$H(s) = \frac{Vout(s)}{Vin(s)} = \left(\frac{1}{\frac{s}{\omega o} + 1} \right) \quad , \qquad (3)$$

where ωo = (RC)$^{-1}$ and is known as the cutoff frequency of the filter.

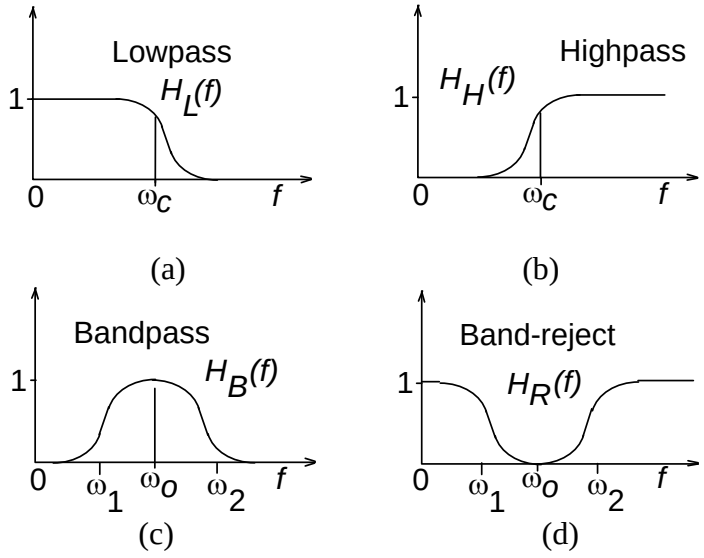


Figure 3: Normalized frequency response curves of four common one-dimensional filters used in Fourier filtering; (a) the lowpass filter, (b) the highpass filter, (c) the bandpass filter, and (d) band-reject filter.

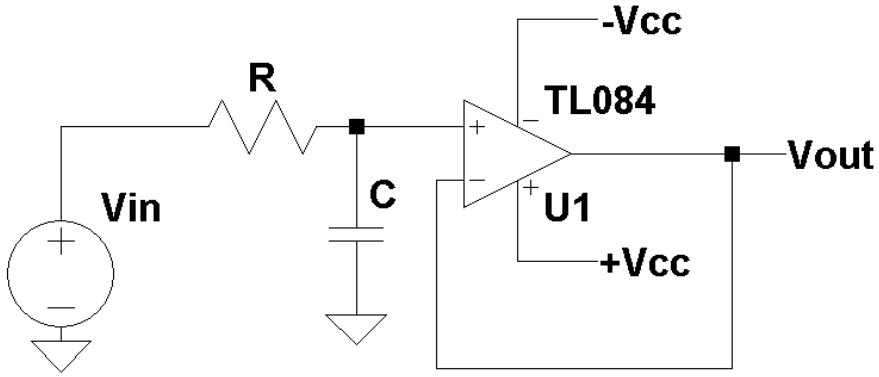


Figure 4: A buffered version of a first order lowpass filter.

Letting s = jω and substituting it into Equation (3) gives

$$H(j\omega) = \frac{Vout(\omega)}{Vin(\omega)} = \left(\frac{1}{\frac{j\omega}{\omega o} + 1} \right) \qquad (4)$$

The magnitude and phase are then given by

$$| H(j\omega) | = | \frac{Vout(\omega)}{Vin(\omega)} | = \left(\frac{1}{\sqrt{\frac{\omega}{\omega o}^2 + 1}} \right) \tag{5}$$

and

$$\arg(H(j\omega)) = \arg(\frac{Vout(\omega)}{Vin(\omega)}) = -\arctan\left(\frac{j\omega}{\omega o}\right) \quad . \tag{6}$$

At the frequency ωo, the magnitude is equal to $1 / \sqrt{2}$ and the phase is equal to -45°. The magnitude in decibels (dB) is found by

$$| H(\omega) | \text{ in dB} = 20 \log(| H(\omega) |) \tag{7}$$

At the cutoff frequency ωo, the magnitude in dB is equal to -3.01 dB or simply -3dB. Below the cutoff frequency ωo, the response of the filter is one and the frequency components of the filter input remains unchanged. Above the cutoff frequency, the frequency components are attenuated at a rate of -20dB per decade.

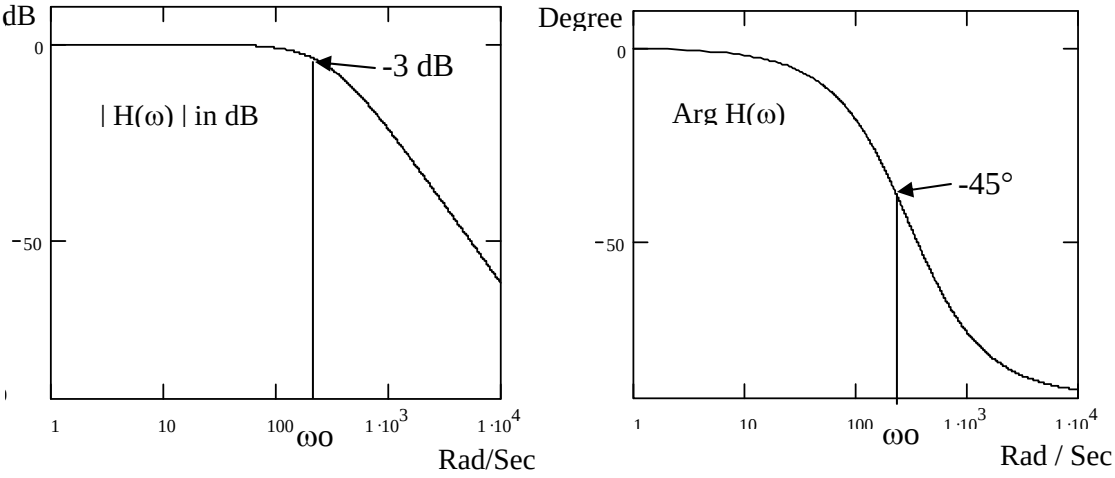


Figure 5: The magnitude and phase spectrums for a first order lowpass R-C filter.

The response to a step input can be found by taking the inverse Laplace transform of

$$Vout(s) = \frac{1}{s} \cdot \left(\frac{1}{\frac{s}{\omega o} + 1} \right) \quad , \tag{8}$$

with the Laplace transform of a unit step u(t) equal to 1 / s and is given as

$$Vout(t) = (1 - e^{-t/RC}) \, u(t) \tag{9}$$

A plot of Equation (9) is given in Figure 6.

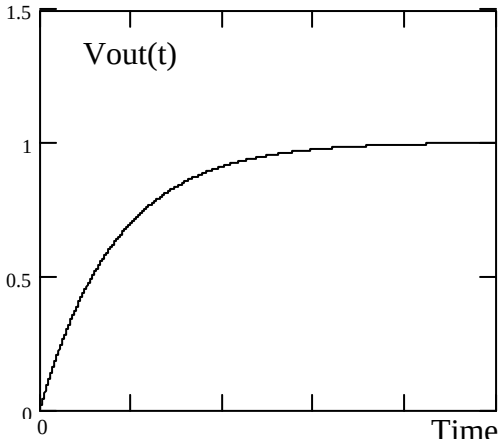


Figure 6: The step response to a first order lowpass R-C filter

The same procedures are used to find the frequency and time response for a first order highpass filter. Swapping the capacitor and resistor in Figure 4 changes the first order lowpass filter to a first order highpass filter, shown in Figure 7(a).

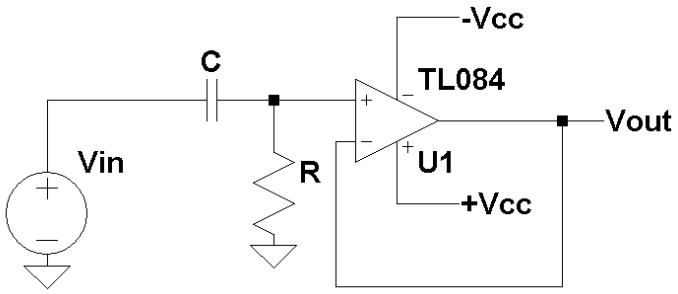


Figure 7(a): A buffered first order highpass R-C filter.

The transfer function of this filter is given as

$$H(s) = \frac{Vout(s)}{Vin(s)} = \left(\frac{\frac{s}{\omega o}}{\frac{s}{\omega o} + 1} \right) \quad , \qquad (10)$$

where $\omega o = (RC)^{-1}$ and is known as the cutoff frequency of the filter. Letting $s = j\omega$ and substituting it into Equation (10) gives

$$H(j\omega) = \frac{Vout(\omega)}{Vin(\omega)} = \left(\frac{\frac{j\omega}{\omega o}}{\frac{j\omega}{\omega o} + 1} \right) \quad . \qquad (11)$$

The magnitude and phase are then given by

$$| H(j\omega) | = | \frac{Vout(\omega)}{Vin(\omega)} | = \left(\frac{\frac{\omega}{\omega o}}{\sqrt{\frac{\omega}{\omega o}^2 + 1}} \right) \qquad (12)$$

and

$$\arg(H(j\omega)) = \arg(\frac{Vout(\omega)}{Vin(\omega)}) = 90° - \arctan\left(\frac{j\omega}{\omega o}\right) \quad . \qquad (13)$$

At the frequency ωo, the magnitude is equal to $1 / \sqrt{2}$ and the phase is equal to +45°. The magnitude in decibels (dB) is found by Equation (7). At the cutoff frequency ωo, the magnitude in dB is equal to -3dB.

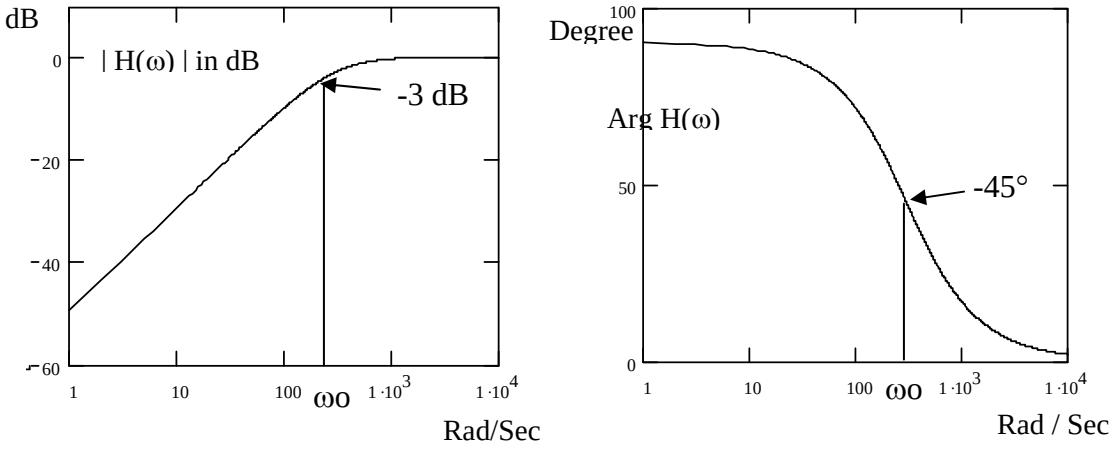


Figure 7(b): The magnitude and phase spectrums for a first order highpass R-C filter.

Below the cutoff frequency, the frequency components are attenuated at a rate of 20dB per decade (Figure 7(b)). Above the cutoff frequency ωo, the response of the filter is one and these frequency components remain unchanged.

The response to a step input can be found by taking the inverse Laplace transform of

$$Vout(s) = \frac{1}{s} \cdot \left(\frac{\frac{s}{\omega o}}{\frac{s}{\omega o} + 1} \right) = \left(\frac{\frac{1}{\omega o}}{\frac{s}{\omega o} + 1} \right) \quad , \qquad (14)$$

with the Laplace transform of a unit step u(t) equal to 1 / s and is given as

$$Vout(t) = e^{-t/RC} u(t) \qquad (15)$$

A plot of Equation (15) is given in Figure 8.

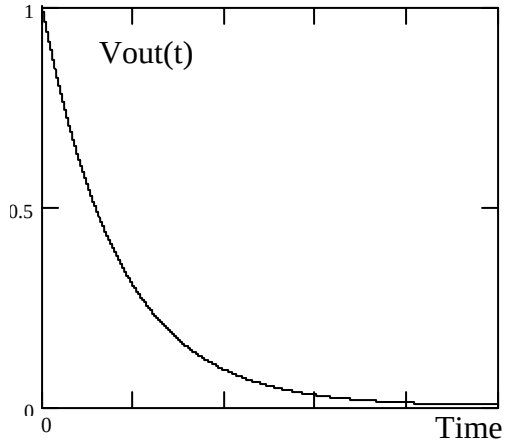


Figure 8: The step response to a first order highpass R-C filter

Second Order Filters

Figure 9 shows the circuit used to implement a buffered version of a second order lowpass filter. This circuit uses both positive and negative feed back to achieve a second order system. The transfer function of this filter is given as

$$H(s) = \frac{Vout(s)}{Vin(s)} = \frac{K \cdot \omega o^2}{s^2 + \frac{\omega o}{Q} s + \omega o^2} \qquad (16)$$

where the cutoff frequency ωo (-3 dB point) is given by

$$\omega o^2 = \frac{1}{C1\ C2\ R1\ R2} \quad , \qquad (17)$$

the gain K by

$$K = \frac{Rb}{Ra} + 1 \quad , \qquad (18)$$

and the Quality factor Q by

$$\frac{1}{Q} = \left(\frac{R2\ C2}{R1\ C1}\right)^{1/2} + \left(\frac{R1\ C2}{R2\ C1}\right)^{1/2} + (1\text{-}K)\left(\frac{R1\ C1}{R2\ C2}\right)^{1/2} \qquad (19)$$

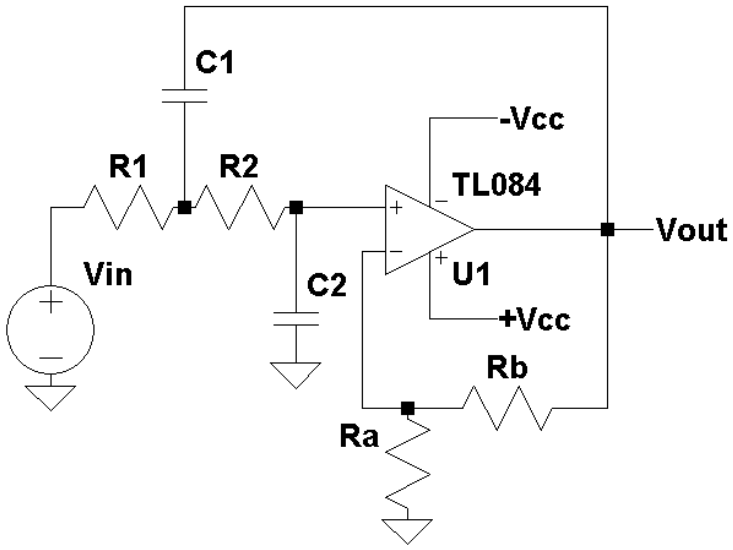


Figure 9: The circuit diagram for a second order lowpass filter.

If both R1 and R2 are is set equal to R and C1 and C2 are set equal to C then the cutoff frequency ωo reduces to

$$\omega o = \frac{1}{R\,C} \quad , \tag{20}$$

the quality factory becomes

$$\frac{1}{Q} = 3 - K \quad , \tag{21}$$

or

$$K = 3 - \frac{1}{Q} \quad , \tag{22}$$

and the gain remaining the same as Equation (18)

$$K = \frac{Rb}{Ra} + 1 \quad , \tag{23}$$

A closer look at Equation (21), with R1 = R2 = R and C1 = C2 = C shows that the quality factor and the gain K are no longer independent and a directly coupled by Equations (21) or (22). In designing this second order filter, highest priority is that the desired Q must first be met. If the gain K, does not meet the desired gain as set forth by the design requirement, it is much easier to add an additional

amplifier stage to increase the overall gain or to add a voltage divider to reduce the overall gain to the desired level. Figure 10 shows the circuit diagram for the second order lowpass filter with R1 =R2 =R and C1 = C2 = C.

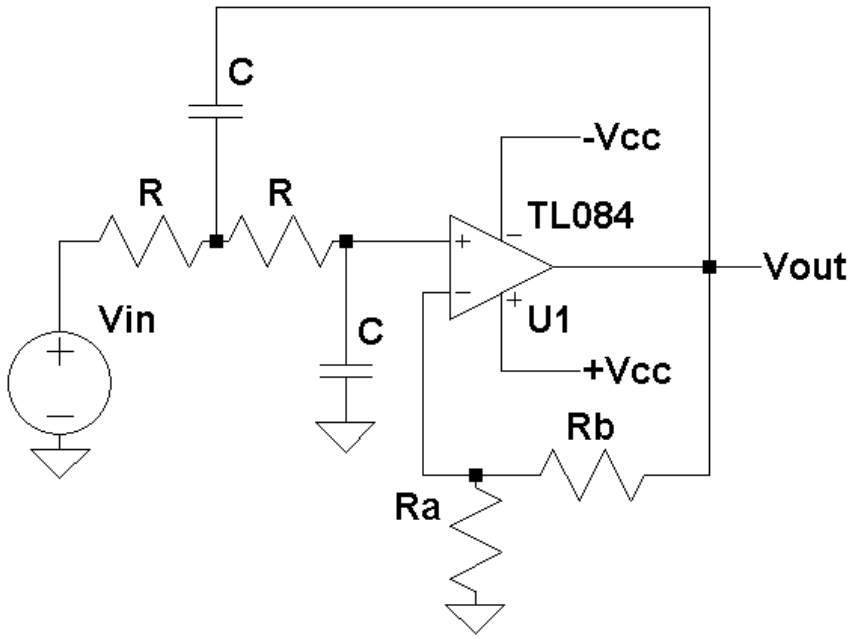


Figure 10: The circuit diagram for a second order lowpass with R1 = R2 = R and C1 = C2 = C filter.

The frequency response of this filter can be found by substituting s = jω into Equation (16), giving

$$H(\omega) = \frac{Vout(\omega)}{Vin(\omega)} = \frac{K \cdot \omega o^2}{\frac{\omega o}{Q} j\,\omega + (\omega o^2 - \omega^2)} \tag{24}$$

The magnitude response is found from Equation (24) as

$$| H(\omega) | = f(Vout(\omega), Vin(\omega)) = \frac{K \cdot \omega o^2}{\sqrt{\frac{\omega o^2}{Q^2}\omega^2 + (\omega o^2 - \omega^2)^2}} \tag{25}$$

At ω = ωo, Equation (25) reduces to

$$H(\omega o) = \frac{Vout(\omega o)}{Vin(\omega o)} = -j \cdot K \cdot Q \tag{26}$$

The magnitude of | H(ωo) | is equal to K · Q and the phase is -90°. At resonance, the gain of the filter increased by the quality factor Q. Figure 11 gives the lowpass filter response for various quality factor Q values with the value of K set equal to one for all cases.

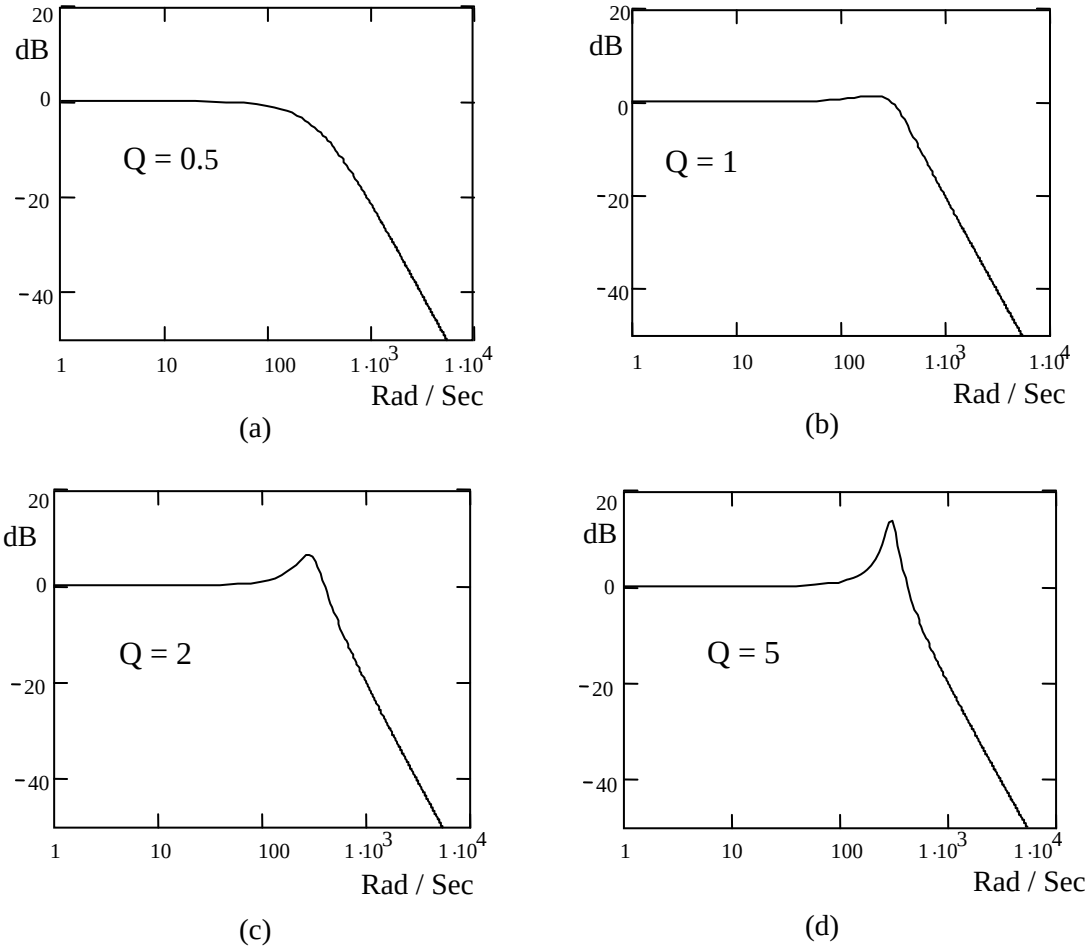


Figure 11: The magnitude spectrum for the second order lowpass filter given in Equation (16) for various quality factor values.

The attenuation factor for a second order filter is -40 dB / decade as compared for a first order system of -20 dB / decade. The rate of attenuation is twice as fast as a first order lowpass filter. As the Q increases, the increase in the gain of the filter response at ω = ωo can be easily seen in Figure 11 (comparing Figure 11a to Figure 11b).

Applying a step input of u(t) with a corresponding Laplace transform for u(t) of 1 / s yields

$$Vout(s) = \frac{1}{s} \frac{K \cdot \omega o^2}{s^2 + \frac{\omega o}{Q} s + \omega o^2} \tag{27}$$

Using partial fraction expansion, the standard Laplace tables, and some algebra gives the step response for a second order lowpass filter as described by Equation (16) as

$$Vout(t) = K\left(1 - \frac{e^{-\omega o \, . \, t / (2Q)}}{\sqrt{1 - \frac{1}{4Q2}}} \sin\left(\sqrt{1 - \frac{1}{4Q2}}\, \omega o \, t + \right)\right) \quad , \tag{28}$$

where

$$\theta = \text{atan}\left(\frac{\sqrt{1 - \frac{1}{4Q^2}}}{\frac{1}{2Q}}\right) = \text{atan}\left(\sqrt{4Q^2 - 1}\right) \tag{29}$$

Figure 12 shows the step response for a fixed cutoff frequency ωo and for various quality factors, Q. These factors correspond to the same quality factors used to generate the magnitude spectrums given in Figure 11, except that for these plots, K is not set to one, but set using Equation (22). For Q > 0.5 there is ringing present. The frequency of this ringing ωr is given by

$$\omega r = \sqrt{1 - \frac{1}{4Q^2}}\, \omega o \tag{30}$$

which is different from the resonance frequency ωo. Note, that the increase in ringing and the amount of overshoot in the waveform are due to an increase value of Q. For Q = 0.5 there is no ringing and no overshoot. Actually, for Q <0.5 the second order transfer function of Equation(16) can be factored into two real poles and can be implemented using the two first order lowpass filters shown in Figure 4. The percent overshoot given in the step responses is defined as

$$\% \text{ overshoot} = \frac{Vpeak - Vfinal}{Vfinal} 100\% \quad , \tag{31}$$

where Vpeak is the peak voltage in the step response and Vfinal is final value of the step response after the ringing has decayed to zero as shown in Figure 12. In summary, the higher value of Q the higher the overshoot. J. C. Daly from the Electrical and Computer Engineering at the University of Rhode Island gives the percent overshoot as a function of Q as

$$\% \text{ overshoot} = e^{-\frac{\pi}{\sqrt{4Q^2 - 1}}} 100\% \tag{32}$$

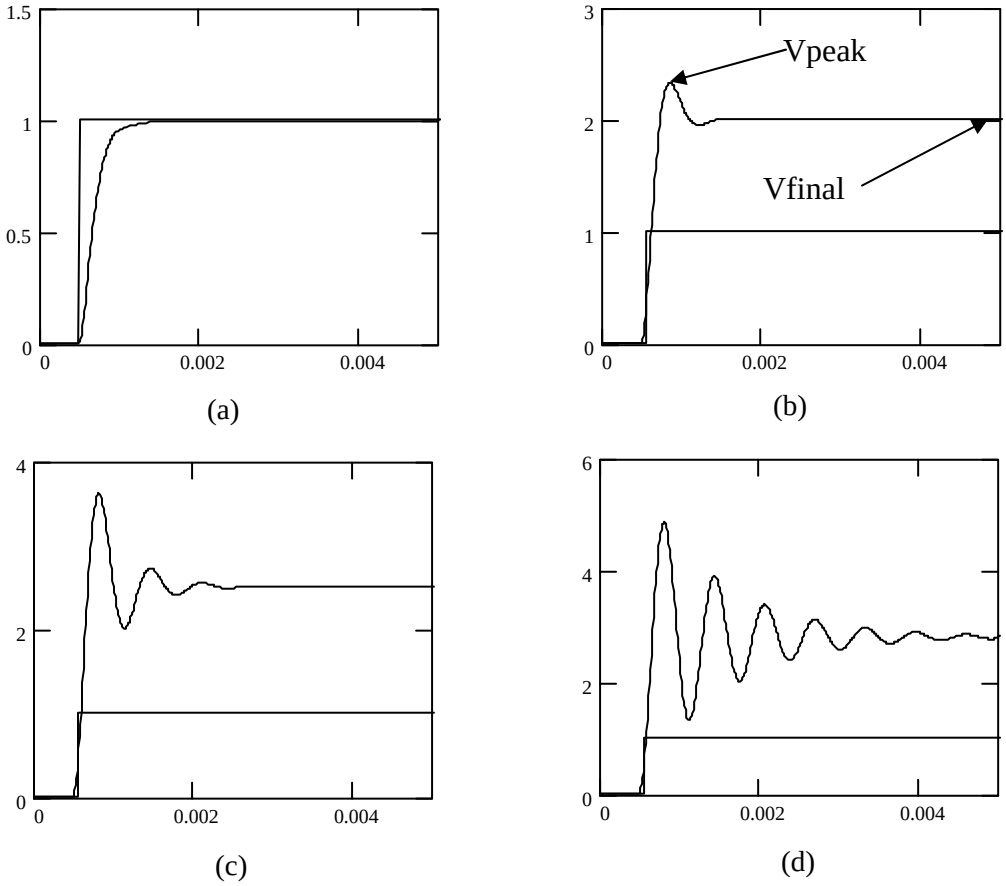


Figure 12: The step response for the second order lowpass filter given in Equation (16) for various quality factor values. For (a) Q = 0.5, (b) Q = 1, (c) Q = 2, and (d) Q = 5.

Figure 13 gives the circuit used to implement a buffered version of a second order highpass filter for R1 = R2 = R and C1 = C2 = C. The only difference between this filter and the lowpass version of this filter is that the R's and the C's are swapped. The transfer function of this filter is given as

$$\text{Vout}(s) = \frac{K \cdot s^2}{s^2 + \frac{\omega o}{Q} s + \omega o^2} \quad , \tag{33}$$

where

$$\omega o = \frac{1}{R\,C} \quad , \tag{34}$$

$$\frac{1}{Q} = 3 - K \quad , \tag{35}$$

or

$$K = 3 - \frac{1}{Q} \quad , \tag{36}$$

and

$$K = \frac{Rb}{Ra} + 1 \quad . \tag{37}$$

which are the same equations as Equations (20) - (23), repeated here for clarity.

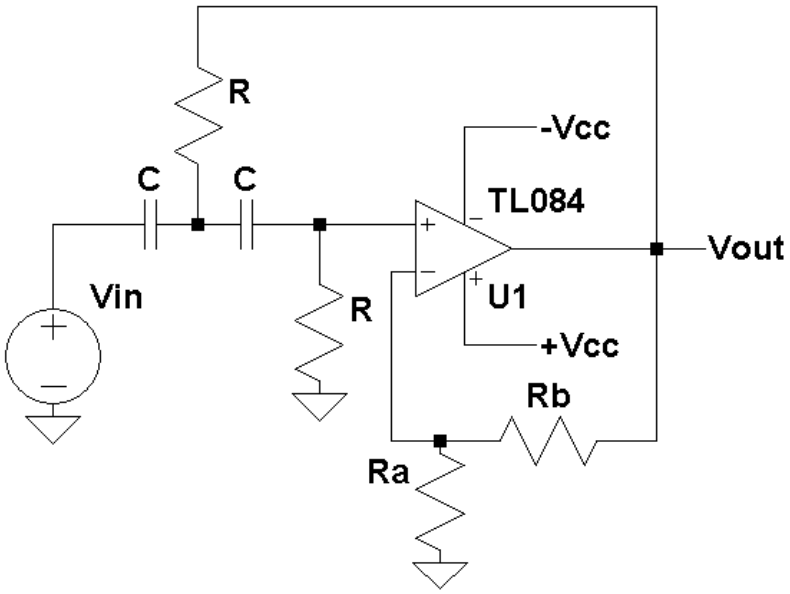


Figure 13: The circuit diagram for a second order highpass with R1 = R2 = R and C1 = C2 = C filter.

The frequency response of this filter can be found by substituting s = jω into Equation (16)

$$H(\omega) = f(Vout(\omega),Vin(\omega)) = \frac{-K \cdot \omega^2}{\frac{\omega o}{Q} j\omega + (\omega o^2 - \omega^2)} \tag{38}$$

The magnitude response is found from Equation (24) as

$$| H(\omega) | = f(Vout(\omega),Vin(\omega)) = \frac{K \cdot \omega^2}{\sqrt{\frac{\omega o^2}{Q^2}\omega^2 + (\omega o^2 - \omega^2)^2}} \tag{39}$$

At $\omega = \omega o$, Equation (25) reduces to

$$H(\omega o) = \frac{Vout(\omega o)}{Vin(\omega o)} = j \cdot K \cdot Q \tag{40}$$

The magnitude of $| H(\omega o) |$ is equal to $K \cdot Q$ and the phase is 90°. At resonance, the gain of the filter increased by the quality factor Q. This is the same gain factor as for the second order lowpass filter but the difference is the phase is +90° for the high pass and -90° for the lowpass filter. Figure 14 gives the highpass filter response for various quality factors values with the value of K set equal to one for all cases.

Applying a step input of u(t) with a corresponding Laplace transform of u(t) as 1 / s yields

$$Vout(s) = \frac{1}{s}\frac{K \cdot s^2}{s^2 + \frac{\omega o}{Q}s + \omega o^2} = \frac{K \cdot s}{s^2 + \frac{\omega o}{Q}s + \omega o^2} \tag{41}$$

Using standard Laplace tables and some algebra gives the step response for a second order highpass filter as described by Equation (33) as

$$Vout(t) = K\, e^{-wo \cdot t / (2Q)} \cdot \left(\cos\left(\sqrt{1 - \frac{1}{4Q^2}}\, wo\, t \right) - \frac{1}{\sqrt{4Q^2 - 1}} \sin\left(\sqrt{1 - \frac{1}{4Q^2}}\, wo\, t \right) \right) \tag{42}$$

The Butterworth Filter

The Butterworth filter offers the ability to control the rate at which the filter changes from passing frequency components to attenuating them. In addition, this filter linearly changes from the pass band to the attenuation band without the presence of the ripples that are typically found in some of the other filters. This filter is known as a *maximumly flat filter*.

The Butterworth lowpass filter is described by

$$H(\omega) = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega o}\right)^{2N}}}\ , \tag{43}$$

where N is the order of the filter and ωo is the cutoff frequency or -3 dB attenuation point. As N increases, the transition band at which the filter's frequency response changes from the pass band to the attenuation band decreases. For N = ∞, the lowpass Butterworth filter becomes the ideal lowpass filter with zero transition band. The rate of attenuation is -N · 20 dB / decade. For ω = 0, the response of this filter is unity and at ω = → ∞, the response is zero. Similar to the Butterworth lowpass filter, the Butterworth highpass filter is defined as

$$H(\omega) = \frac{1}{\sqrt{1 + \left(\frac{\omega o}{\omega}\right)^{2N}}} \quad , \tag{44}$$

For ω = 0, the response of this filter is zero and for ω → ∞ , the response is one.

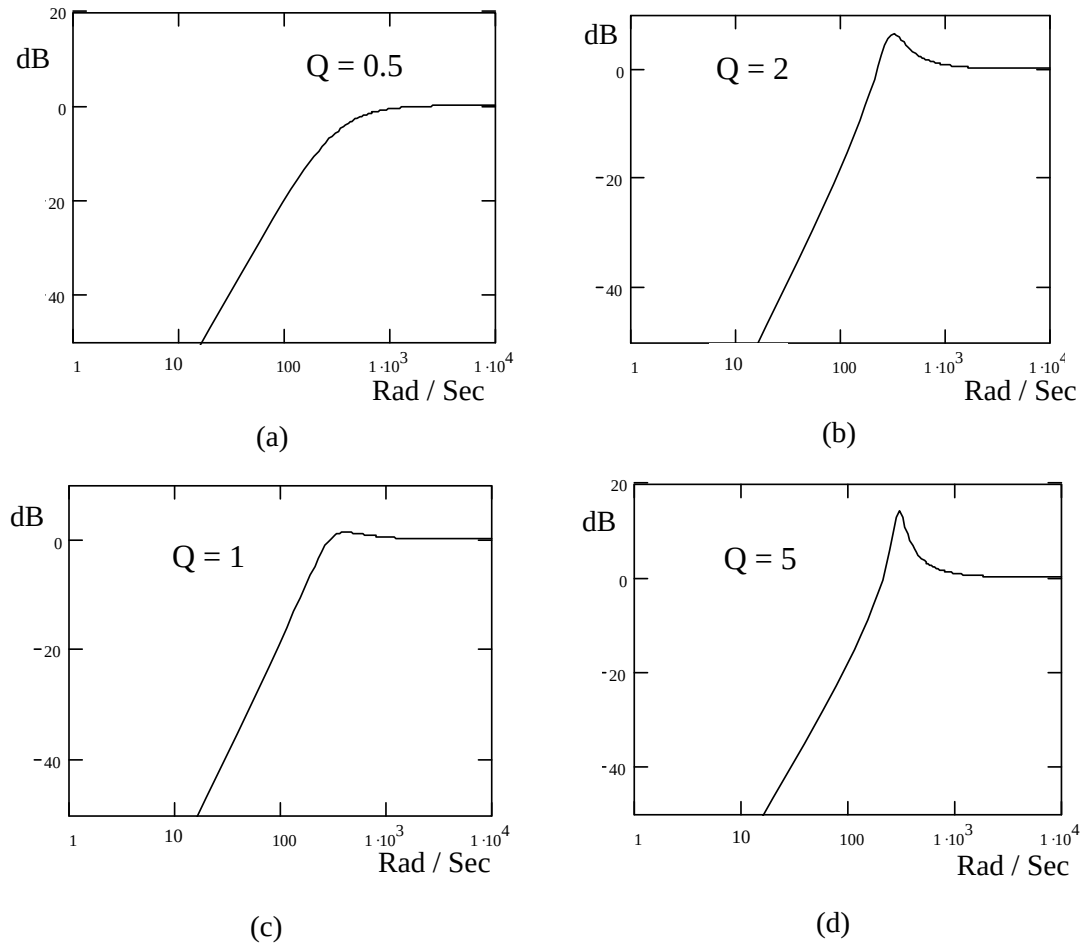


Figure 14: The magnitude spectrum for the second order highpass filter given in Equation (16) for various quality factor values.

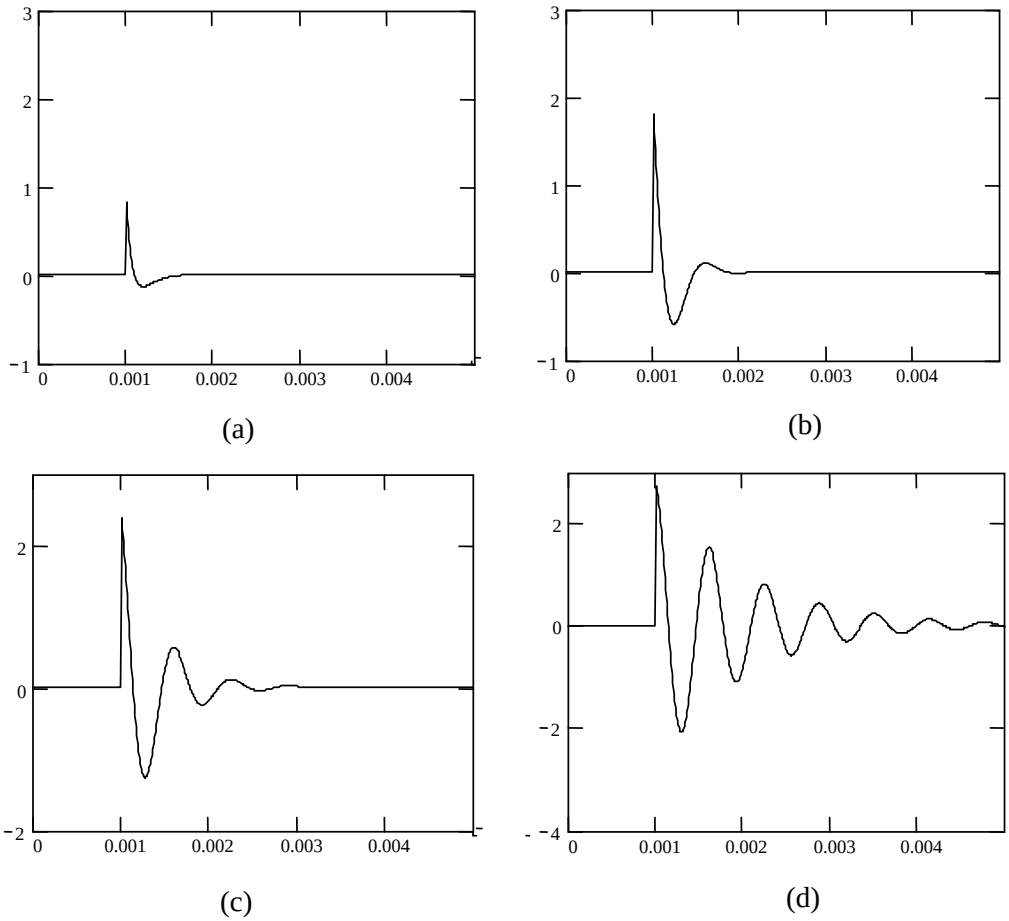


Figure 15: The step response for the second order highpass filter, given in Equation (33) for various quality factor values. For (a) Q = .5, (b) Q = 1, (c) Q = 2, and (d) Q = 5.

To design a Butterworth filter, the locations of the poles are required. Most tables that give the Butterworth poles are computed with a normalized cutoff frequency of $\omega o = 1$. Table 1 gives the poles for up to a 7^{th} order filter factored into first and second order terms for a normalized frequency $\omega o = 1$. The advantage of this table is that a high order filter can be implemented by cascading several second order filters with a first order filter. For example, if N = 6, there will three second order filter stages and no first order stage.

The steps involved in designing an Nth order Butterworth lowpass filter is as follows.

1. Pick the order N of the filter and the desired filter gain Kd (the desired gain of the overall filter) and cutoff frequency ωo.
2. Using Table 1, obtain the normalized factored poles $\omega o = 1$ for the given N.

3. For N odd, there will be an (s + 1) pole. This can be easily implemented with the first order lowpass filter given in Figure 4. Pick C and find R from

$$R = \frac{1}{C\,\omega o} \tag{45}$$

4. For each second order section (Figure 10) and Equation (16), the K and Q must be found. This is done by using the corresponding constant in front of the s term in the second order pole equation. This term is equal to ωo / Q. But ωo is equal to 1 so this term is simply equal to 1 / Q.

Table 1: The factored Poles for a Butterworth Filter.

N	Second order Factored Butterworth filter Normalized Poles (ωo = 1)
1	(s + 1)
2	(s^2 + 1.414s + 1)
3	(s + 1) (s^2 + s + 1)
4	(s^2 + 0.7654s + 1) (s^2 + 1.847s + 1)
5	(s +1) (s^2 + 1.618s + 1) (s^2 + 0.618s + 1)
6	(s^2 + 0.5176s + 1) (s^2 + 1.414s + 1) (s^2 + 1.9319)
7	(s + 1) (s^2 + 0.445s + 1) (s^2 + 1.247s + 1) (s^2 + 1.8019s + 1)

5. Using

$$K = 3 - \frac{1}{Q} \quad , \tag{46}$$

solve for K given Q from step 4 and with

$$K = \frac{Rb}{Ra} + 1 \quad . \tag{47}$$

Pick Ra or Rb and then solve Equation (47) for the other resistor (Ra or Rb).

6. Pick C and solve for R using

$$R = \frac{1}{C\,\omega o} \tag{48}$$

7. Since K and Q are dependent, compute the actual Ka of total gain implemented for all stages. The total actual gain is implemented in the design is given by

$$Ka = K1 \cdot K2 \cdot K3 \cdot K4 \ldots . \quad (49)$$

where K1, K2, K3 etc. are the actual gains used in each of the first and second order stages as given by Equation (37).

8. If the actual implemented gain Ka < Kd (the original desired gain) then an additional gain stage as shown in Figure 16 is required with a gain of

$$Kg = \frac{Kd}{Ka} = \frac{Ry}{Rx} + 1 \quad . \quad (50)$$

Pick Rx or Ry and solve for the other resistor.

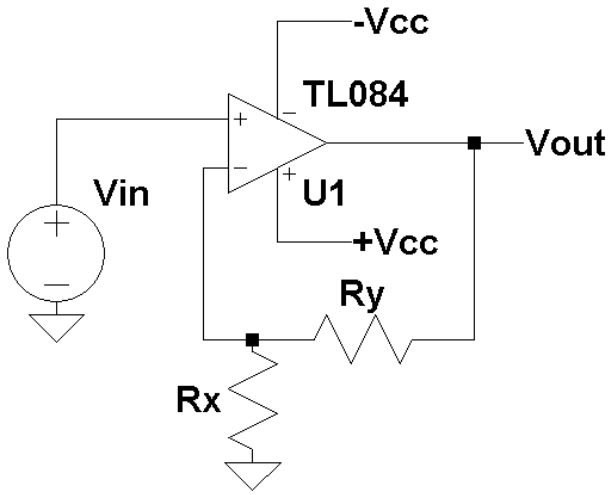


Figure 16: A non-inverting amplifier with a gain of Kg.

9. If the original desired gain Kd is less than the actual implemented gain Ka, then a buffered voltage divider network as shown in Figure 17 will be needed to reduce the total gain

$$Kg = \frac{Kd}{Ka} = \frac{Rx}{Rx + Ry} \quad . \quad (51)$$

Pick Rx or Ry and solve for the other resistor.

10. The design is now complete.
11. To design a highpass Butterworth filter, all of the steps are identically the same as for the lowpass filter except the R's and C's are interchanged and Figure 7 applies for the first order highpass filter and Figure 13 applies for the second order highpass filter.

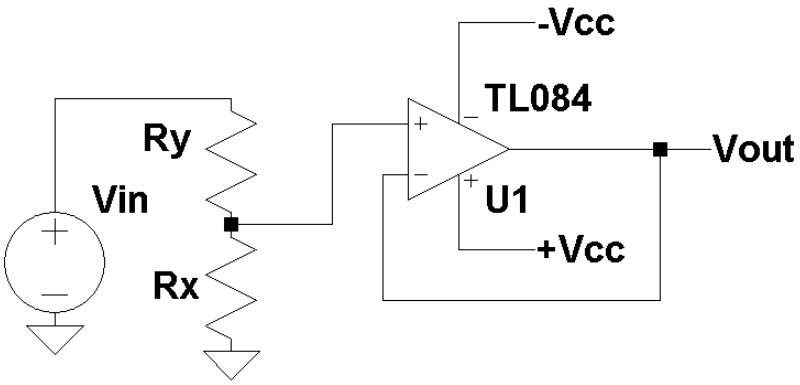


Figure 17: A buffered voltage divider.

Procedure:

General Setup:

1. Record the model and serial number of the scope, power supply, multimeter and function generator used in laboratory experiment.
2. When measuring any values make sure to measure all inputs as well as the output of the circuit. Do not rely on the values indicated on the instruments. Always measure all signal values.
3. Before turning any power on, double check the wiring to make sure that it is correct.
4. Measure all resistors that are used in the amplifier circuits using the multimeter and record these values.
5. Use all measured values to determine experimental results such as gain and cutoff frequency, or quality factor.
6. Comparing data means to calculate the percent difference between two values. For example, theoretical values versus measured values.
7. Comparing data graphically means to plot the data on the same plot to see how the data overlaps.
8. The square wave used with laboratory experiment is assumed to have a 50% duty cycle.

First order Filters:

1. Build a first order lowpass filter using the circuit given in Figure 4 with ωo = 10,000 rad / sec (minimum filter resistor should be 10kΩ).
2. Applying a 1 volt peak sine wave input with frequencies varying from 100 Hz to 100 kHz, plot its magnitude spectrum. Measure at least 3 points per decade 1X, 2X, and 5X.
3. Determine the attenuation factor in dB / Decade.
4. Apply a 1-volt peak-to-peak square wave input with a frequency of 500 Hz. Measure and plot, using an oscilloscope, the step response of this filter.
5. Repeat Step 4 for square wave frequencies of 1000, 2000, and 5000 Hz.
6. Build a first order highpass filter using the circuit given in Figure 7(a) with ωo = 10,000 rad / sec.

7. Applying a 1 volt peak sine wave input with frequencies varying from 100 Hz to 100 kHz, plot its magnitude spectrum. Measure at least 3 points per decade 1X, 2X, and 5X.
8. Determine the attenuation factor in dB / Decade.
9. Apply a 1-volt peak-to-peak square wave input with a frequency of 500 Hz. Measure and plot, using an oscilloscope, the step response of this filter.
10. Repeat Step 9 for square wave frequencies of 1000, 2000, and 5000 Hz.

Second order Filters

1. Build a second order lowpass filter using the circuit given in Figure 10 with ωo = 10,000 rad / sec with Q = 2 (minimum filter resistor should be 10kΩ).
2. Applying a 2-volt peak-to-peak sine wave input with frequencies varying from 100 Hz to 100 kHz, plot its magnitude spectrum. Measure at least 3 points per decade 1X, 2X, and 5X. What is the attenuation factor in dB / Decade?
3. Measure Vout at $\omega = \omega o$ and compare this result to $K \cdot Q$.
4. Apply a 2-volt peak-to-peak square wave input with a frequency of 500 Hz. Measure and plot, using an oscilloscope, the step response of this filter.
5. Measure the peak overshoot and compute the percent overshoot using Equation (31)
6. Repeat Steps 4 and 5 for Q = 0.5 and 5. How do these oscilloscope plots compare to Figure 12.
7. From step 6, compare the measured % overshoot to Equation (31).
8. Build a second order highpass filter using the circuit given in Figure 13 with ωo = 10,000 rad / sec with Q = 2.
9. Applying a 2-volt peak-to-peak sine wave input with frequencies varying from 100 Hz to 100 kHz, plot its magnitude spectrum. Measure at least 3 points per decade 1X, 2X, and 5X. What is the attenuation factor in dB / Decade?
10. Measure Vout at $\omega = \omega o$ and compare this result to $K \cdot Q$.
11. Apply a 2-volt peak-to-peak square wave input with a frequency of 500 Hz. Measure and plot, using an oscilloscope, the step response of this filter.
12. Repeat Step 11 for Q = 0.5 and 5. How do these oscilloscope plots compare to Figure 15.

Butterworth Filter

13. Build a fifth order Butterworth filter using the steps described in the laboratory experiment with ωo = 10,000 rad / sec and Kd = 5. The attenuation factor should be -100 dB / Decade. Make sure that the R's and C's are easily swappable (minimum filter resistor should be 10kΩ).
14. Applying a 2 volt peak-to-peak sine wave input with frequencies varying from 100 Hz to 10 kHz, plot its magnitude spectrum. Measure at least 3 points per decade 1X, 2X, and 5X.
15. Measure Vout at $\omega = \omega o$.
16. Apply a 2-volt peak-to-peak square input with a frequency of 200 Hz. Measure and plot, using an oscilloscope, the step response of this filter.
17. Compare the measure low frequency gain to the desired gain of 5.

18. Swapping the R's and the C's in the lowpass Butterworth filter design, build a 5^{th} order highpass Butterworth filter with a desired gain Kd of 5.
19. Applying a 2-volt peak-to-peak sine wave input with frequencies varying from 10 Hz to 10 kHz, plot its magnitude spectrum. Measure at least 3 points per decade 1X, 2X, and 5X.
20. Measure Vout at $\omega = \omega o$.
21. Apply a 2-volt peak-to-peak square wave input with a frequency of 200 Hz. Measure and plot, using an oscilloscope, the step response of this filter.
22. Compare the measured high frequency gain to the desired gain of 5.

Report: Please follow the procedures in this laboratory manual for writing the report for this experiment. Include in your report;

1. The equipment used model and serial number.
2. Laboratory partners
3. Date and time data was taken.
4. Your laboratory report should include the goal of the laboratory experiment.
5. The procedures.
6. The pre-laboratory results.
7. All calculations for each step.
8. All plots generated for each step.
9. All comparisons calculations.
10. For each data collection step in the procedure, there should be either data collected, a calculation performed, a waveform recorded. Please include these in the report.
11. Short summary discussing what is observed for each of the steps given in the laboratory experiment.
12. Also include what you learned.
13. Make sure to include comparisons with simulated results and actual results.
14. Include the comparison of the measure percent overshoot with Equation (31).
15. Include all time plots.
16. Include all frequency plots.
17. Include the designs steps used to design the 5^{th} order Butterworth filter. List all resistor and capacitor values used in a table.
18. How are the time and frequency domain signals related?

EXPERIMENT #7

Voltage Comparators and Schmitt Triggers

Goals:
To introduce the concepts of using an operational amplifier as a voltage comparator. The theory of voltage comparator will be presented along with the design of several comparator circuits. The Schmitt trigger comparator will be presented.

References:

Microelectronics-Circuit Analysis and Design, D. A. Neamen, McGraw-Hill, 4th Edition, 2007, ISBN: 978-0-07-252362-1.

The following link is to the Tektronix website for the user manual for the DPO 4034B oscilloscope:
http://www2.tek.com/cmswpt/madetails.lotr?ct=MA&cs=mur&ci=16272&lc=EN

Equipment:

Oscilloscope: DPO 4034B
Function Generator: AFG3022B
Triple Power supply
Capacitors available in the laboratory
Resistors available in the laboratory
Multimeter
TL084 Operational Amplifier
LM393 Comparator

Pre-laboratory:

Read this laboratory experiment carefully to become familiar with the background and the procedural steps in this experiment. Carefully read each section and become familiar with the equations for each circuit.

Using the simulation package of your choice in which you are the most familiar with: Mulitsim, Workbench or LTSpice IV simulate the various comparator circuits.

a. Download the National Semiconductor LM393 voltage comparator datasheet and become familiar with this part.
b. Using an op-amp with +Vcc set to +15 volts and -Vcc set to -15 volts, simulate the comparator circuit of Figure 3.
c. Use a 10 volts peak 500 Hz triangle waveform for the input Vin (DC offset =0 volts).
d. Plot Vout as a function of time for Vref = 1volt.
e. Determine the voltage Vin where Vout switches from +Vcc to -Vcc.

f. Repeat Steps b - e for Vref = 2 volts, 5 volts and 8 volts.
g. Using an op-amp with +Vcc set to +15 volts and -Vcc set to -15 volts, simulate the comparator circuit of Figure 4.
h. Use a 10 volts peak 500 Hz triangle waveform for the input Vin (DC offset =0 volts).
i. Plot Vout as a function of time for Vref = 1 volt.
j. Determine the voltage Vin where Vout switches from +Vcc to -Vcc.
k. Repeat Steps g - j for Vref = 2 volts, 5 volts and 8 volts.
l. Using an op-amp with +Vcc set to +15 volts and -Vcc set to -15 volts, simulate the comparator circuit of Figure 8.
m. Let R2 =10k and R1 =1k.
n. Use a 5 volts peak 500 Hz triangle waveform for the input Vin (DC offset =0 volts).
o. Determine the voltage Vin where Vout switches from +Vcc to -Vcc.
p. Plot Vout as a function of time.
q. Determine Vout max and Vout min. Replace +Vcc with Vout max and -Vcc with Vout min in Equations (22) - (25).
r. Compare the Equations (22) - (25) with Step o.
s. Using an op-amp with +Vcc set to +15 volts and -Vcc set to -15 volts, simulate the comparator circuit of Figure 12.
t. Let R2 =10k and R1 =1k.
u. Use a 5 volts peak 500 Hz triangle waveform for the input Vin (DC offset =0 volts).
v. Determine the voltage, Vin, where Vout switches from +Vcc to -Vcc.
w. Plot Vout as a function of time.
x. Determine Vout max and Vout min. Replace +Vcc with Vout max and -Vcc with Vout min in Equations (30) - (33).
y. Compare the Equations (30) - (33) with Step v.
z. Simulate the pulse width modulator circuit of Figure 14.
aa. Use a 0 to 10 volt 1000 Hz sawtooth waveform. Vary Vin from 0 to 10 volts (0, 1, 2, 5, 8, and 10 volts) and measure T1 the time Vout = +Vcc.
bb. Plot T1 versus Vin.
cc. Compare Step bb to Equation (36) with T=0.001 sec and K 10 volts.

Discussion:

Voltage comparison is commonly required in electronic circuit design when there is a need to compare two input voltages. Figure 1 shows the circuit diagram for a voltage comparator. It is the same diagram as an operational amplifier and in many cases an operational amplifier can be used as a voltage comparator. When an operation amplifier is used as a comparator, care must be taken so that the input does not exceed its common mode input range.

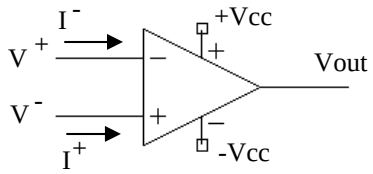


Figure 1: A circuit diagram of a typical voltage comparator

Voltage comparators require either a dual power supply like an op-amp or a single supply. The type of power supply that is required depends on the voltage range of the voltage comparator's output. The output voltage Vout for a comparator is

$$\text{Vout} = \begin{cases} \text{Va} & \text{for } V^+ > V^- \\ \text{Vb} & \text{for } V^+ < V^- \end{cases} \qquad (1)$$

Figure 2 gives a diagram of Vout versus Vin. The output has two possible states. State 1: for $V^+ > V^-$ and the second state for $V+ < V^-$. As with an op-amp the current flowing in the two inputs I^+ and I^- can be assumed to be zero.

When an op-amp is used as a voltage comparator, the open loop equation of the op-amp (from laboratory Experiment #1) is

$$\text{Vout} = \text{Aod}\,(V^+ - V^-) \quad , \qquad (2)$$

where Aod is the open loop gain of the op-amp. Since Aod is very large, with

$$(V^+ - V^-) = \frac{\text{Vout}}{\text{Aod}} \qquad (3)$$

and with Vout bounded between the two powers supply voltages:

$$-\text{Vcc} \le \text{Vout} \le +\text{Vcc} \quad , \qquad (4)$$

if $V^+ > V^-$ then Vout must be equal +Vcc, the positive output rail of the op-amp. But, if $V^+ < V^-$, then Vout = -Vcc, the negative rail of the op-amp. As mentioned earlier V^+ and V^- must be maintained within the allowed common mode input of the op-amp.

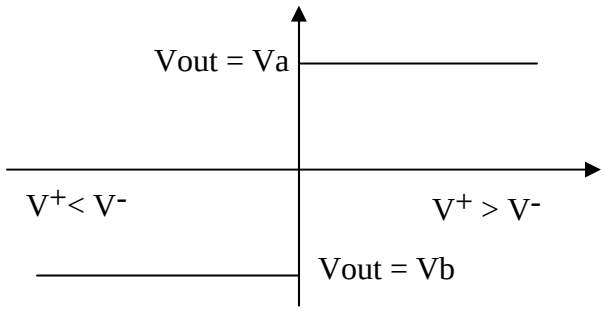


Figure 2: Vout versus Vin for a voltage comparator.

Figure 3 is a common comparator circuit with Vin connected to V+ with a dual power supply for the comparator of +Vcc and -Vcc. Using the voltage divider equation, V- is given by

$$V^- = +Vcc \frac{R1}{R1 + R2} \tag{5}$$

and

$$Vout = \begin{cases} +Vcc & \text{for } Vin > +Vcc \dfrac{R1}{R1 + R2} \\ -Vcc & \text{for } Vin < +Vcc \dfrac{R1}{R1 + R2} \end{cases} \tag{6}$$

Figure 4 is a graph of Vout versus Vin, showing the transition of Vout from +Vcc to - Vcc when

$$Vin = +Vcc \frac{R1}{R1 + R2} \quad . \tag{7}$$

Since the voltage divider circuit of Figure 3 does nothing more than produce a reference voltage that sets the value of Vin that will result in Vout changing states, this voltage divider circuit can be replaced by the label Vref, which can be called the *reference voltage*.

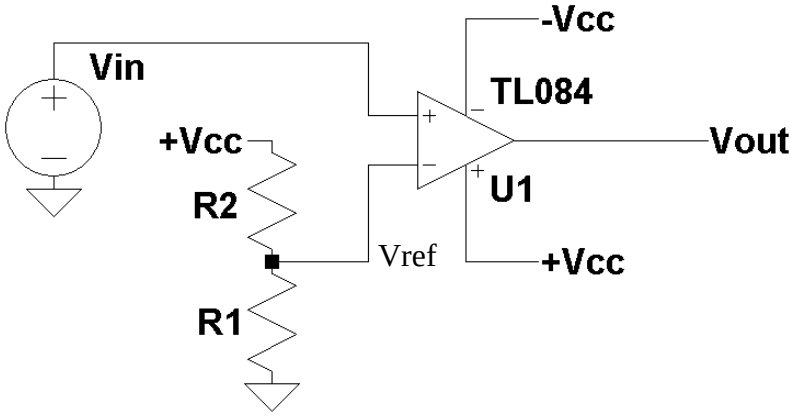


Figure 3: A simple comparator circuit.

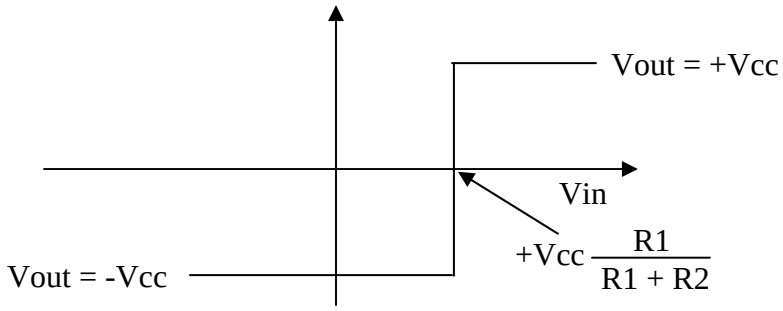


Figure 4: Vout versus Vin for the comparator circuit of Figure 3.

Changing the inputs to the voltage comparator circuit given in Figure 3 as shown in Figure 5 produces the output of

$$\text{Vout} = \begin{cases} \text{Vout} = +\text{Vcc} & \text{for Vin} < \text{Vref} \\ \text{Vout} = 0 & \text{for Vin} > \text{Vref} \end{cases} \tag{8}$$

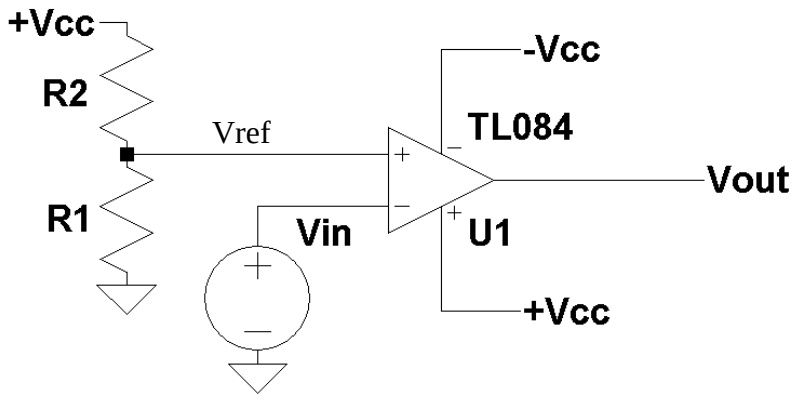


Figure 5: Another comparator circuit.

Figure 6 gives its corresponding plot of Vout versus Vin. The difference in the two comparator circuits of Figures 3 and 5 is the polarity of the output with respect to the input Vin. For figure 3, Vout = + Vcc for

$$\text{Vin} > +\text{Vcc}\,\frac{\text{R1}}{\text{R1} + \text{R2}} \quad , \tag{9}$$

while for the comparator circuit for Figure 5, Vout = + Vcc for

$$\text{Vin} < +\text{Vcc}\,\frac{\text{R1}}{\text{R1} + \text{R2}} \quad . \tag{10}$$

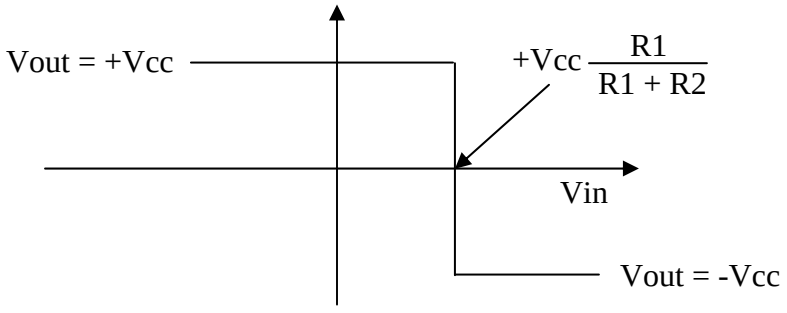


Figure 6: Vout versus Vin for the comparator circuit of Figure 5.

Figure 7 gives Vout as a function of time for the comparator circuit of Figure 3. During the time Vin > Vref, Vout = +Vcc else Vout = -Vcc.

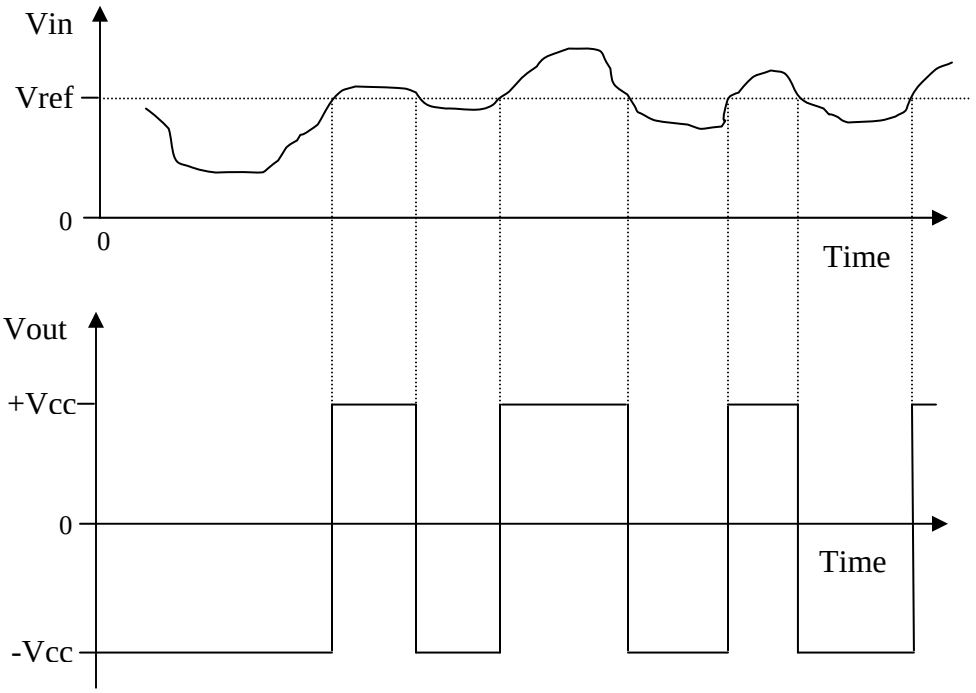
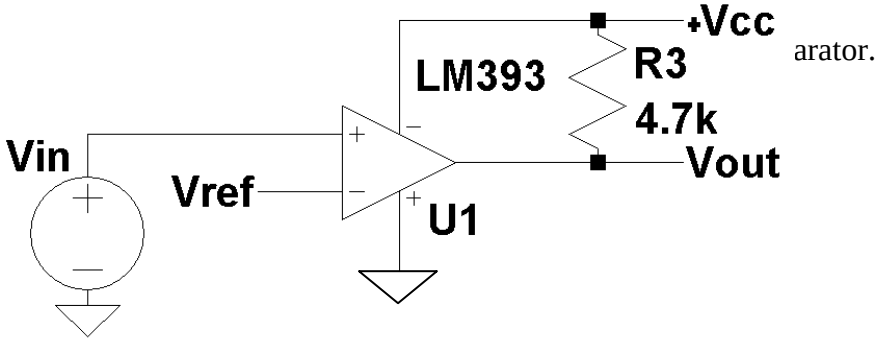


Figure 7: Vout as a function of time for the comparator circuit of Figure 3.

If the LM393 comparator as shown in Figure 8, is used to implement the comparator circuit given in Figure 3, then

$$\text{Vout} = \begin{cases} +\text{Vcc} & \text{for Vin} > \text{Vref} \\ 0 & \text{for Vin} < \text{Vref} \end{cases}, \tag{11}$$

where the output voltage Vout is defined as Va = +Vcc and Vb = 0. The output of the LM393 comparator is an open collector transistor and it needs a pull-up resistor (typically 2k to 4k). The only requirement in picking the value of the pull-up resistor is the maximum current for the output transistor can not exceed 10 milliamps. Figure 9 gives the output as a function time for the comparator circuit for Figure 3 using the LM393 comparator.



arator.

Figure 8: A simple comparator circuit using the LM393 comparator.

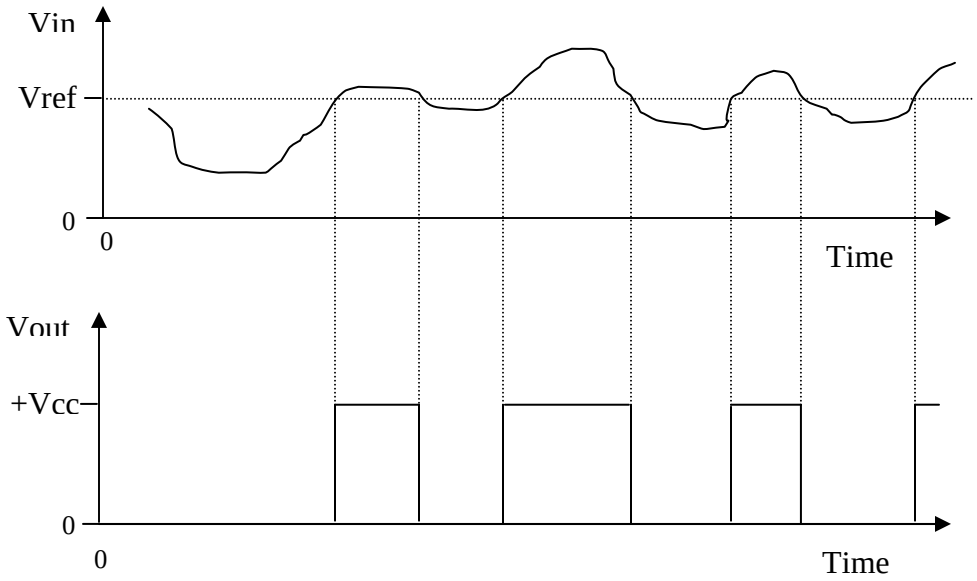


Figure 9: Vout as a function of time for the comparator circuit of Figure 3 using an LM393 comparator.

Consider the comparator circuit given in Figure 10. Starting with

$$\text{Vout} = \begin{cases} +\text{Vcc for } V^+ > V^- \\ -\text{Vcc for } V^+ < V^- \end{cases} . \qquad (12)$$

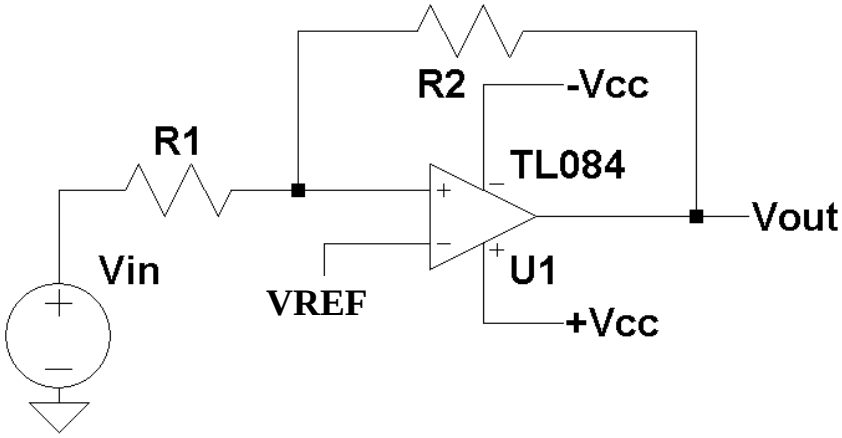


Figure 10: A comparator circuit with hysteresis (Schmitt Trigger).

But V^- = Vref,

$$\text{Vout} = \begin{cases} +\text{Vcc for } V^+ > \text{Vref} \\ -\text{Vcc for } V^+ < \text{Vref} \end{cases} . \qquad (13)$$

Solving for V^+ gives

$$V+ = Vin + R1\frac{Vout - Vin}{R1 + R2} = \frac{R1 \cdot Vout + R2 \cdot Vin}{R1 + R2} \quad . \tag{14}$$

Substituting Equation (14) into Equation (13) for the case when Vout = +Vcc yields

$$Vout = +Vcc \qquad \text{when} \quad \frac{R1 \cdot Vout + R2 \cdot Vin}{R1 + R2} > Vref \quad . \tag{15}$$

Solving Equation (15) for Vin gives

$$Vout = +Vcc \qquad \text{when} \quad Vin > Vref\left(\frac{R1}{R2} + 1\right) - Vout\frac{R1}{R2} \quad . \tag{16}$$

or substituting for Vout = +Vcc

$$Vout = +Vcc \qquad \text{when} \quad Vin > Vref\left(\frac{R1}{R2} + 1\right) - Vcc\frac{R1}{R2} \quad . \tag{17}$$

Using the same approach for when Vout = -Vcc gives

$$Vout = -Vcc \qquad \text{when} \quad \frac{R1 \cdot Vout + R2 \cdot Vin}{R1 + R2} < Vref \quad . \tag{18}$$

Substituting Vout with -Vcc and solving for Vin gives

$$Vout = -Vcc \qquad \text{when} \quad Vin < Vref\left(\frac{R1}{R2} + 1\right) + Vcc\frac{R1}{R2} \quad . \tag{19}$$

If Vout = +Vcc then by Equation (17) Vout switches to -Vcc when

$$Vout\ (+Vcc \rightarrow -Vcc) \qquad \text{when} \quad Vin < Vref\left(\frac{R1}{R2} + 1\right) - Vcc\frac{R1}{R2} \quad . \tag{20}$$

and if Vout = -Vcc then by Equation (19) Vout switches to +Vcc when

$$Vout\ (-Vcc \rightarrow +Vcc) \qquad \text{when} \quad Vin > Vref\left(\frac{R1}{R2} + 1\right) + Vcc\frac{R1}{R2} \quad . \tag{21}$$

For the special case when Vref = 0 Equations (17) and (19) reduce to

$$Vout = +Vcc \qquad \text{when} \quad Vin > -Vcc\frac{R1}{R2} \quad . \tag{22}$$

and

$$\text{Vout} = -\text{Vcc} \qquad \text{when Vin} < +\text{Vcc}\,\frac{R1}{R2}\ . \tag{23}$$

If Vout = +Vcc, then by Equation (22) Vout switches to -Vcc when

$$\text{Vout } (+\text{Vcc} \rightarrow -\text{Vcc}) \qquad \text{when Vin} < -\text{Vcc}\,\frac{R1}{R2}\ . \tag{24}$$

and if Vout = -Vcc then by Equation (23) Vout switches to +Vcc when

$$\text{Vout } (-\text{Vcc} \rightarrow +\text{Vcc}) \qquad \text{when Vin} > +\text{Vcc}\,\frac{R1}{R2}\ . \tag{25}$$

Figure 11 gives a plot of Vout versus Vin for the case when Vref = 0 volts. Note the hysteresis that exist between transitioning Vout from -Vcc to +Vcc and from +Vcc to -Vcc of

$$\text{Hysteresis value} = \text{Vcc}\,\frac{2\cdot R1}{R2}\ . \tag{26}$$

This type of comparator circuit with hysteresis is commonly called a Schmitt Trigger.

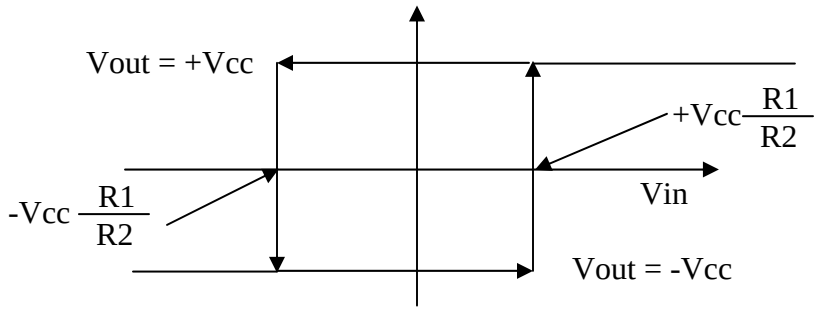


Figure 11: Vout versus Vin for the comparator circuit of Figure 8.

Figure12 gives another commonly used Schmitt trigger circuit. Using the same approach in solving the Schmitt trigger circuit given in Figure 8

Consider the comparator circuit given in Figure 12. Starting with

$$\text{Vout} = \begin{cases} +\text{Vcc for } V^+ > V^- \\ -\text{Vcc for } V^+ < V^- \end{cases}\ . \tag{27}$$

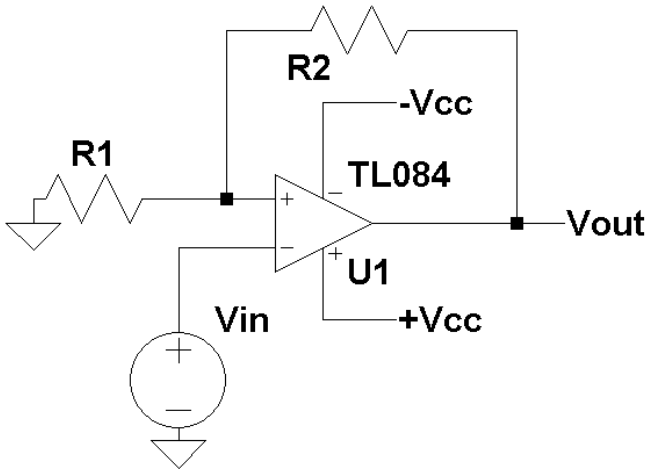


Figure 12: A comparator circuit with hysteresis (Schmitt Trigger).

But V^- = Vin,

$$\text{Vout} = \begin{cases} +\text{Vcc for } V^+ > \text{Vin} \\ -\text{Vcc for } V^+ < \text{Vin} \end{cases} . \tag{28}$$

Solving for V^+ gives

$$\text{V+} = \text{Vout}\,\frac{\text{R1}}{\text{R1} + \text{R2}} . \tag{29}$$

Substituting Equation (29) into Equation (28) for the case where Vout = +Vcc

$$\text{Vout} = +\text{Vcc} \qquad \text{when Vin} < +\text{Vcc}\,\frac{\text{R1}}{\text{R1} + \text{R2}} . \tag{30}$$

For the case when Vout = -Vcc, Vout becomes

$$\text{Vout} = -\text{Vcc} \qquad \text{when Vin} > -\text{Vcc}\,\frac{\text{R1}}{\text{R1} + \text{R2}} . \tag{31}$$

If Vout = +Vcc then by Equation (30) Vout switches to -Vcc when

$$\text{Vout } (+\text{Vcc} \rightarrow -\text{Vcc}) \qquad \text{when Vin} > +\text{Vcc}\,\frac{\text{R1}}{\text{R1} + \text{R2}} . \tag{32}$$

and if Vout = -Vcc then by Equation (31) Vout switches to +Vcc when

$$\text{Vout } (-\text{Vcc} \rightarrow +\text{Vcc}) \qquad \text{when Vin} < -\text{Vcc}\,\frac{\text{R1}}{\text{R1} + \text{R2}} . \tag{33}$$

Figure 13 gives Vout versus Vin for the Schmitt trigger circuit given in Figure 12.

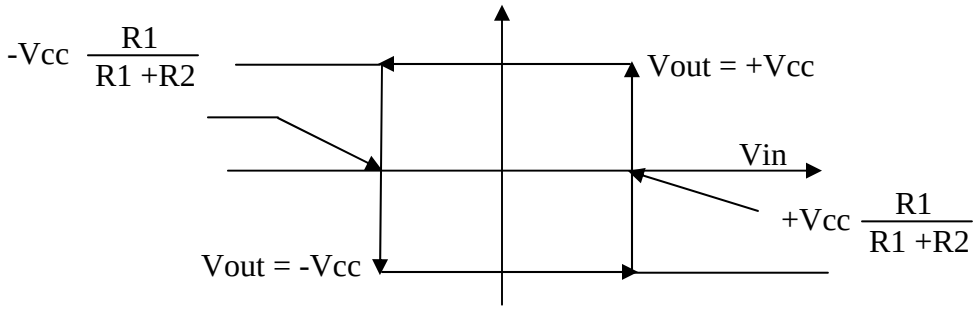


Figure 13: Vout versus Vin for the Schmitt Trigger circuit of Figure 12.

As illustrated in laboratory experiment #4, a comparator can be used as a pulse width modulator as shown in Figure 14. Defining Vout as

$$\text{Vout} = \begin{cases} +\text{Vcc} & \text{for Vin} > \text{Vx} \\ 0 & \text{for Vin} < \text{Vx} \end{cases}, \qquad (34)$$

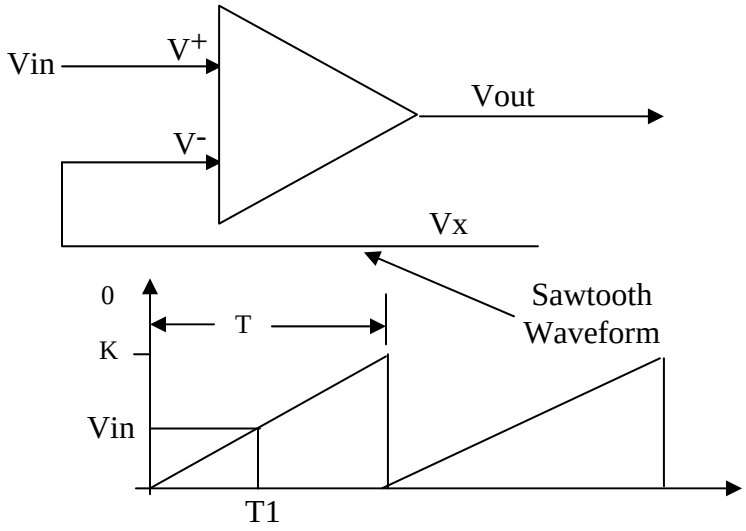


Figure 14. A block diagram of a pulse width modulator.

But, the sawtooth waveform over one period T can written as

$$\text{Vx} = \text{K}\frac{\text{t}}{\text{T}} \qquad \text{for } 0 \le \text{t} < \text{T} \qquad (35)$$

As long as Vx < Vin Vout will be equal to +Vcc. The point in time (T1) when Vx > Vin, Vout goes to zero as shown in Figure 15. Solving Equation (35) for t and setting Vx = Vin give the time T1 as

$$T1 = T\frac{Vin}{K} \qquad \text{for } 0 \le Vin < K \quad . \qquad (36)$$

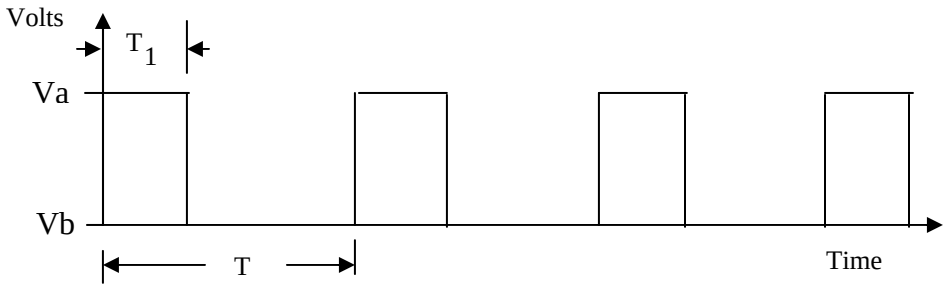


Figure 15: An example Vout from the pulse width modulator given in Figure 12.

Procedure:

General Setup:

1. Record the model and serial number of the scope, power supply, multimeter and function generator used in laboratory experiment.
2. Download the datasheet for the LM393 comparator. This will be needed to obtain the pin-out of the comparator. When comparing datasheet data values to experimental data use the typical values in the datasheet if given.
3. When measuring any values make sure to measure all inputs as well as the output of the circuit. Do not rely on the values indicated on the instruments. Always measure all signal values.
4. Before turning any power on double check the wiring to make sure that it is correct.
5. Measure all resistors that are used in the amplifier circuits using the multimeter and record these values.
6. Use all measured values to determine experimental results such as gain and current.
7. Comparing data means to calculate the percent difference between two values. For example, theoretical values versus measured values.
8. Comparing data graphically means to plot the data on the same plot to see how the data overlaps.

Comparator Circuits

1. Download the National Semiconductor LM393 voltage comparator datasheet and become familiar with this part.
2. Using an op-amp with +Vcc set to +15 volts and -Vcc set to -15 volts, build the comparator circuit of Figure 3.
3. Use a 20 volt peak-to-peak 500 Hz triangle waveform for the input Vin (DC offset =0 volts).
4. Plot Vout as a function of time for Vref = 1volt using an oscilloscope.
5. Determine the voltage Vin where Vout switches from +Vcc to -Vcc.
6. Repeat Steps 3 - 5 for Vref = 2 volts and 8 volts.
7. Using an op-amp with +Vcc set to +15 volts and -Vcc set to -15 volts, build

the comparator circuit of Figure 5.

8. Use a 20 volt peak-to-peak 500 Hz triangle waveform for the input Vin (DC offset =0 volts).
9. Plot Vout as a function of time for Vref = 1volt using an oscilloscope.
10. Determine the voltage Vin where Vout switches from +Vcc to -Vcc.
11. Repeat Steps 8 - 10 for Vref = 2 volts and 8 volts.
12. Using an op-amp with +Vcc set to +15 volts and -Vcc set to -15 volts, build the comparator circuit of Figure 10.
13. Let R2 =10k and R1 =1k.
14. Use a 10 volt peak-to-peak 500 Hz triangle waveform for the input Vin (DC offset =0 volts).
15. Determine the voltage Vin where Vout switches from +Vcc to -Vcc.
16. Plot Vout as a function of time using an oscilloscope.
17. Determine Vout max and Vout min from the oscilloscope traces. Replace +Vcc with Vout max and -Vcc with Vout min in Equations (22) - (25).
18. Compare the Equations (22) - (25) with Step 15.
19. Using an op-amp with +Vcc set to +15 volts and -Vcc set to -15 volts, build the comparator circuit of Figure 12.
20. Let R2 =10k and R1 =1k.
21. Use a 10 volt peak-to-peak 500 Hz triangle waveform for the input Vin (DC offset =0 volts).
22. Determine the voltage Vin where Vout switches from +Vcc to -Vcc.
23. Plot Vout as a function of time using an oscilloscope.
24. Determine Vout max and Vout min from the oscilloscope traces. Replace +Vcc with Vout max and -Vcc with Vout min in Equations (30) - (33).
25. Compare the Equations (30) - (33) with Step 22.
26. Repeat steps 2-5 and steps 7-10 using the LM393 comparator with around a 2k pull-up resistor.
27. Build the pulse width modulator circuit of Figure 14.
28. Use a 0 to 10 volt 1000 Hz sawtooth waveform. Vary Vin from 0 to 10 volts (0, 2, 4, 8, and 10 volts) and measure T1 the time Vout = +Vcc.
29. Plot T1 versus Vin.
30. Compare Step 29 to Equation (36) with T=0.001 sec and K 10 volts.

Report: Please follow the procedures in this laboratory manual for writing the report for this experiment. Include in your report:

1. The equipment used model and serial number.
2. Laboratory partners
3. Date and time data was taken.
4. Your laboratory report should include the goal of the laboratory experiment.
5. The procedures.
6. The pre-laboratory results.
7. All calculations for each step.
8. All plots generated for each step.
9. All comparisons calculations.

10. For each data collection step in the procedure, there should be either data collected, a calculation performed, a waveform recorded. Please include these in the report.
11. Short summary discussing what is observed for each of the steps given in the laboratory experiment.
12. Also include what you learned.

EXPERIMENT #8

Oscillators and Waveform Generators

Goals:
To introduce the concepts of using an operational amplifier as an oscillator to produce an output waveform. The Schmitt trigger comparator will be used to produce a square wave and a triangle waveform.

References:

Microelectronics-Circuit Analysis and Design, D. A. Neamen, McGraw-Hill, 4th Edition, 2007, ISBN: 978-0-07-252362-1.

The following link is to the Tektronix website for the user manual for the DPO 4034B oscilloscope:
http://www2.tek.com/cmswpt/madetails.lotr?ct=MA&cs=mur&ci=16272&lc=EN

Equipment:

Oscilloscope: DPO 4034B
Function Generator: AFG3022B
Triple Power supply
Capacitors available in the laboratory
Resistors available in the laboratory (use a minimum of 1k resistors)
Multimeter
TL084 Operational Amplifier

Pre-laboratory:

Read this laboratory experiment carefully to become familiar with the background and the procedural steps in this experiment. Carefully read each section and become familiar with the equations for each circuit.

Using the simulation package of your choice in which you are the most familiar with: Mulitsim, Workbench or LTSpice IV simulate the various oscillator and waveform generator circuits.

a. Using an op-amp with +Vcc set to +15 volts and -Vcc set to -15 volts, design and simulate the phase shift oscillator circuit of Figure 1. Set ωo = 5,773 rad / sec. Adjust R2 until oscillation occurs (somewhere above $8 \cdot R$). Make sure to run the simulation for a long enough time.
b. From the output waveform determine the frequency of oscillation and the peak-to-peak value.
c. Increase R2 to $15 \cdot R$ and repeat step b. Discuss the difference observed in-between steps b and c.

d. Using an op-amp with +Vcc set to +15 volts and -Vcc set to -15 volts, design and simulate the Wien-bridge oscillator circuit of Figure 3. Set ωo = 10,000 rad / sec. Adjust R2 until oscillation occurs (somewhere above 2 · R1). Make sure to run the simulation for a long enough time.
e. From the output waveform determine the frequency of oscillation and the peak-to-peak value.
f. Increase R2 to 8 · R1 and repeat step e. Discus the difference observed in between steps e and f.
g. Using an op-amp with +Vcc set to +15 volts and -Vcc set to -15 volts, design and simulate the Schmitt trigger oscillator circuit of Figure 5. Set fo = 1000 Hz. Make sure to run the simulation for a long enough time.
h. Obtain waveforms for Vout, V-, and V+. Determine the frequency of oscillation and the peak-to-peak value of Vout.
i. Using an op-amp with +Vcc set to +15 volts and -Vcc set to -15 volts, design and simulate the triangle-square wave waveform generator circuit of Figure 7. Set fo = 1000 Hz. Make sure to run the simulation for a long enough time.
j. Obtain waveforms for Vout and Vx. Determine the frequency of oscillation and the peak-to-peak value of Vout.

Discussion:

Oscillators and waveform generators are commonly used to generate sine wave, triangle wave and square wave signals used as input sources to various types of electronic circuits. Figure 1 shows the circuit diagram for a Phase Shift Oscillator Depending on R2 this oscillator can produce either a sine wave or square wave output. To analyze this circuit the feedback loop is opened and its transfer function is found from its input, all the way back, to its output.

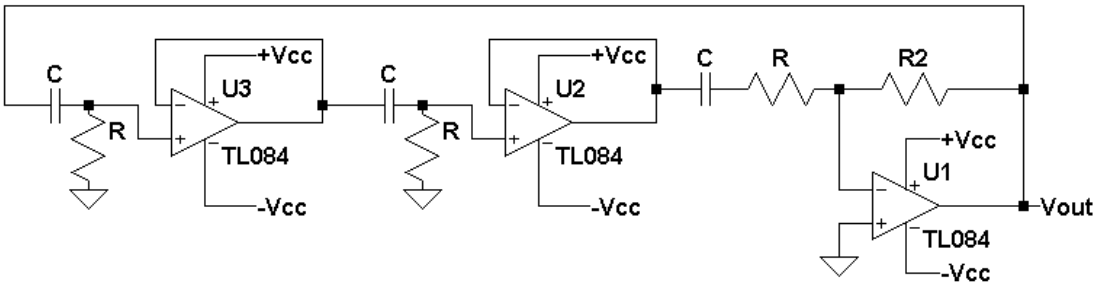


Figure 1: A circuit diagram for a phase shift oscillator.

Figure 2 shows the feedback loop open at point A. The goal is to find the output Y as a function of the input X. Starting at X, the transfer function from X to X1 is

$$\frac{X1(s)}{X(s)} = \frac{RCs}{RCs + 1} \quad . \qquad (1)$$

Since the next stage (U2) is identically the same as the fist stage (U3), the transfer function from X2 to X1 is

$$\frac{X2(s)}{X1(s)} = \frac{RCs}{RCs + 1} \quad . \tag{2}$$

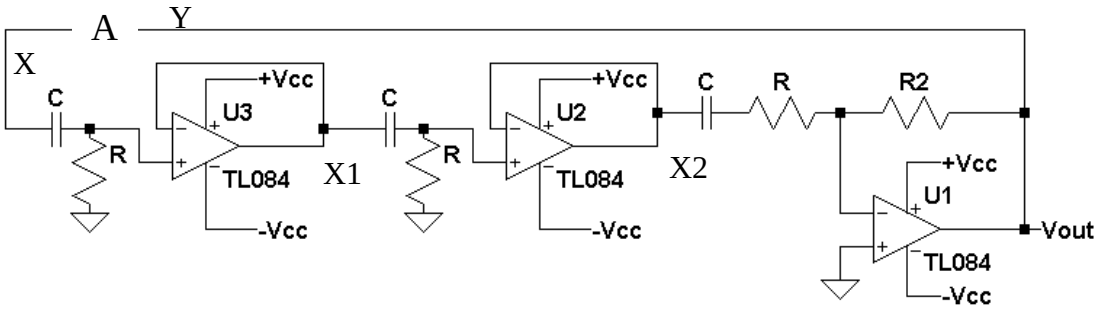


Figure 2: The phase shift oscillator with its loop feedback open at point A.

The transfer function for the final stage (U1) is given as

$$\frac{Y(s)}{X2(s)} = \frac{-R2}{R + \frac{1}{sC}} = \frac{-R2\ Cs}{RCs + 1} \quad . \tag{3}$$

The loop feedback is then given as

$$\frac{Y(s)}{X(s)} = \frac{X1(s)}{X(s)} \frac{X2(s)}{X1(s)} \frac{Y(s)}{X2(s)} \quad . \tag{4}$$

Combine Equations (1), (2) and (3) together in Equation (4) gives the total loop feedback transfer function of

$$\frac{Y(s)}{X(s)} = \frac{RCs}{RCs + 1} \frac{RCs}{RCs + 1} \frac{-R2\ Cs}{RCs + 1} \tag{5}$$

or

$$\frac{Y(s)}{X(s)} = \frac{-R2\ R^2C^3s^3}{(RCs + 1)^3} = \frac{-R2}{R}\left(\frac{RCs}{RCs + 1}\right)^3 \quad . \tag{6}$$

Substituting jω for s gives

$$\frac{Y(j\omega)}{X(j\omega)} = \frac{-R2}{R}\left(\frac{RCj\omega}{RCj\omega + 1}\right)^3 \quad . \tag{6}$$

For this circuit to oscillate, the feedback must be positive feedback with a magnitude of 1 and a feedback phase of zero degrees:

$$\left| \frac{Y(j\omega)}{X1(j\omega)} \right| = 1 \qquad (8)$$

and

$$\mathrm{Arg}\left(\frac{Y(j\omega)}{X1(j\omega)} \right) = 0° \quad . \qquad (9)$$

The criteria given in Equations (8) and (9) are known as the Barkhausen criteria. Expanding Equation (6) gives

$$\frac{Y(j\omega)}{X(j\omega)} = \frac{-R2}{R} \frac{RCj\omega\,[RC\omega]^2}{[1 - 3(\omega RC)^2] + RCj\omega[3 - (RC\omega)^2]} \quad . \qquad (10)$$

Since Equation (8) is real and contains no imaginary terms, to satisfy this criteria Equation (10) must also be real. This occurs when

$$[1 - 3(\omega RC)^2] = 0 \quad . \qquad (11)$$

Solving Equation (11) for ω gives

$$\omega = \frac{1}{\sqrt{3}RC} = \omega o \quad . \qquad (12)$$

This is the frequency of oscillation and will be called ωo.

At ωo, Equation (10) reduces to

$$\frac{Y(j\omega o)}{X(j\omega o)} = \frac{-R2}{R} \frac{-RCj\omega o\,[RC\omega o]^2}{RCj\omega o[3 - (RC\omega o)^2]} \quad , \qquad (13)$$

but by Equation (12)

$$\frac{Y(j\omega o)}{X(j\omega o)} = \frac{R2}{R} \frac{\sqrt{1/3}\,1/3}{\sqrt{1/3}(3 - 1/3)} = \frac{R2}{R}\frac{1}{8} \qquad (14)$$

Before Equation (14) can be solved, another look at the Barkhausen criteria is needed. The Barkhausen criteria state that a magnitude of 1 and 0° of phase are required for oscillation. This is another way of stating that

$$\frac{Y(j\omega o)}{X(j\omega o)} = 1 \rightarrow \left|\frac{Y(j\omega o)}{X(j\omega o)}\right| = 1 \text{ and } \arg\left(\frac{Y(j\omega o)}{X(j\omega o)}\right) = 0° \quad . \tag{15}$$

Substituting Equation (15) into Equation (14) and solving for R2 gives

$$R2 = 8 \cdot R \quad . \tag{16}$$

Equation (16) defines the minimum value that R2 can be to obtain oscillation based on ideal conditions. Equation (16) is for the ideal case assuming an ideal op-amp. Typically, R2 is selected such that R2 set to be slightly greater than 8 · R to guarantee oscillation. R2 is usually implemented using a variable resistor and is increased in value to the point where oscillation begins. Equations (12) and (16) are the two design equations that are needed to design and build a phase shift oscillator. Usually C is chosen and Equation (12) is used to find R. Then Equation (16) is used to find the minimum value for R2.

Another common oscillator is the Wien-Bridge Oscillator, shown in Figure 3, which can be used to generate sine or square waves, depending on the gain. The same approach will be used to analyze this oscillator that was used for the phase shift oscillator. Figure 4 shows Wien-bridge with the loop feedback opened.

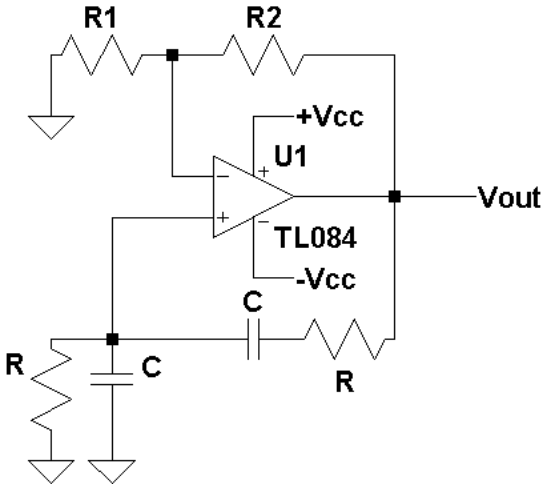


Figure 3: The Wien-bridge oscillator.

Point Y can be written in terms of X1 as

$$\frac{Y(s)}{X1(s)} = \frac{R2}{R1} + 1 \tag{17}$$

and X1 in terms of X as

$$\frac{X1(s)}{X(s)} = \frac{\frac{R}{RCs + 1}}{\frac{R}{RCs + 1} + \frac{1 + RCs}{Cs}} = \frac{RCs}{(RCs)^2 + 3RCs + 1} \quad . \tag{18}$$

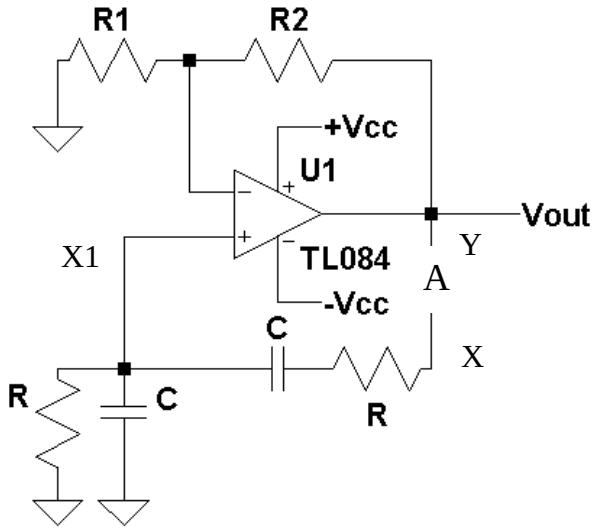


Figure 4: The Wien-bridge oscillator with a loop feedback opened at A.

Combining Equations (17) and (18) gives the transfer function of the loop feedback as

$$\frac{Y(s)}{X(s)} = \left(\frac{R2}{R1} + 1\right) \frac{RCs}{(RCs)^2 + 3RCs + 1} \quad . \tag{19}$$

Substituting jω for s gives

$$\frac{Y(j\omega)}{X(j\omega)} = \left(\frac{R2}{R1} + 1\right) \frac{RCj\omega}{(RCj\omega)^2 + 3RCj\omega + 1} = \left(\frac{R2}{R1} + 1\right) \frac{RCj\omega}{1 - (RC\omega)^2 + 3RCj\omega} . \tag{20}$$

Since Equation (20) must be real with no imaginary terms to satisfy Equations (8) and (9), the Barkhausen criteria:

$$1 - (RC\omega)^2 = 0 \tag{21}$$

or

$$\omega = \frac{1}{RC} = \omega o \quad , \tag{22}$$

where, ωo is the frequency of oscillation. Substituting ω =ωo into Equation (20) gives

$$\frac{Y(\omega o)}{X1(\omega o)} = \frac{1}{3}\left(\frac{R2}{R1} + 1\right) \quad . \tag{24}$$

Since to satisfy the Barkhausen criteria, the phase of Equation must be 0° and the magnitude is 1 or

$$\frac{1}{3}\left(\frac{R2}{R1} + 1\right) = 1 \quad . \tag{23}$$

Solving for R2 gives

$$R2 = 2 \cdot R1 \quad . \tag{25}$$

Equation (25) defines the minimum value that R2 can be to obtain oscillation based on ideal conditions. Equation (22) is for the ideal case assuming an ideal op-amp. Typically, R2 is selected such that R2 set to be slightly greater than 2 · R1 to guarantee oscillation. R2 is usually implemented using a variable resistor and is increased in value to the point where oscillation begins. Equations (22) and (25) are the two design equations that are needed to design and build a phase shift oscillator. Usually C is chosen and Equation (22) is used to find R. R1 is chosen and then Equation (25) is used to find the minimum value of R2.

Another type of oscillator or waveform generator is one that generates a square wave output using a Schmitt trigger and an RC network. Figure 5 gives the circuit diagram for a Schmitt trigger oscillator. The two inputs to the op-amp can be written in terms of Vout as

$$V^+ = \frac{R1}{R1 + R2} Vout \tag{26}$$

and

$$V^- = \frac{1}{RCs + 1} Vout \tag{27}$$

Resistors R1 and R2 form the positive feedback that is needed for a Schmitt trigger. From laboratory experiment #7, for

$$Vout = +Vcc \qquad \text{when } V^- < +Vcc \frac{R1}{R1 + R2} \quad . \tag{28}$$

For the case when Vout = -Vcc

$$\text{Vout} = -\text{Vcc} \qquad \text{when } V^- > -\text{Vcc}\,\frac{R1}{R1 + R2}\ . \tag{29}$$

If Vout = +Vcc, then by Equation (28) Vout switches to -Vcc when

$$\text{Vout } (+\text{Vcc} \rightarrow -\text{Vcc}) \qquad \text{when } V^- > +\text{Vcc}\,\frac{R1}{R1 + R2}\ . \tag{30}$$

and if Vout = -Vcc then by Equation (29) Vout switches to +Vcc when

$$\text{Vout } (-\text{Vcc} \rightarrow +\text{Vcc}) \qquad \text{when } V^- < -\text{Vcc}\,\frac{R1}{R1 + R2}\ . \tag{31}$$

Equations (28) - (31) assume that Vout is a rail to rail op-amp with Vout(max) = +Vcc and Vout(min) = -Vcc. If the maximum and minimum Vout is any other values than +Vcc is replaced with Vout(max) and -Vcc is replaced with Vout(min). If R1 = R2, then Equation (28) - (31) reduce to reduces to V+(s) = 1/2 Vout or +Vcc / 2 or -Vcc / 2.

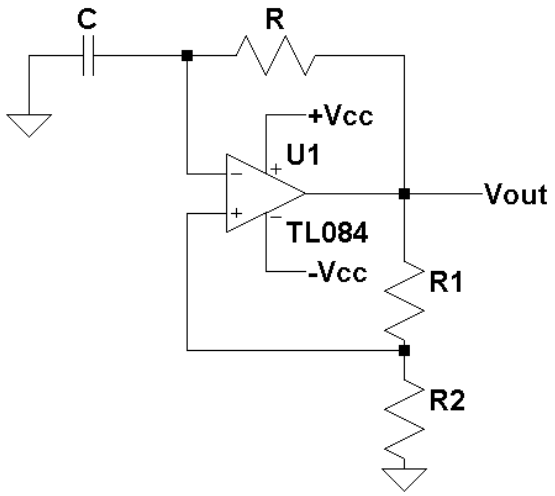


Figure 5: The circuit diagram for a Schmitt trigger oscillator.

Since the output of this circuit is a square wave, this looks like a step input to the RC network that is connected from Vout to V^- terminal of the op-amp and is given by

$$V^-(t) = Vf + (Vi - Vf)\cdot e^{-t/RC}\ , \tag{32}$$

where Vf is the final voltage the capacitor charges to and Vi is the initial voltage on the capacitor at the time the step input occurred.

Assume R1 = R2 and the Vout = -Vcc and Vout just changes states to +Vcc, and since Vout has been at -Vcc, the initial voltage on the capacitor will be -Vcc / 2

(V^+ = Vout / 2). At this point the capacitor starts charging to +Vcc and Equation (32) becomes

$$V^-(t) = +Vcc + (-Vcc / 2 - Vcc)\, e^{-t/RC} \quad = +Vcc - 3 / 2 \cdot Vcc \cdot e^{-t/RC}, \qquad (33)$$

The capacitor continues to charge to +Vcc until $V^- > V^+ = +Vcc / 2$. At this point Vout switches states, going to -Vcc. Setting $V^-(t) = Vcc / 2$ and solving for t gives the total time T1 it takes the capacitor to charge to +Vcc / 2

$$T1 = RC \cdot \ln(3) = 1.0986 \cdot RC \qquad . \qquad (34)$$

At this point Vout switches back from +Vcc to - Vcc, the capacitor starts to charge to -Vcc with an initial voltage on the capacitor of +Vcc / 2. Substituting these values into Equation (32) gives

$$V^-(t) = -Vcc + (+Vcc / 2 + +Vcc)\, e^{-t/RC} \quad = -Vcc + 3 / 2 \cdot Vcc \cdot e^{-t/RC}, \qquad (33)$$

The capacitor continues to charge to -Vcc until $V^- < V^+ = -Vcc / 2$. At this point Vout switches states, going to +Vcc again. Setting $V^-(t) = Vcc / 2$ and solving for t gives the total time T2 it takes the capacitor to charge to -Vcc / 2

$$T2 = RC \cdot \ln(3) = 1.0986 \cdot RC \qquad . \qquad 34)$$

The process of charging the capacitor to +Vcc / 2 to -Vcc / 2 produces a square wave with a period Tp

$$Tp = T1 + T2 = RC \cdot 2 \cdot \ln(3) \quad . \qquad (35)$$

The frequency of oscillation is then defined as

$$f = \frac{1}{Tp} = \frac{1}{RC \cdot 2 \cdot \ln(3)} = \frac{0.455}{RC} \quad . \qquad (36)$$

Figure 5 gives a sample output showing Vout, V^- and V^+ as a function of time.

Another form of an oscillator using a Schmitt trigger is shown in Figure 7. This is a triangle-square wave generator, which uses an integrator and a Schmitt trigger. The equations that describe the Schmitt trigger are taken from Laboratory #7 and given here as

$$Vout = +Vcc \qquad \text{when} \quad Vx > -Vcc \frac{R1}{R2} \ . \qquad (37)$$

and

$$\text{Vout} = -\text{Vcc} \qquad \text{when } \text{Vx} < +\text{Vcc}\,\frac{\text{R1}}{\text{R2}}\ . \tag{38}$$

If Vout = +Vcc then by Equation (37), Vout switches to -Vcc when

$$\text{Vout } (+\text{Vcc} \rightarrow -\text{Vcc}) \qquad \text{when } \text{Vx} < -\text{Vcc}\,\frac{\text{R1}}{\text{R2}}\ . \tag{39}$$

and if Vout = -Vcc then by Equation (38) Vout switches to +Vcc when

$$\text{Vout } (-\text{Vcc} \rightarrow +\text{Vcc}) \qquad \text{when } \text{Vx} > +\text{Vcc}\,\frac{\text{R1}}{\text{R2}}\ . \tag{40}$$

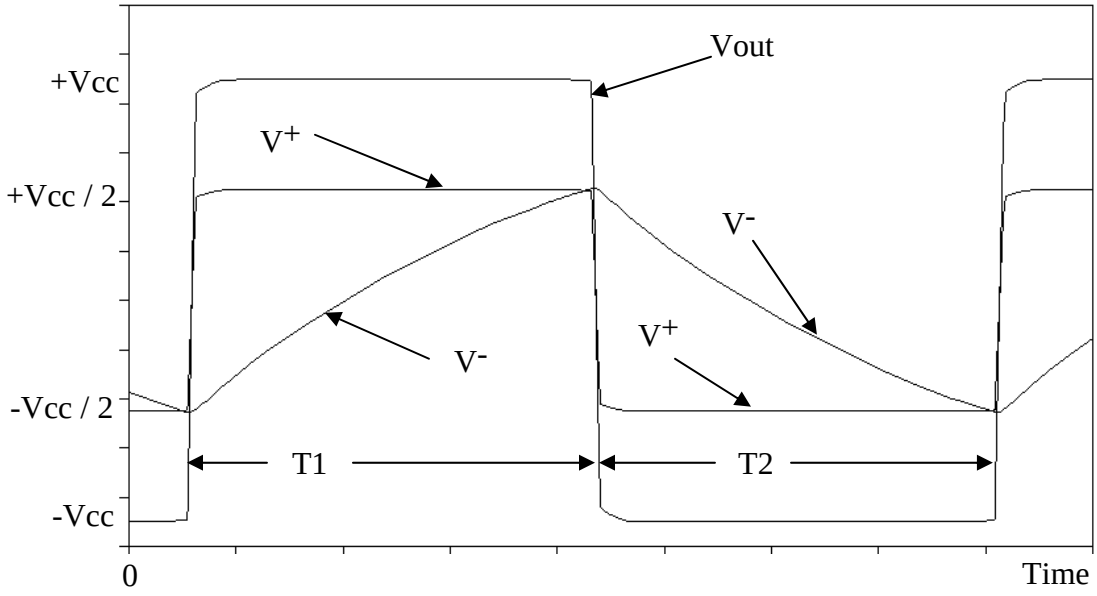


Figure 6: The Schmitt trigger oscillator waveforms.

But, Vx is nothing more than the integral of Vout since V1 = Vout.

$$\text{Vx}(t) = \frac{-1}{\text{RC}}\int_0^t \text{V1}(\tau)\, d\,\tau + \text{Vx}(0^-) = \frac{-1}{\text{RC}}\int_0^t \text{Vout}(\tau)\, d\,\tau + \text{Vx}(0^-) \quad , \tag{41}$$

where $\text{Vx}(0^-)$ is the initial voltage across the capacitor. Vout simply switches between +Vcc and -Vcc. When Vout is switching from -Vcc to +Vcc this can be modeled as a unit step with an amplitude of v1(t) = +Vcc. Substituting this value into Equation (41) gives

$$Vx(t) = \frac{-1}{RC}\int_{0}^{t} +Vcc\ d\tau = \frac{-1}{RC}(+Vcc)\cdot t + Vx(0^-) \quad . \tag{42}$$

If R2 = 2 · R1, then Vout switches from -Vcc to +Vcc when Vx = +Vcc / 2 and Vout switches from +Vcc to -Vcc when Vx = -Vcc / 2. For the case when Vout switches from -Vcc to +Vcc, the initial voltage across the capacitor $Vx(0^-)$ = +Vcc / 2. Substituting this value into Equation (42) gives

$$Vx(t) = \frac{-1}{RC}(+Vcc)\cdot t + \frac{+Vcc}{2} \quad . \tag{43}$$

The Vx(t) now decreases until it reaches a value of -Vcc / 2 at which point Vout switches to +Vcc. Setting Vout(t) = -Vcc / 2 in Equation (43) and solving for t gives the total time, T2, for Vout = -Vcc

$$T2 = RC \quad . \tag{44}$$

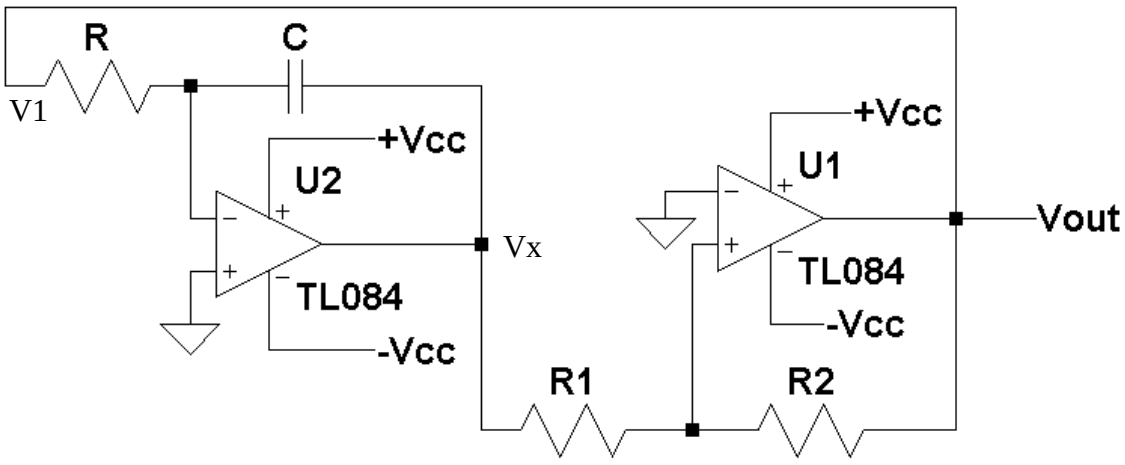


Figure 7: Triangle-square wave waveform generator.

Using Equation (41) and substituting V1(t) = -Vcc and with the initial voltage across the capacitor $Vx(0^-)$ = -Vcc / 2 gives

$$Vx(t) = \frac{-1}{RC}(-Vcc)\cdot t + \frac{-Vcc}{2} \tag{45}$$

Equation (45) describes the case when Vout = +Vcc. At the point Vout switches from +Vcc back to -Vcc, Vx = +Vcc / 2. Substituting this value into Equation (45) and solving for T gives the total time T1 with Vout = +Vcc:

$$T1 = RC \quad . \tag{46}$$

The total period of oscillation is then defined as

$$Tp = RC + RC = 2 \cdot RC \quad . \tag{47}$$

And the frequency of oscillation

$$f = \frac{1}{Tp} = \frac{1}{2 \cdot RC} \quad . \tag{44}$$

Figure 7 gives the signal waveforms for Vout and Vx. Also shown in Figure 6 are T1 and T2.

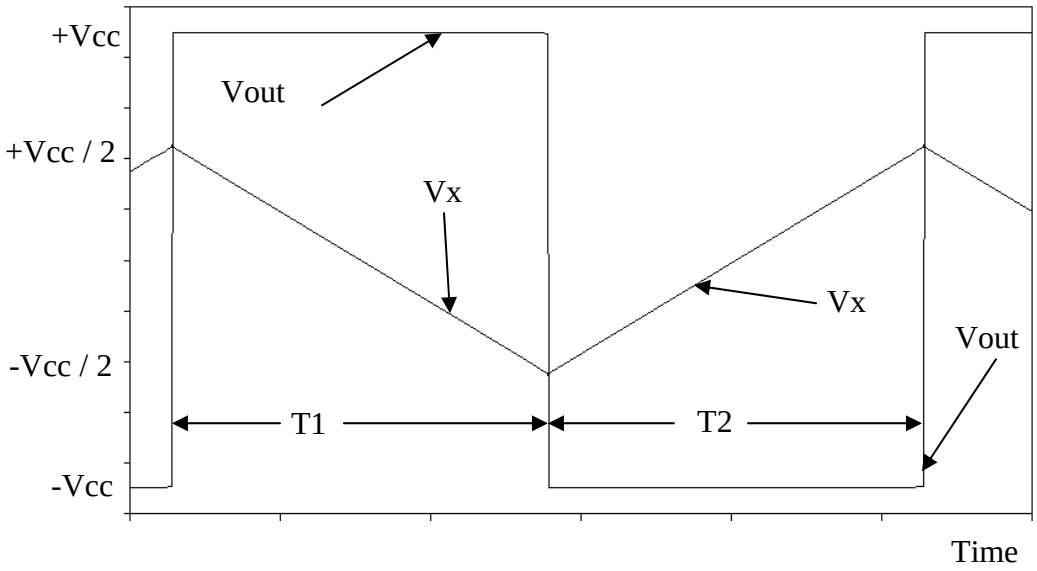


Figure 8: The Triangle-Square wave waveforms.

Procedure:

General Setup:

1. Record the model and serial number of the oscilloscope, power supply, multimeter and function generator used in laboratory experiment.
2. When measuring any values make sure to measure all inputs as well as the output of the circuit. Do not rely on the values indicated on the instruments. Always measure all signal values.
3. Before turning any power on double check the wiring to make sure that it is correct.
4. Measure all resistors that are used in the amplifier circuits using the multimeter and record these values.
5. Use all measured values to determine experimental results such as gain and current.
6. Comparing data means to calculate the percent difference between two values. For example, theoretical values versus measured values.

7. Comparing data graphically means to plot the data on the same plot to see how the data overlaps.

Oscillators and Waveform Generator Circuits

1. Using an op-amp with +Vcc set to +15 volts and -Vcc set to -15 volts, design and build the phase shift oscillator circuit of Figure 1. Be certain to include bypass capacitors at the two power supplies, of value 100μF each. Set ωo = 5,773 rad / sec. Use a resistor box for R2. Adjust R2 until oscillation occurs (somewhere above 8 · R). Measure this value of R2 and include it in the laboratory report.
2. From the output waveform determine the frequency of oscillation and the peak-to-peak value. Obtain oscilloscope waveforms of Vout as a function of time.
3. Increase R2 to about 15 · R and repeat step 2. Discuss the difference observed in between steps 2 and 3.
4. Using an op-amp with +Vcc set to +15 volts and -Vcc set to -15 volts, design and build the Wien-bridge oscillator circuit of Figure 3. Be certain to include bypass capacitors at the two power supplies, of value 100μF each. Set ωo = 10,000 rad / sec. Use a resistor box for R2. Adjust R2 until oscillation occurs (somewhere above 2 · R1). Measure this value of R2 and include it in the laboratory report.
5. From the output waveform determine the frequency of oscillation and the peak-to-peak value. Obtain oscilloscope waveforms of Vout as a function of time.
6. Increase R2 to 8 · R1 and repeat step 5. Discuss the difference observed in between steps 5 and 6.
7. Using an op-amp with +Vcc set to +15 volts and -Vcc set to -15 volts, design and build the Schmitt trigger oscillator circuit of Figure 5. Be certain to include bypass capacitors at the two power supplies, of value 100μF each. Set fo = 1000 Hz.
8. Obtain oscilloscope waveforms of Vout, V-, and V+ as a function of time.
9. Determine the frequency of oscillation the duty cycle, and the peak-to-peak value of Vout.
10. By changing the capacitor, increase the frequency of oscillation until Vout is no longer an acceptable square wave. Measure this frequency and include it in the laboratory report. Obtain oscilloscope waveforms of Vout as a function of time.
11. Disconnect R2 from ground and apply a 0 to 5 volt voltage source between the disconnected end of R2 and ground. Determine the frequency of oscillation, the duty cycle, and the peak-to-peak value of Vout. Obtain oscilloscope waveforms of Vout as a function of time.
12. Using an op-amp with +Vcc set to +15 volts and -Vcc set to -15 volts, design and build the triangle-square wave waveform generator circuit of Figure 7. Be certain to include bypass capacitors at the two power supplies, of value 100μF each. Set fo = 1000 Hz.
13. Obtain oscilloscope waveforms of Vout and Vx as a function of time. Determine the frequency of oscillation and the peak-to-peak value of Vout.

Report: Please follow the procedures in this laboratory manual for writing the report for this experiment. Include in your report:

1. The equipment used model and serial number.
2. Laboratory partners
3. Date and time data was taken.
4. Your laboratory report should include the goal of the laboratory experiment.
5. The procedures.
6. The pre-laboratory results.
7. All calculations for each step.
8. All plots (oscilloscope waveforms) generated for each step.
9. All comparisons calculations.
10. For each data collection step in the procedure, there should be either data collected, a calculation performed, a waveform recorded. Please include these in the report.
11. Short summary discussing what is observed for each of the steps given in the laboratory experiment.
12. Also include what you learned.

EXPERIMENT #9

The 555 Timer

Goals:
To introduce the concepts of using the versatile LM555 timer as a monostable pulse generator, an astable oscillator and as a pulse width modulator. The internal block diagram of the LM555 will also be presented.

References:

Microelectronics-Circuit Analysis and Design, D. A. Neamen, McGraw-Hill, 4th Edition, 2007, ISBN: 978-0-07-252362-1.

The following link is to the Tektronix website for the user manual for the DPO 4034B oscilloscope:
http://www2.tek.com/cmswpt/madetails.lotr?ct=MA&cs=mur&ci=16272&lc=EN

Equipment:

Oscilloscope: DPO 4034B
Function Generator: AFG3022B
Triple Power supply
Capacitors available in the laboratory
Resistors available in the laboratory (use a minimum of 1k resistors)
Multimeter
LM555 (NE555) Universal Timer

Pre-laboratory:

Read this laboratory experiment carefully to become familiar with the background and the procedural steps in this experiment. Carefully read each section and become familiar with the equations for each circuit.

Using the simulation package of your choice in which you are the most familiar with: Multisim, Workbench or LTSpice IV simulate the various oscillator and waveform generator circuits.

a. Using LM555 with +Vcc set to +10 volts, design and simulate the astable oscillator of Figure 3(a) with fo = 1000 Hz and with a duty cycle of 33%.
b. Record Vout, and the Threshold Pin 7 simulated waveforms. Compare these two waveforms to the waveforms given in Figure 4. How are they the same and how are they different?
c. What is the frequency and duty cycle for this circuit.
d. Add a 1N5818 diode across Rb as shown in Figure 5.
e. Record Vout and the Threshold Pin 7 simulated waveforms.

f. What is the measured frequency and duty cycle for this circuit?
g. Using LM555 with +Vcc set to +10 volts design and simulate the monostable oscillator of Figure 6 with a pulse width of 0.5 millisecond. For V3, use a square wave with a 50% duty cycle that goes from 0 to +Vcc / 2 with a frequency of 200 Hz.
h. Record Vout, V3, and the Trigger Pin 2 simulated waveforms. How does Vout and Trigger Pin 2 of Step g compare to the plot given in Figure 8?
i. Using LM555 with +Vcc set to +10 volts and -Vcc set to -10 volts design and simulate the pulse width modulator of Figure 9 with a pulse width of 0.2 milliseconds. This is the same circuit as the monostable circuit but with the addition of a unity gain buffer and an additional signal source Vg.
j. Set V3 to a 0 to +Vcc / 2 square wave with a 50% duty cycle and a frequency of 2000 Hz.
k. Set Vg = 6.67 volts DC and measure Tp from the simulated waveform for Vout and compare this result to what is expected from Equation (16).
l. Set Vg to a sine wave with a peak value of 3 volts and an offset of 4 volts so that Vg varies in a sinusoidal manner from 1 volt to 7 volts.
m. Measure Vout and Vg simulated waveforms. Compare these results to that given in Figure 10.

Discussion:

The LM555 / NE555 timer is a versatile integrated circuit that can be configured as an oscillator, a pulse width modulator and a single, variable width, pulse generator known as an astable oscillator or one shot. Most datasheets give many other application of this device. Figure 1 is the pin-out for the LM555 timer and Figure 2 gives the internal block diagram. The LM555 contains two voltage comparators, one *set-reset* (RS, also SR) *flip-flop* (also *latch* or *register*), one inverter and one open collector NPN transistor. The voltage divider composed of R1, R2 and R3 set the voltage at the V^- input of comparator C2 (Pin 5) to 2/3 +Vcc and the V+ input of comparator C1 to 1/3 +Vcc. The transistor Q1 (Pin 7) is typically used as a method of discharging any timing capacitors used in any timing circuit configurations.

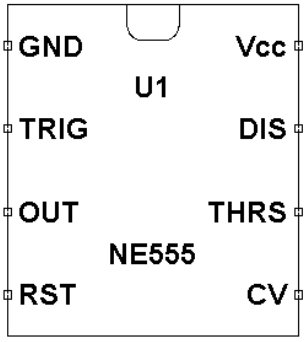


Figure1: The pin-out for the LM555 timer IC.

The set-reset flip-flop (RS-FF) is placed in a set or reset condition depending on the R and S inputs. Table 1 gives the output Q of the RS-FF as a function of R and S. When R = 0, S = 0, the RS-FF is in a hold state and Q does not change. When R = 1 and S = 0, the RS-FF is in a reset state and Q goes to 0 and when R = 0, S = 1, the RS-FF is in a set state and Q = 1. The condition for R = 1, S = 1, is not allowed. There is also the ability to externally reset the RS-FF using the RESET NOT pin (Pin 4).

Table 1 The Next State Table for and RS-FF

R	S	Q Old	QNew
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	X
1	1	1	X

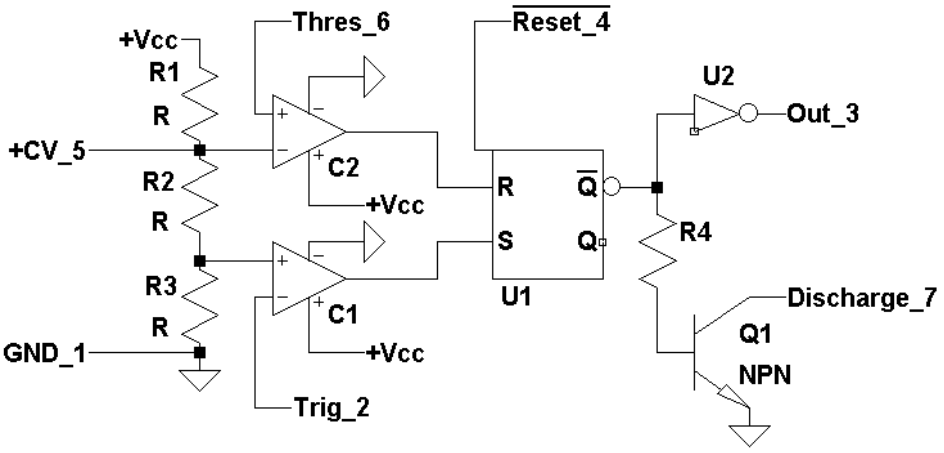
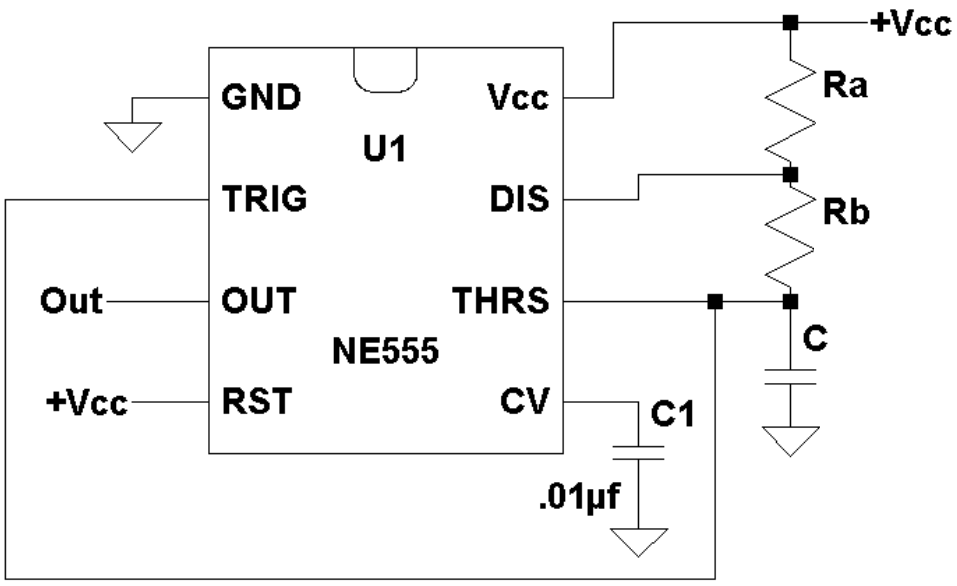
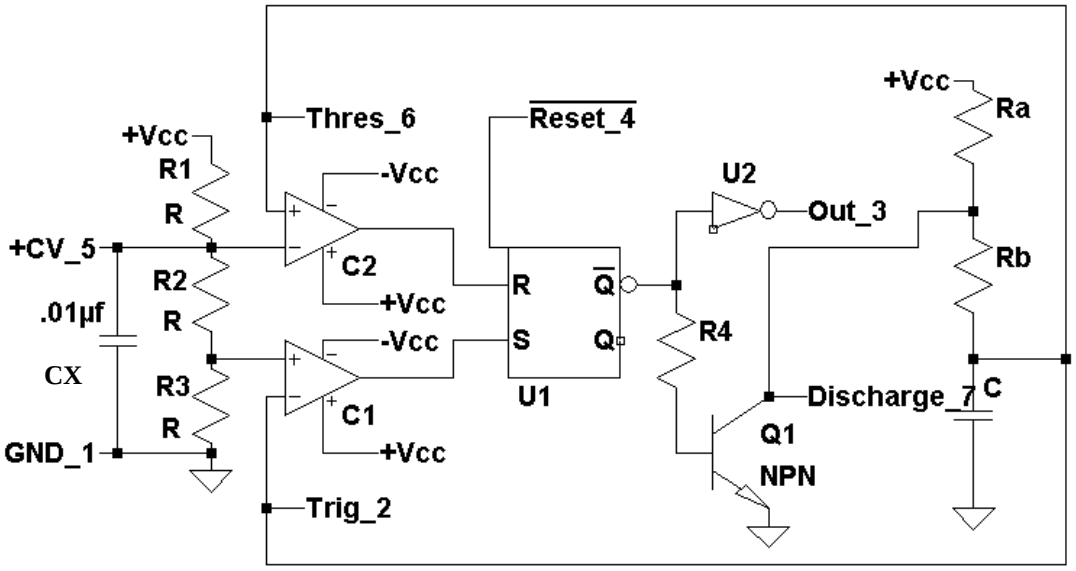


Figure 2: Functional block diagram for the LM555 Timer

Figure 3(a) shows the LM555 timer configured as an astable oscillator (the output indefinitely changes states between Vcc and 0). Resistors Ra, Rb, and capacitor C form the timing network that determines the frequency of oscillation and the duty cycle of the square wave output. Figure 3(b) gives the same astable oscillator circuit showing also the internal functional block diagram for the LM555 timer. Capacitor CX in Figure 3(a) is used as a bypass filter for the reference voltages going to the two comparators C1 and C2. The capacitor is used to filter any noise that may be present on +Vcc to maintain a constant reference voltage on V^+ of C1 and V^- on C2.



(a)



(b)

Figure 3: (a) The external circuit diagram of the LM555 timer configured as an astable oscillator and (b) the same circuit showing the internal functional block diagram of the LM555 timer.

Assuming initially Q = 1, the transistor Q1 is off, and the initial voltage across the capacitor is just slightly greater than 1/3 +Vcc. Since the Trigger input (pin 2) and Threshold (pin 6) are tied together, $V^+ < V^-$ of C2 and $V^+ < V^-$ of C1, the output of both C1 and C2 are 0. The RS-FF is in a hold condition maintaining Q = 1. The capacitor C starts to charge toward +Vcc through Ra and Rb. Equation (32) from laboratory experiment 8 gives the voltage across the capacitor as

$$Vpin\_2(t) = Vf + (Vi - Vf)e^{-t/RC} \quad , \qquad (1)$$

where Vf is the final voltage and Vi is the initial voltage across the capacitor. Substituting Ra + Rb for R, Vi = 1/3 +Vcc, and Vf = +Vcc gives

$$Vpin\_2(t) = +Vcc + (-2/3 +Vcc)e^{-t/(Ra+Rb)C} \quad , \qquad (2)$$

Figure 4 shows the voltage across the capacitor C and Vout as a function on time. The capacitor initially has a voltage 1/3 +Vcc and starts charging toward +Vcc. The capacitor continues to charge to +Vcc until the voltage across the capacitor reaches 2/3 +Vcc. At this point, $V^+ > V^-$ of C2 and $V^+ < V^-$ of C1 yielding the output of C2 = 1 and the output of C1 = 0. This sets the RS-FF to a reset condition changing Q = 0. The output Vout = 0, and Qnot of U1 is now 1, turning on the transistor Q1. This starts discharging the capacitor C toward 0. When the voltage across the capacitor goes below 2/3 +Vcc, $V < V^-$ of C2 and $V^+ > V^-$ of C1, yielding the output C2 = 0 and the output of C1 = +0. The RS-FF is now in hold condition leaving Q = 0 of the RS-FF and the transistor Q1 on continuing to discharge the capacitor.

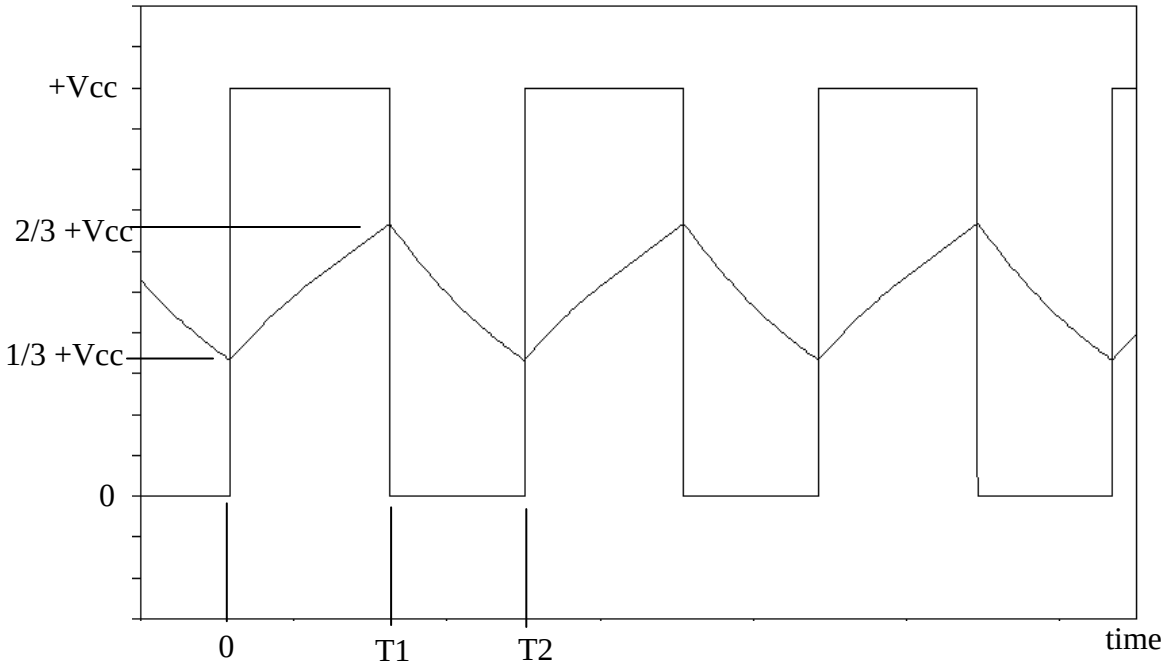


Figure 4: Vout and the voltage across the capacitor C as a function of time.

The time T1 it takes to charge to 2/3 +Vcc is found by substituting +2/3 +Vcc for Vpin_2(t) into Equation (2) and solving for t

$$T1 = \ln(2) \cdot (Ra + Rb) \cdot C \quad . \tag{3}$$

During the charge cycle the capacitor C discharges through Rb and the transistor Q1. The voltage across the capacitor is then defined as

$$Vpin\_2(t) = (2/3 + Vcc)e^{-(t - T1)/Rb\,C} \quad , \tag{4}$$

The capacitor C continues to discharge until it reaches a voltage of 1/3 +Vcc. At this point, $V^+ < V^-$ of C2 and $V^+ > V^-$ of C1, yielding the output C2 = 0 and the output of C1 = 1. This sets the output of the RS-FF to the condition Q =1. The transistor Q1 turns off and Vout goes to 1 starting a new cycle of oscillation. The time it takes T2 - T1 to discharge the capacitor to 1/3 +Vcc is found by substituting this value into Equation (4) for Vpin_2(t) and solving for t -T1, with t = T2

$$T2 - T1 = \ln(2) \cdot (Rb) \cdot C \tag{5}$$

The total time period of oscillation T2 is found by adding Equations (3) and (5) together

$$T2 = \ln(2) \cdot (Ra + 2 \cdot Rb) \cdot C \tag{6}$$

The frequency of oscillation which is given by 1 / T2 is

$$f = \frac{1}{\ln(2) \cdot (Ra + 2 \cdot Rb) \cdot C} = \frac{1.44}{(Ra + 2 \cdot Rb) \cdot C} \quad . \tag{7}$$

The duty cycle which is defined as the time the output is low to the total time period is

$$D\% = \frac{T2 - T1}{T2} = \frac{Rb}{Ra + 2 \cdot Rb} \cdot 100\% \quad . \tag{8}$$

A closer investigation of Equation (8) yields that for a 50% duty cycle, Ra would have to be zero which is not possible for the astable oscillator circuit configuration of Figures 3(a) and (b). To build an astable oscillator with a 50% duty cycle requires the addition of a diode, as shown in Figure 5. During charging of capacitor C, the diode is on. Essentially Rb is in parallel with the on-state (forward-biased) resistance of the diode, which is typically much smaller than the resistance Rb. For the most part, this parallel combination can be considered as zero ohms. The best diode to use in this configuration is a Schottky diode, as this

diode has a much smaller turn-on voltage than a regular diode. Since the parallel combination of Rb and the forward-biased diode (on) resistance is approximately zero ohms, the capacitor only charges through resistor Ra yielding a charge time for T1 of

$$T1 = \ln(2) \cdot Ra \cdot C \quad . \tag{9}$$

When the capacitor is discharging, the diode is on and the capacitor discharges through Rb as described by equation (4) yielding a discharge time of

$$T2 - T1 = \ln(2) \cdot Rb \cdot C \; . \tag{10}$$

The total period of oscillation is then given by adding Equations (9) and (10) together

$$T2 - T1 = \ln(2) \cdot (Ra + Rb) \cdot C \; . \tag{11}$$

and the frequency of oscillation as

$$f = \frac{1}{\ln(2) \cdot (Ra + Rb) \cdot C} = \frac{1.44}{(Ra + Rb) \cdot C} \quad . \tag{12}$$

The duty cycle is then given by

$$D\% = \frac{T2 - T1}{T2} = \frac{Rb}{Ra + Rb} \cdot 100\% \tag{13}$$

If Ra = Rb, then the duty cycle reduces to 50%.

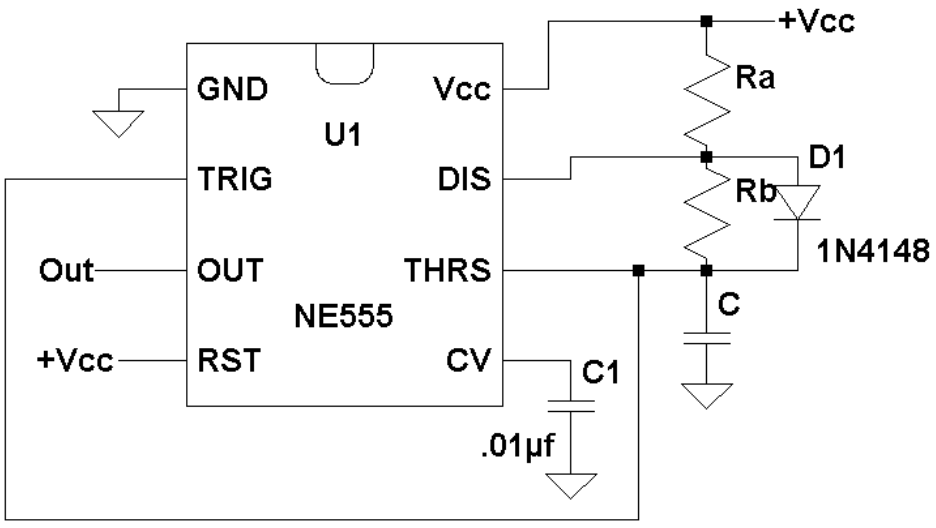


Figure 5: An astable oscillator using the LM555 timer with a 50% duty cycle.

The LM555 timer can also be configured as a monostable oscillator generating a single pulse of a given pulse width when triggered. Figure 6 shows the LM555 timer in a monostable configuration. Ra and C determine the pulse width. R1, R2, C1, D1, and D2 form an input network to trigger the LM555 timer. V3 is assumed to be a pulse input in the range of 0 to +Vcc / 2. Diodes D1 and D2 are used to protect pin 2 of the LM555 timer. D1 turns on when the trigger input exceeds +Vcc + Vd (the forward diode voltage) and D2 turns on when the trigger input goes below -Vd. These two diodes guarantee that the trigger input is bounded between -Vd to +Vcc + Vd protecting this input pin. Resistors R1, R2 and the capacitor C2 form a highpass filter used to take the derivative of the input V3. The trigger input which has the steady input of +Vcc / 2 uses the edges of V3 to trigger a single pulse output from the LM555 timer. Figure 7 shows the trigger input and the V3 supply. Note how the input network has taken the derivative of V3. The trigger input (Pin 2) is nothing more the derivative of V3 superimposed on a +Vcc /2 offset due to the steady value of the trigger input of +Vcc / 2.

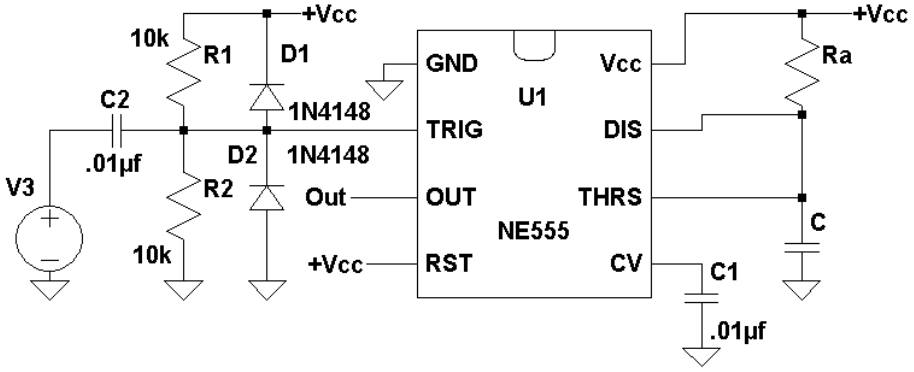


Figure 6: The LM555 timer in a monostable configuration.

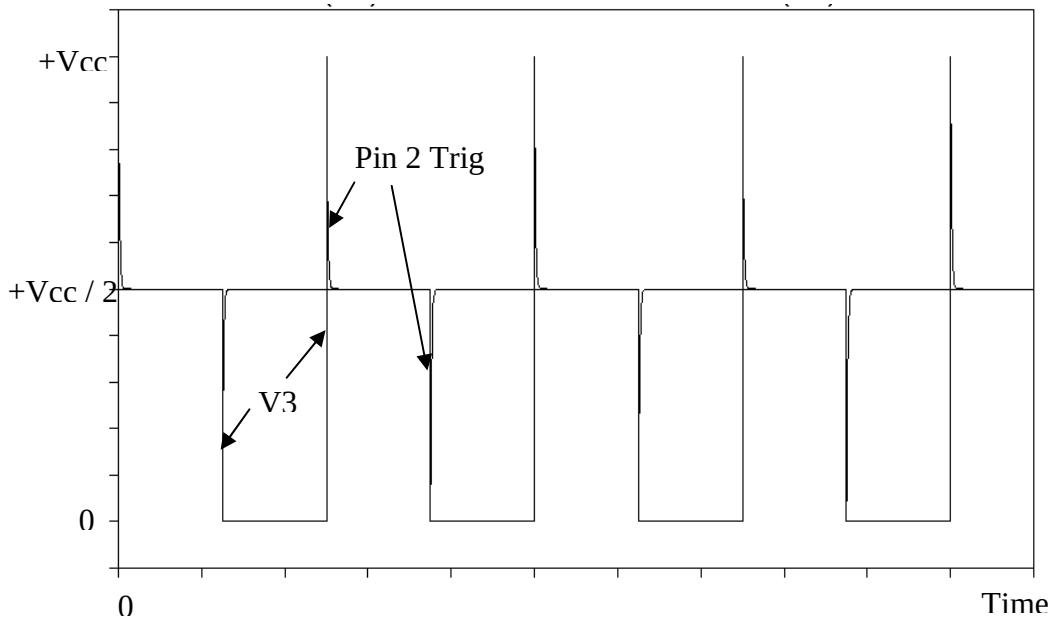


Figure 7: The trigger input to the monostable oscillator circuit given in Figure 6.

A negative going edge on the trigger input starts a trigger event that generates a single pulse. At this point in time, the voltage on the capacitor C is 0 volts. The trigger event on the trigger input sets the RS-FF to a set condition (C2 = 0 , and C1 = 1 from Figure 2) and starts capacitor C charging through Ra. As the trigger input returns to its steady state value of +Vcc / 2, $V^+ < V^-$ of C1 and $V^+ < V^-$ of C2 (see Figure 2) yielding the output C1 = 0 and the output of C2 = 0. This sets the RS-FF to a hold condition leaving RS-FF output Q = 1 (see Figure 2). With Q = 1, Qnot = 0 and the transistor Q1 is still off and the capacitor continues to charge through Ra toward +Vcc. This capacitor continues to charge until it reaches a voltage of 2/3 +Vcc. At this point, $V^+ > V^-$ of C1 and $V^+ < V^-$ of C2 yielding the output C1 = 1 and the output of C2 = 0, setting the RS-FF to a reset condition. This turns on Q1 discharging the capacitor C to 0. Starting with Equation (1) with Vf = +Vcc and the initial voltage across the capacitor C, Vi = 0 gives

$$Vpin\_2(t) = +Vcc\ (1 - e^{-t/RaC}) \quad . \tag{14}$$

The capacitor C charges towards +Vcc until it reaches the value 2/3 +Vcc. At this point, $V^+ < V^-$ of C1 and $V^+ > V^-$ of C2 yielding the output C1 = 0 and the output of C2 = 1. This sets the RS-FF to a reset condition leaving Q = 0. With Q = 0, Qnot = 1, transistor Q1 turns on and the capacitor discharges to zero where the capacitor voltage stays at this value until another negative-going trigger pulse occurs on the trigger input.

The total time Tp it takes the capacitor to reach 2/3 +Vcc is found by substituting this value into Equation (14) and solving for t

$$Tp = \ln(3) \cdot Ra \cdot C \tag{15}$$

Figure 8 shows Vout, the voltage across the capacitor C, Vcapacitor, and the trigger input as a function of time.

Since the pulse width of the monostable oscillator circuit depends on the charging to the voltage of 2/3 +Vcc, changing this voltage value changes the time it takes for condition of $V^+ > V^-$ of C2 and $V^+ < V^-$ of C1. At this point, the outputs C1 = 0 and C2 = 1 setting the RS-FF to reset state on the transistor Q1 and discharging the capacitor C to zero. Removing the 0.01 μf capacitor applied to the CV input and applying a varying voltage as shown in Figure 9 will vary the pulse width of the pulse output. The op-amp circuit is nothing more than a unity gain buffer isolating the voltage source Vg from reference voltage CV input of the LM555 timer. Letting Vg be the voltage on the CV input, the total time Tp to reach this voltage on the capacitor is

$$Tp = - Ra \cdot C \cdot \ln\left(1 - \frac{Vg}{+Vcc}\right) \tag{16}$$

Figure 9 is nothing more than a pulse width modulator (PWM) with the pulse width proportional to the input voltage Vg. Figure 10 gives an example of Vout as a function Vg. For this example, +Vcc = 10 volts and Vg is a sine wave with a peak value of 3 volts and an offset of 4 volts so that Vg varies in a sinusoidal manner from 1 volt to 7 volts. Figure 9 shows how the pulse width increases as the value of Vg increases.

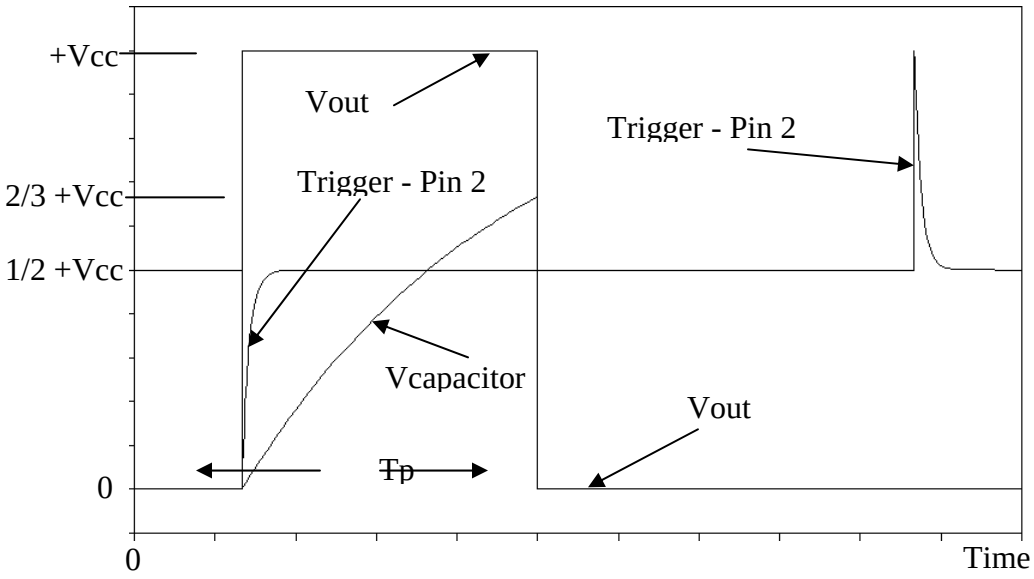


Figure 8: Vout, the voltage across the capacitor C Vcapacitor, and the trigger input Pin 2 as a function of time for monostable oscillator circuit given in Figure 6.

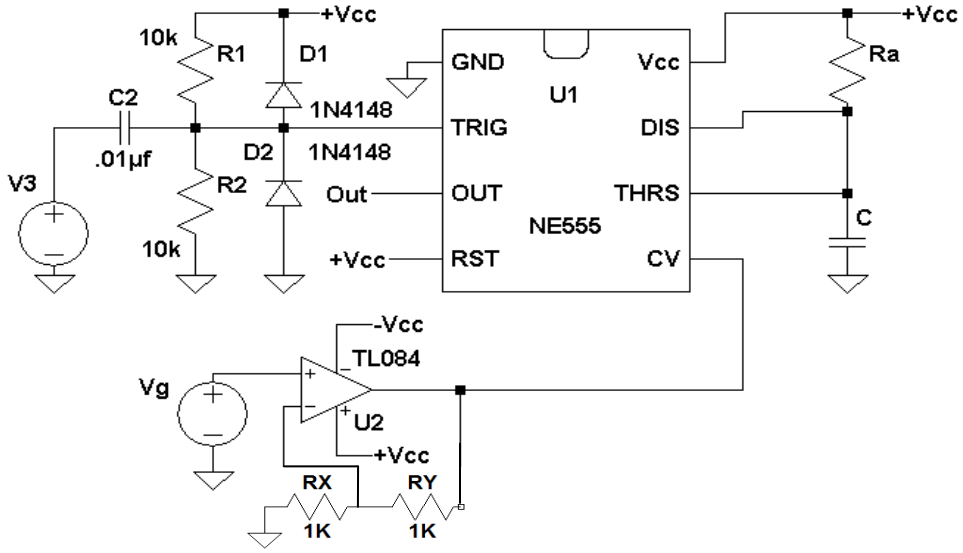


Figure 9: A LM555 timer configured as a pulse width modulator.

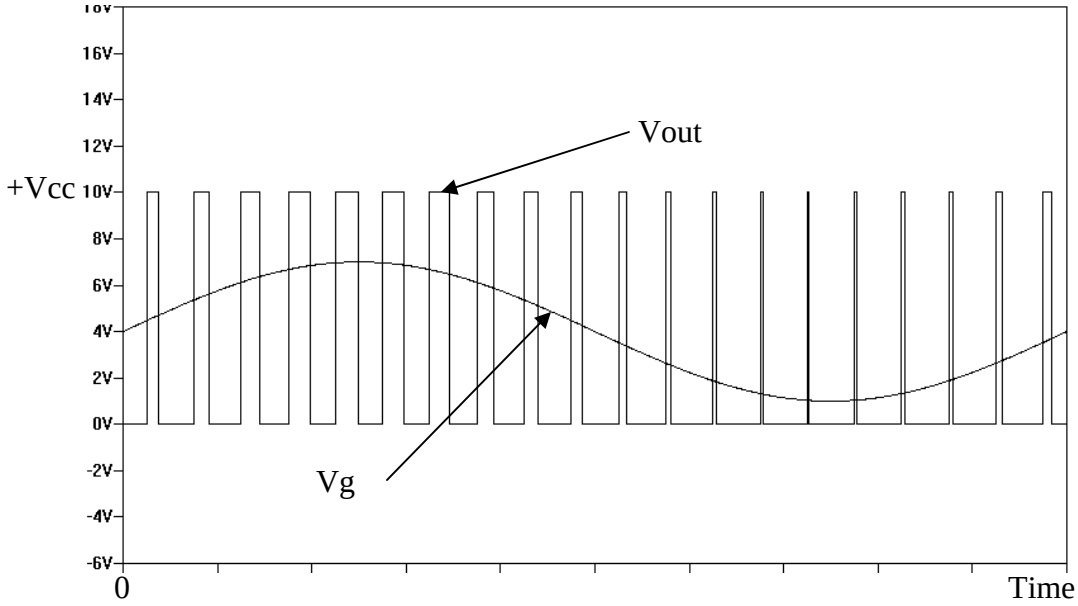


Figure 10: An example of using the LM555 timer as a pulse width modulator.

Procedure:

General Setup:

1. Record the model and serial number of the scope, power supply, multimeter and function generator used in laboratory experiment.
2. When measuring any values make sure to measure all inputs as well as the output of the circuit. Do not rely on the values indicated on the instruments. Always measure all signal values.
3. Before turning any power on double check the wiring to make sure that it is correct.
4. Measure all resistors that are used in the amplifier circuits using the multimeter and record these values.
5. Use all measured values to determine experimental results such as gain and current.
6. Comparing data means to calculate the percent difference between two values. For example, theoretical values versus measured values.
7. Comparing data graphically means to plot the data on the same plot to see how the data overlaps.

The LM555 Universal Timer Circuits

1. Using an LM555 timer with +Vcc set to +10 volts, design and build the astable oscillator of Figure 3(a) with fo = 1000 Hz and with a duty cycle of 33% (as defined in Equation (8)).
2. Measure and record with an oscilloscope Vout, and the threshold input (pin 7). Compare these two waveforms to the waveforms given in Figure 4. How are they same and how are they different?
3. What is the measured frequency and duty cycle for this circuit.
4. Compute the percentage difference between the measured and original design

requirements for the frequency and the duty cycle. Discuss the differences in the laboratory report.

5. What is the value on the threshold input (pin 7) when Vout changes states?
6. Setting the oscilloscope to AC coupling, and increasing the vertical sensitivity of the oscilloscope measure and record the voltage at +Vcc Pin 8. Discuss what you observe in the laboratory report.
7. Now connect at least a 10μf capacitor between +Vcc Pin 8 and ground and repeat Step 6. Discuss what you observe in the laboratory report. Leave this capacitor connected between +Vcc and ground for the rest of the laboratory experiment.
8. Add a 1N4148 diode across Rb as shown in Figure 5.
9. Measure and record with an oscilloscope Vout, and the threshold input (pin 7).
10. What is the measured frequency and duty cycle for this circuit.
11. How did adding the diode change the frequency and duty cycle? How does the measured frequency compare to the values calculated from Equations (12) and (13)?
12. Using an LM555 timer with +Vcc set to +10 volts design and build the monostable oscillator of Figure 6 with fo = 1000 Hz and with a pulse width of 0.5 millisecond. For V3, use a square wave with a 50% duty cycle that goes from 0 to +Vcc / 2 with a frequency of 200 Hz.
13. Measure and record with an oscilloscope Vout, V3 and the trigger input (pin 2).
14. How does Vout and the trigger input of Step 14 compare to the plot given in Figure 8?
15. Measure the actual pulse width of Vout and compare this result to Equation (15).
16. Using an LM555 timer with +Vcc set to +10 volts and -Vcc set to -10 volts design and build the pulse width modulator of Figure 9 with a pulse width of 0.2 milliseconds. This is the same circuit as the monostable circuit but with the addition of a 2X non-inverting amplifier and an additional signal source Vg.
17. Set V3 to 0 to +Vcc / 2, square wave with a 50% duty cycle and a frequency of 2000 Hz.
18. Set Vg = 6.67 volts DC and measure Tp. Compare this result to what is expected from Equation (16).
19. Varying Vg from 0.5 to 4 volts (0.5, 1.5, 3.5 and 4), measure Tp and compare these values to the results expected from Equation (16).
20. Set Vg to a sine wave with a peak value of 1.5 volts and an offset of 2 volts so that Vg varies in a sinusoidal manner from 0.5 volt to 3.5 volts (Note: On the AFG3022 Function Generator, make sure that the Frequency CH1= CH2 is "Off").
21. Measure and record with an oscilloscope Vout and Vg. Compare these results to that given in Figure 9.

Report: Please follow the procedures in this laboratory manual for writing the report for this experiment. Include in your report:

1. The equipment used model and serial number.

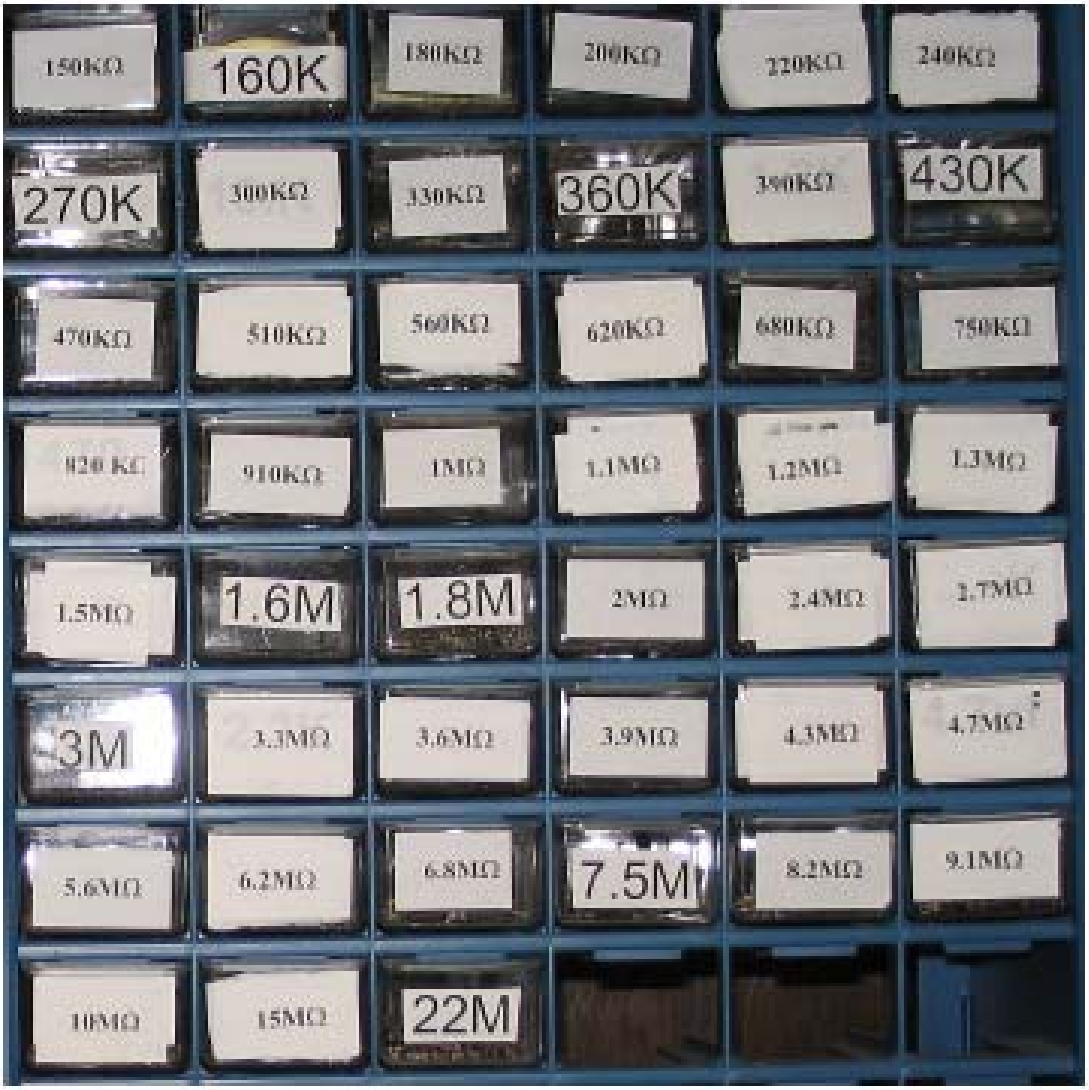
2. Laboratory partners
3. Date and time data was taken.
4. Your laboratory report should include the goal of the laboratory experiment.
5. The procedures.
6. The pre-laboratory results.
7. All calculations for each step.
8. All plots (oscilloscope waveforms) generated for each step.
9. All comparisons calculations.
10. For each data collection step in the procedure, there should be either data collected, a calculation performed, a waveform recorded. Please include these in the report.
11. Short summary discussing what is observed for each of the steps given in the laboratory experiment.
12. Also include what you learned.

APPENDICES

Appendix A

Available Resistors and Capacitors

Appendix A


150KΩ
160K
180KΩ
200KΩ
220KΩ
240KΩ
270K
300KΩ
330KΩ
360K
390KΩ
430K
470KΩ
510KΩ
560KΩ
620KΩ
680KΩ
750KΩ
820 KΩ
910KΩ
1MΩ
1.1MΩ
1.2MΩ
1.3MΩ
1.5MΩ
1.6M
1.8M
2MΩ
2.4MΩ
2.7MΩ
3M
3.3MΩ
3.6MΩ
3.9MΩ
4.3MΩ
4.7MΩ
5.6MΩ
6.2MΩ
6.8MΩ
7.5M
8.2MΩ
9.1MΩ
10MΩ
15MΩ
22M

Appendix A


100pF
120pF
150pF
180pF
200pF
220pF
270pF
330pF
390pF
470pF
560pF
680pF
820pF
0.001uF
0.0012uF
0.0015uF
0.0018uF
0.002uF
0.0022uF
0.0027uF
0.0033uF
0.0039uF
0.0047uF
0.005uF
0.0056uF
0.0068uF
.01uf
.015uf
.022uf
0.047uF
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10uf
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